SIEMENS

Microcomputer Components Data Catalog 1985/86

MC Components and Memories

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All dimensions are specified in mm.

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SAB 80286 High-performance microprocessor with memory management and protection
management and protection
SAB 80515/80535 8-bit single-chip microcontroller
SAR 80C482 8 bit single object CMOS microscoptroller
SAB 80C482 8-bit single-chip CMOS microcontroller
Peripheral Components
SAB 179X Floppy disk formatter/controller family
SAB 2793A/2797A Floppy disk formatter/controller family
SAB 7201A Multi-protocol serial communications controller
SAB 81C52 256 × 8-bit static CMOS RAM NMOS-compatible
SAB 8155 2048-bit static MOS RAM with I/O ports and timer
SAB 8237A High-performance programmable DMA controller 513
SAB 8256A Programmable multifunction UART (MUART)
SAB 8259A Programmable interrupt controller
SAB 8275 Programmable CRT controller
SAB 8276 Small system CRT controller
SAB 8282A/8283A Octal latch
SAB 8284B Clock generator and driver for SAB 8086 family processors 631
SAB 8286A/8287A Octal bus transceiver
SAB 8288A Bus controller for SAB 8086 family processors
SAB 8289 Bus arbiter
SAB 82200 Local bus arbiter
SAB 82220 Bus interface controller
SAB 82258 Advanced DMA controller for 16-bit MC systems
SAB 82284 Clock generator and ready interface for
SAB 80286 processors
SAB 82288 Bus controller for SAB 80286 processors
SAB 82289 Bus arbiter for SAB 80286 processor family
SAB 82520 High-level serial communications controller 803
SAB 82731 Dot rate generator

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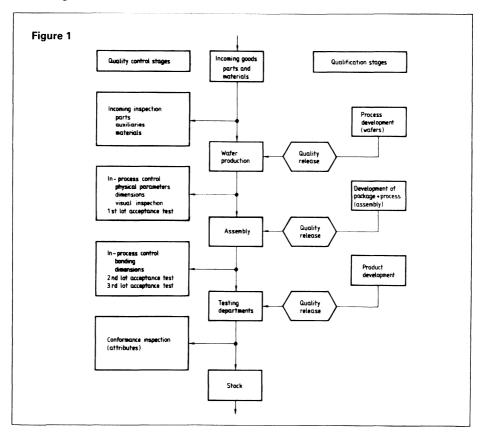
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Memory Compon	ents							
HYB 4116	RAM dyn., 16384 × 1 bit .							835
HYB 4164	RAM dyn., 65536 × 1 bit .							845
HYB 41256	RAM dyn., 262144 × 1 bit							861
HYB 41257	RAM dyn., 262144 × 1 bit							879
Siemens Offices								897

Quality Assurance

1 Quality Assurance System

The high quality and reliability of integrated circuits from Siemens is the result of a carefully arranged production which is systematically checked and controlled at each stage. The procedures are subject to a quality assurance system; full details are given in brochure "Siemens Quality Assurance System – Integrated Circuits" (SQS-IC).

Figure 1 shows the most important stages of the "SQS-IC". A quality assurance (QA) department which is independent of production and development departments, is responsible for the selected control measures, acceptance procedures, and information feedback loops. This department has state-of-the-art test and measuring equipment at its disposal, works according to approved methods of statistical quality control, and is provided with facilities for accelerated life and environmental tests used for both qualification and routine monitoring tests.



The latest methods and equipment for preparation and analysis are employed to continuously improve quality and reliability.

Quality Assurance

2 Conformance

Each integrated circuit is subject to a final test at the end of the production process. This test is carried out by computer-controlled, automatic test systems because hundreds of thousands of operating conditions as well as many static and dynamic parameters are to be considered. Moreover, these test systems are extremely reliable and reproducible. The quality assurance department finally checks the ICs in the form of a lot-by-lot sampling inspection to additionally ensure this minimum failure rate as well as the acceptable quality level (AQL). Sampling inspection is performed in accordance with the inspection plans of DIN 40080, as well as of the identical MIL-STD-105 or IEC 410.

The table below shows the results of such sampling inspections performed with hundreds of thousands of ICs in 1984. Those results correspond to the average outgoing quality (AOQ), and are specified as defectives per million (DPM).

	Total defects	Sum of electrical defects	Sum of mechanical defects
	AOQ (DPM)	AOQ (DPM)	AOQ (DPM)
SSI/MSI ≤ 1000 gate functions	60	300	500
LSI/VLSI ≥ 1000 gate functions	400	800	600

3 Reliability

3.1 Measures Taken during Development

The reliability of ICs is already considerably influenced at the development stage. Siemens has, therefore, fixed certain design standards for the development of circuit and layout, specifying e.g. minimum width and spacing of conductive layers on a chip, dimensions and electrical parameters of protective circuits for electrostatic charge, etc. An examination with the aid of carefully arranged programs run on large-scale computers, guarantees an immediate identification and elimination of unintentional offenses against those design standards.

3.2 In-Process Control during Production

Manufacturing of integrated circuits comprises several hundred production steps. As each step is to be executed with utmost accuracy, the in-process control is of outstanding importance. Some processes involve more than hundred different test measures. The tests have been arranged such that the individual process steps are continuously reproducible.

The decreasing failure rates reflect the never ending effort towards this direction; in the course of years they have been reduced considerably despite an immense rise in the IC's complexity.

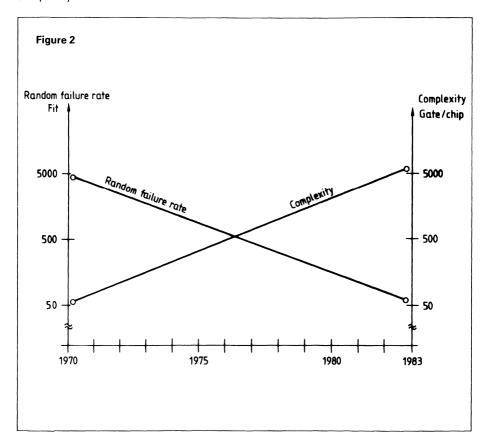
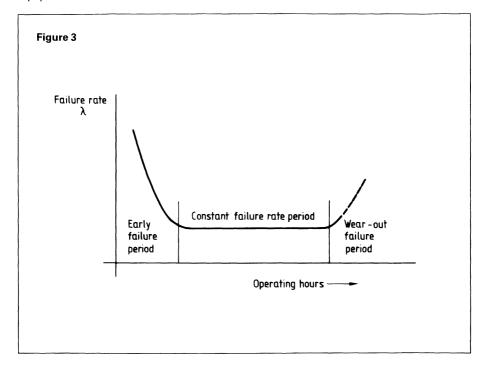


Figure 2 shows the general course of the failure rate for digital MOS ICs in fit for the years 1970 to 1983. The increasing complexity as regards gate functions/chip is also specified.

3.3 Reliability Monitoring

The general course of the IC's failure rate versus time is shown by a so-called "bathtub" curve (figure 3). The failure rate has its peak during the first few operating hours (early failure period). After the early failure period has decayed, the "constant" failure rate period starts during which the failures may occur at an approximately uniform rate. This period ends with a repeated rise of the curve during the wear-out failure period. For ICs, however, the latter period lies usually far beyond the service life specified for the individual equipment.



Reliability tests for ICs are usually destructive examinations. They are, therefore, carried out with samples. Most failure mechanisms can be accelerated by means of higher temperatures. Due to this temperature dependence, the time required to simulate a future operational behavior can be shortened by applying high temperatures; this is called life test.

The acceleration factor B for the life test can be obtained from the Arrhenius equation

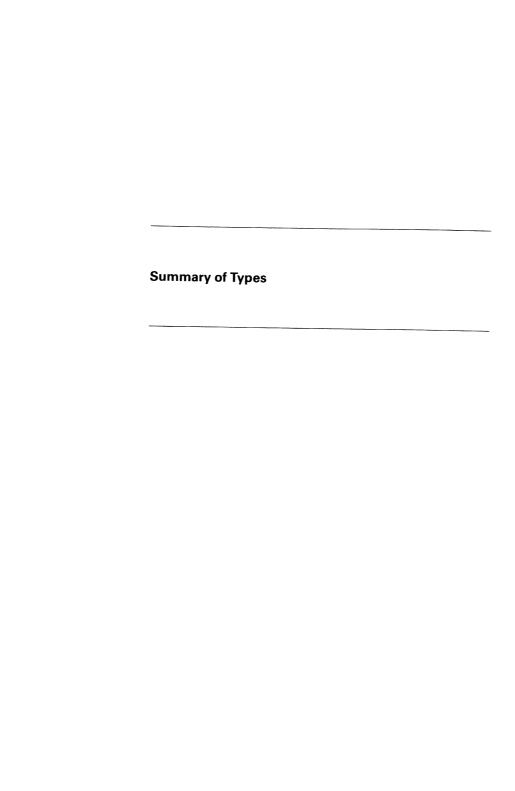
$$B = \exp(E_A/k [T_2 - T_1])$$

where T_2 is the temperature at which the life test is performed, T_1 is the assumed operating temperature, and k is the Boltzmann constant.

Important for factor B is the activation energy E_A which lies between 0.3 and 1.3 eV and differs considerably for the individual failure mechanisms.

For all Siemens ICs, the reliability data gathered from life tests is converted to an operating temperature of Tamb = $40\,^{\circ}$ C, assuming an average activation energy of 0.4 eV. The acceleration factor for life tests is thus 24, compared with operational behavior. This method considers also failure mechanisms with low activation energy, i.e. which are only slightly accelerated by the temperature effect.

Various reliability tests are periodically performed with IC types that are representative of a certain production line – this is described in the brochure "SQS-IC". Such tests are e.g. humidity test at 85°C and 85% relative humidity, pressure cooker test, as well as life tests up to 1000 hours and more. Test results are available in the form of summary reports.



Summary of Types (incl. ordering codes)

Type	Function	Ordering	Page	
		Ceramic	Plastic	
Microcontroller and	Microprocessor Components			
SAB 8031A	8-bit single-chip MC without internal ROM		Q67120-C183	27
SAB 8031A-T40/85	8-bit single-chip MC extended temperature range		Q67120-C230	47
SAB 8031A-T40/110	8-bit single-chip MC extended temperature range		Q67120-C232	47
SAB 8031A-15	8-bit single-chip MC (15 MHz) without internal ROM	_	Q67120-C189	27
SAB 8032A	8-bit single-chip MC without internal ROM		Q67120-C196	65
SAB 8032A-T40/85	8-bit single-chip MC without internal ROM	_	Q67120C235	83
SAB 8032A-T40/100	8-bit single-chip MC without internal ROM	-	Q67120-C239	83
SAB 8035L	8-bit single-chip MC without internal ROM		Q67120-C43	117
SAB 8035L-T40/85	8-bit single-chip MC extended temperature range, without internal ROM	_	Q67120-C140	101
SAB 8048	8-bit single-chip MC with mask-programmable ROM		Q67120-C32	117
SAB 8048-T40/85	8-bit single-chip MC with mask-programmable ROM, extended temperature range	_	Q67120-C133	101
SAB 8048-T40/110	8-bit single-chip MC with mask-programmable ROM, extended temperature range	_	Q67120-C162	101

Type	Function	Ordering Co	Page	
		Ceramic	Plastic	
SAB 8051A	8-bit single-chip MC with mask-programmable ROM	_	Q67120-C186	27
SAB 8051A-T40/85	8-bit single-chip MC with mask-programmable ROM, extended temperature range	_	Q67120-C233	47
SAB 8051A-T40/110	8-bit single-chip MC with mask-programmable ROM, extended temperature range	_	Q67120-C231	47
SAB 8051A-15	8-bit single-chip MC (15 MHz) with mask-programmable ROM	_	Q67120-C214	27
SAB 8052A	8-bit single-chip MC with mask-programmable ROM	_	Q67120-C195	65
SAB 8052A-T40/85	8-bit single-chip MC with mask-programmable ROM, extended temperature range	_	Q67120-C247	83
SAB 8052A-T40/100	8-bit single-chip MC with mask-programmable ROM, extended temperature range	_	Q67120-C248	83
SAB 8085A	8-bit microprocessor, 3 MHz		Q67120-C34	135
SAB 8085A-2	8-bit microprocessor, 5 MHz		Q67120-C41	135
SAB 8085AH	8-bit microprocessor, 3 MHz	_	Q67120-C122	163
SAB 8085AH-2	8-bit microprocessor, 5 MHz		Q67120-C124	163
SAB 8086	16-bit microprocessor, 5 MHz	Q67120-C45	Q67120-C116	191
SAB 8086-1	16-bit microprocessor, 10 MHz	Q67120-C104	Q67120-C141	191
SAB 8086-2	16-bit microprocessor, 8 MHz	Q67120-C60	Q67120-C142	191
SAB 8088	8-bit microprocessor, 5 MHz		Q67120-C106	231
SAB 8088-2	8-bit microprocessor, 8 MHz		Q67120-C213	
	High-integration 16-bit microprocessor	_		261
	High-integration 8-bit microprocessor		_	263

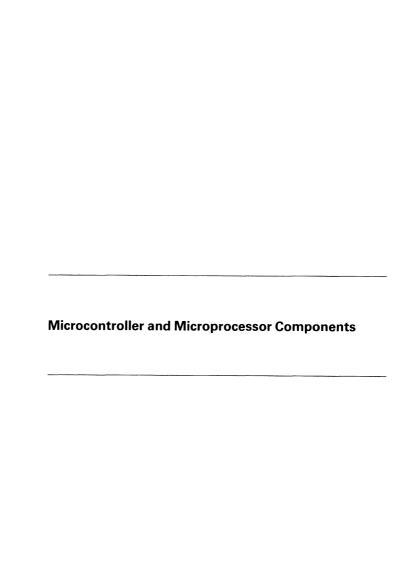
Туре	Function	Ordering Co Ceramic	de Plastic	Page
SAB 80215	8-bit single-chip MC with mask-programmable ROM	_	Q67120-C81	265
SAB 80286	High-performance 16-bit microprocessor with memory management and protection, 8 MHz (CLCC)	Q67120-C151		303
SAB 80286-CG	High-performance 16-bit microprocessor with memory management and protection, 8 MHz (pin grid array)	Q67120-C222	_	303
SAB 80286-CG T0/55	High-performance 16-bit microprocessor with memory management and protection, 8 MHz (PGA, restr. temp.)	Q67120-C255	_	303
SAB 80286-6	High-performance 16-bit microprocessor with memory management and protection, 6 MHz (CLCC)	Q67120-C226		303
SAB 80286-6-CG	High-performance 16-bit microprocessor with memory management and protection, 6 MHz (pin grid array)	Q67120-C228	3 —	303
SAB 80286-6-CG T0/55	High-performance 16-bit microprocessor with memory management and protection, 6 MHz (PGA, restr. temp.)	Q67120-C256	5 —	303
SAB 80315	MC like SAB 80215 but with external EPROM (piggyback version)	Q67120-C82	_	265
SAB 80515	8-bit single-chip MC with mask-programmable ROM,	_	Q67120-C211	367
SAB 80515-T40/85			Q67120-C210	367

Туре	Function	Ordering	Page	
		Ceramic	Plastic	
SAB 80535	8-bit single-chip MC without internal ROM		Q67120-C241	367
SAB 80535-T40/85	8-bit single-chip MC extended temperature range, without internal ROM	_	Q67120-C240	367
SAB 80C382	8-bit single-chip CMOS MC without internal ROM	_	Q67100-H3205 Q67100-H3199	397
SAB 80C482	8-bit single-chip CMOS MC		Q67100-Z154	397
Peripheral Compon	ents			
SAB 1791-02	Floppy disk controller, inverted data bus, single-sided		Q67120-Y39	427
SAB 1793-02	Floppy disk controller, true data bus, single-sided		Q67120-Y40	427
SAB 1795-02	Floppy disk controller, inverted data bus, double-sided	_	Q67120-Y46	427
SAB 1797-02	Floppy disk controller, true data bus, double-sided		Q67120-Y47	427
SAB 2793A-02	Floppy disk controller, true data bus, single-sided		Q67120-Y82	453
SAB 2797A-02	Floppy disk controller, true data bus, double-sided	_	Q67120-Y84	453
SAB 7201A	Multiprotocol serial communications controller	_		483
SAB 81C52	256×8 -bit static CMOS RAM, NMOS-compatible	_	Q67100-Q486	485

Type	Function	Ordering Co	Page	
		Ceramic	Plastic	
SAB 8155	RAM stat., 2048 bit with I/O ports and timer	_	Q67120-Q42	495
SAB 8155-2	RAM stat., 2048 bit with I/O ports and timer	_	Q67120-Q86	495
SAB 8237A	High-performance programmable DMA controller, 3 MHz	_	Q67120-Y49	513
SAB 8237A-5	High-performance programmable DMA controller, 5 MHz	***************************************	Q67120-Y72	513
SAB 8256A	Programmable multifunction UART (MUART), 3 MHz	Q67120-Y55	Q67120-Y43	531
SAB 8256A-2	Programmable multifunction UART (MUART), 5 MHz	Q67120-Y58	Q67120-Y59	531
SAB 8259A	Programmable interrupt controller, 5 MHz	_	Q67120-P46	559
SAB 8259A-2	Programmable interrupt controller, 8 MHz	_	Q67120-P81	559
SAB 8275	Programmable CRT controller, 2 MHz	_	Q67120-P58	571
SAB 8275-2	Programmable CRT controller, 3 MHz	_	Q67120-P92	571
SAB 8276	Small system CRT controller, 2 MHz	_	Q67120-P83	599
SAB 8276-2	Small system CRT controller, 3 MHz		Q67120-P93	599
SAB 8282A	Octal latch, non-inverted data		Q67020-Y149	625
SAB 8283A	Octal latch, inverted data		Q67020-Y150	625
SAB 8284B	Clock generator for SAB 8086 family processors, 8 MHz	_	Q67020-Y151	631
SAB 8284B-1	Clock generator for SAB 8086 family processors, 10 MHz	_	Q67020-Y152	631

Туре	Function	Ordering C	Ordering Code		
	**************************************	Ceramic	Plastic		
SAB 8286A	Octal bus transceiver, non-inverted data	_	Q67020-Y153	645	
SAB 8287A	Octal bus transceiver, inverted data	_	Q67020-Y154	645	
SAB 8288A Bus controller for SAB 8086 family processors		_	Q67020-Y155	653	
SAB 8289	Bus arbiter, 8 MHz	_	Q67020-Y74	665	
SAB 8289-1	Bus arbiter, 10 MHz		Q67120-Y85	665	
SAB 82200	Local bus arbiter	_		677	
SAB 82220	Bus interface controller			679	
SAB 82258	Advanced DMA controller for 16-bit MC systems	Q67120-P122	2 —	681	
SAB 82284	Clock generator for SAB 80286 family processors, up to 16 MHz		Q67020-Y162	729	
SAB 82284-6	Clock generator for SAB 80286 family processors, up to 12 MHz	_	Q67020-Y165	729	
SAB 82288	Bus controller for SAB 80286 processors, up to 16 MHz		Q67120-Y75	741	
SAB 82288-6	Bus controller for SAB 80286 processors, up to 12 MHz	_	Q67120-Y110	741	
SAB 82289	Bus arbiter for SAB 80286 processor family, 16 MHz		Q67020-Y77	769	
SAB 82289-6	Bus arbiter for SAB 80286 processor family, 12 MHz	_	Q67120-Y111	769	
SAB 82520	High-level serial communi- cations controller	_		803	
SAB 82731	Dot rate generator, 50 MHz		Q67020-Y114	805	
SAB 82731-2	Dot rate generator, 80 MHz		Q67020-Y118	805	

Туре	Function	Ordering	Page	
		Ceramic	Plastic	
Memory Compo	nents			
HYB 4116-2	RAM dyn., 16384×1 bit access time 150 ns	_	Q67100-Q308	835
HYB 4116-3	RAM dyn., 16384×1 bit access time 200 ns		Q67100-Q306	835
HYB 4164-1	RAM dyn., 65536×1 bit access time 120 ns		Q67100-Q339	845
HYB 4164-2	RAM dyn., 65536×1 bit, access time 150 ns	_	Q67100-Q325	845
HYB 4164-3	RAM dyn., 65536×1 bit, access time 200 ns		Q67100-Q326	845
HYB 41256-12	RAM dyn., 262144×1 bit access time 120 ns	_	Q67100-Q346	861
HYB 41256-15	RAM dyn., 262144×1 bit access time 130 ns	_	Q67100-Q347	861
HYB 41256-20	RAM dyn., 262144×1 bit access time 200 ns	_ ·	Q67100-Q348	861
HYB 41257-12	RAM dyn., 262144×1 bit access time 120 ns	_	Q67100-Q349	879
HYB 41257-15	RAM dyn., 262144×1 bit access time 150 ns	_	Q67100-Q350	879
HYB 41257-20	RAM dyn., 262144 \times 1 bit access time 200 ns	_	Q67100-Q351	879



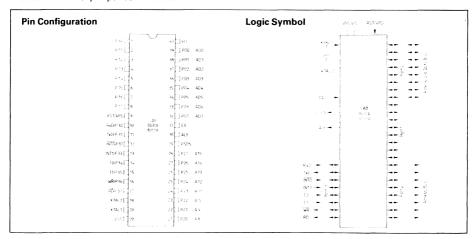
Preliminary

SAB 8031A/8051A SAB 8031A-15/8051A-15 8-Bit Single-Chip Microcontroller

SAB 8031A/8031A-15 Control Oriented CPU with RAM and I/O SAB 8051A/8051A-15 A SAB 8031A with Factory Mask-Programmable ROM

- SAB 8031A/8051A, 12 MHz Operation SAB 8031A-15/8051A-15, 15 MHz Operation
- 4K × 8 ROM
- 128 × 8 RAM
- Four 8-Bit Ports, 32 I/O Lines
- Two 16-Bit Timer/Event Counters
- High-Performance Full-Duplex Serial Channel
- External Memory Expandable to 128K

- Compatible with SAB 8080/8085 Peripherals
- Boolean Processor
- 218 User Bit-Addressable Locations
- Most Instruction Execute in: 1 µs (SAB 8031A/8051A) 800 ns (SAB 8031A-15/8051A-15)
- 4 μs (3.2 μs) Multiply and Divide



The SAB 8031A/8051A is a stand-alone, high-performance single-chip computer fabricated in +5V advanced Siemens MYMOS technology and packaged in a 40-pin DIP. It provides the hardware features, architectural enhancements and new instructions that are necessary to make it a powerful and cost effective controller for applications requiring up to 64 Kbytes of program memory and/or up to 64 Kbytes of data storage.

The SAB 8051A contains a non-volatile 4K \times 8 readonly program memory; a volatile 128 \times 8 read/write

data memory; 32 I/O lines; two 16-bit timer/counters; a five-source, two-priority-level, nested interrupt structure; a serial I/O port for either multiprocessor communications, I/O expansion, or full duplex UART; and on-chip oscillator and clock circuits. The SAB 8031A is identical, except that it lacks the program memory.

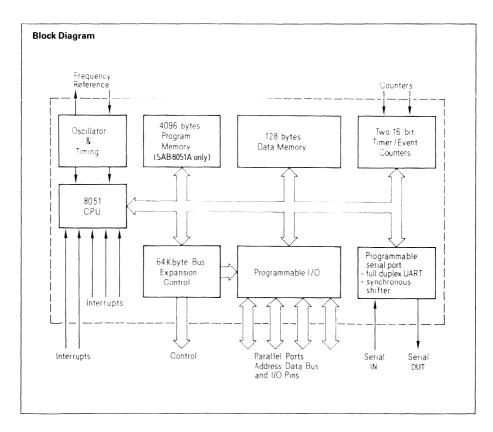
For systems that require extra capability, the SAB 8051A can be expanded using standard TTL compatible memories and the byte oriented SAB 8080 and SAB 8085 peripherals.

Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Functions
P1.0-P1.7	1-8	I/O	Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. Port 1 can sink/source four LS TTL loads.
RST/VPD	9	1	A high level on this pin resets the SAB 8051A. A small internal pulldown resistor permits power-on reset using only a capacitor connected to VCC. If VPD is held within its spec while VCC drops below spec, VPD will provide standby power to the RAM. When VPD is low, the RAM's current is drawn from VCC.
P3.Ø-P3.7	10-17	1/0	Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and RD and WR pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source four LS TTL loads. The secondary functions are assigned to the pins of Port 3, as follows: RXD/data (P3.0). Serial port's receiver data input (asynchronous) or data input/output (synchronous). TXD/clock (P3.1). Serial port's transmitter data output (asynchronous) or clock output (synchronous). INTO (P3.2). Interrupt 0 input or gate control input for counter 0. INT1 (P3.3). Interrupt 1 input or gate control input for counter 1. T0 (P3.4). Input to counter 0. T1 (P3.5). Input to counter 0. T1 (P3.6). The write control signal latches the data byte from port 0 into the external data memory. RD (P3.7). The read control signal enables external data memory to port 0.
XTAL1 XTAL2	19 18	1	XTAL 1 input to the oscillator's high gain amplifier. Required when a crystal is used. Connect to VSS when external source is used on XTAL 2. XTAL 2 output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal or external source can be used.
P2.0-P2.7	21-28	1/0	Port 2 is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source four LS TTL loads.
PSEN	29	0	The program store enable output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses Remains high during internal program execution.
ALE	30	0	Provides address latch enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.

Pin Definitions and Functions (continued)

Symbol	Number	Input (I) Output (O)	Functions
ĒĀ	31	1	When held at a TTL high level, the SAB 8051A executes instructions from the internal ROM when the PC is less than 4096. When held at a TTL low level, the SAB 8051A fetches all instructions from external program memory. For the SAB 8031A this pin must be tied low.
P0.0-P0.7	39-32	1/0	Port 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source eight LS TTL loads.
VCC	40		+5V power supply during operation and program verification.
VSS	20		Circuit ground potential.



Instruction Set Description

Mnemonic		Description	Byte	Cycle
Arithmetic op	erations			
ADD	A, Rn	Add register to Accumulator	1	1
ADD	A, direct	Add direct byte to Accumulator	2	1
ADD	A, @Ri	Add indirect RAM to Accumulator	1	1
ADD	A,#data	Add immediate data to Accumulator	2	1
ADDC	A,Rn	Add register to Accumulator with Carry flag	1	1
ADDC	A,direct	Add direct byte to Accu with Carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to Accu with Carry flag	1	1
ADDC	A,#data	Add immediate data to Accu with Carry flag	2	1
SUBB	A,Rn	Subtract register from Accu with borrow	1	1
SUBB	A,direct	Subtract direct byte from Accu with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	Α	Increment Accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	Α	Decrement Accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A & B	1	4
DIV	AB	Divide A & B	1	4
DA	Α	Decimal adjust Accumulator	1	1
Logical operat	tions			
ANL	A,Rn	AND register to Accumulator	1	1
ANL	A,direct	AND direct byte to Accumulator	2	1
ANL	A,@Ri	AND indirect RAM to Accumulator	1	1
ANL	A,#data	AND immediate data to Accumulator	2	1
ANL	direct,A	AND Accumulator to direct byte	2	1

Instruction Set Description (continued)

Mnemonic		Description	Byte	Cycle
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to Accumulator	1	1
ORL	A,direct	OR direct byte to Accumulator	2	1
ORL	A,@Ri	OR indirect RAM to Accumulator	1	1
ORL	A,#data	OR immediate data to Accumulator	2	1
ORL	direct,A	OR Accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive-OR register to Accumulator	1	1
XRL	A,direct	Exclusive-OR direct byte to Accumulator	2	1
XRL	A,@Ri	Exclusive-OR indirect RAM to Accumulator	1	1
XRL	A,#data	Exclusive-OR immediate data to Accumulator	2	1
XRL	direct,A	Exclusive-OR Accumulator to direct byte	2	1
XRL	direct,#data	Exclusive-OR immediate data to direct	3	2
CLR	А	Clear Accumulator	1	1
CPL	Α	Complement Accumulator	1	1
RL	Α	Rotate Accumulator left	1	1
RLC	А	Rotate A left through the Carry flag	1	1
RR	Α	Rotate Accumulator right	1	1
RRC	Α	Rotate A right through Carry flag	1	1
SWAP	Α	Swap nibbles within the Accumulator	1	1

Data transfer

MOV	A,Rn	Move register to Accumulator	1	1
MOV	A,direct*)	Move direct byte to Accumulator	2	1
MOV	A,@Ri	Move indirect RAM to Accumulator	1	1
MOV	A,#data	Move immediate data to Accumulator	2	1
MOV	Rn,A	Move Accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move Accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct	3	2

^{*)} MOV A, ACC is not a valid instruction

Instruction Set Description (continued)

Mnemonic		Description	Byte	Cycle
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move Accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
Data transfer (c	ont.)			
MOVC	A,@A+DPTR	Move code byte relative to DPTR to Accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to Accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr) to Accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr) to Accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with Accumulator	1	1
XCH	A,direct	Exchange direct byte with Accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with Accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit ind. RAM with Accu	1	1
Boolean variabl	e manipulation			
CLR	С	Clear Carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	С	Set Carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	С	Complement Carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to Carry flag	2	2
ANL	C,/bit	AND complement of direct bit to Carry	2	2
ORL	C,bit	OR direct bit to Carry flag	2	2
ORL	C,/bit	OR complement of direct bit to Carry	2	2
MOV	C,bit	Move direct bit to Carry flag	2	1
MOV	bit,C	Move Carry flag to direct bit	2	2

Instruction Set Description (continued)

Mnemonic		Description	Byte	Cycle
Program and r	nachine control			
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if Accumulator is zero	2	2
JNZ	rel	Jump if Accumulator is not zero	2	2
JC	rel	Jump if Carry flag is set	2	2
JNC	rel	Jump if Carry flag is not set	2	2
JB	bit,rel	Jump if direct bit set	3	2
JNB	bit,rel	Jump if direct bit not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct to accu and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to accu and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp.immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2
NOP		No operation	1	1

rel

Notes on data addressing modes:

Rn - Working register R0-R7

direct – 128 internal RAM locations, any I/O port, control or status register

@Ri – Indirect internal RAM location addressed by register R0 or R1

#data - 8-bit constant included in instruction

#data 16 - 16-bit constant included as bytes 2 & 3 of instruction

bit – 128 software flags, any I/O pin, control or status bit

- Accumulator

Accumulator

Notes on program addressing modes:

addr 16 — Destination address for LCALL & LJMP may be anywhere within the 64-Kbyte program memory address space.

addr 11 – Destination address for ACALL & AJMP will be within the same 2-Kbyte page of program memory as the first byte of the following instruction.

 SJMP and all conditional jumps include an 8-bit offset byte. Range is + 127/ – 128 bytes relative to first byte of the following instruction.

All mnemonics copyrighted © Intel Corporation 1979

Instruction Opcodes in Hexadecimal Order

Hex Code	Number of Bytes	Mnemonic	Operands	Hex Code	Number of Bytes	Mnemonic	Operands
00	1	NOP		34	2	ADDC	A,#data
00 01	2	AJMP	code addr	35	2	ADDC	A,data addr
		LJMP	code addr	36	1	ADDC	A.@R0
02	3	RR	A	37	1	ADDC	A,@R1
03	1	INC	A	38	l i	ADDC	A,R0
04	1	INC	data addr	39	l i	ADDC	A,R1
05	2		@R0	3A	1	ADDC	A,R2
06	1	INC		3B	i	ADDC	A,R3
07	1	INC	@R1	3C	1	ADDC	A,R4
80	1	INC	R0	3D	1	ADDC	A,R5
09	1	INC	R1		1	ADDC	A,R7
0A	1	INC	R2	3E	1	ADDC	A,R7
0B	1	INC	R3	3F			code addr
0C	1	INC	R4	40	2	JC	ļ
0D	1	INC	R5	41	2	AJMP	code addr
0E	1	INC	R6	42	2	ORL	data addr,A
0F	1	INC	R7	43	3	ORL	data addr,#data
10	3	JBC	bit addr code addr	44	2	ORL	A,#data
11	2	ACALL	code addr	45	2	ORL	A,data addr
12	3	LCALL	code addr	46	1	ORL	A,@R0
13	1	RRC	Α	47	1	ORL	A,@R1
14	1	DEC	Α	48	1	ORL	A,R0
15	2	DEC	data addr	49	1	ORL	A,R1
16	1	DEC	@R0	4A	1	ORL	A,R2
17	1	DEC	@R1	4B	1	ORL	A,R3
18	1	DEC	R0	4C	1	ORL	A,R4
19	1	DEC	R1	4D	1	ORL	A,R5
1A	1	DEC	R2	4E	1	ORL	A,R6
1B	l i	DEC	R3	4F	1	ORL	A,R7
1C	1	DEC	R4	50	2	JNC	code addr
1D	1	DEC	R5	51	2	ACALL	code addr
1E	1	DEC	R6	52	2	ANL	data addr,A
	1	DEC	R7	53	3	ANL	data addr.#data
1F	3	JB	bit addr code addr	54	2	ANL	A,#data
20	2	1	code addr	55	2	ANL	A.data addr
21		AJMP	Code addi	56	1	ANL	A,@R0
22	1	RET		50 57	1	ANL	A,@R1
23	1	RL	A	57 58	1	ANL	A,R0
24	2	ADD	A,#data		11	ANL	A,R1
25	2	ADD	A,data addr	59	1	ANL	A,R2
26	1	ADD	A,@R0	5A		ANL	A,R3
27	1	ADD	A,@R1	5B 5C	1	ANL	A,R4
28	1	ADD	A,R0		1	ANL	A,R5
29	1	ADD	A,R1	5D	1	1	A,R6
2A	1	ADD	A,R2	5E	1	ANL	
2B	1	ADD	A,R3	5F	1	ANL	A,R7
2C	1	ADD	A,R4	60	2	JZ	code addr
2D	1	ADD	A,R5	61	2	AJMP	code addr
2E	1	ADD	A,R6	62	2	XRL	data addr,A
2F	1	ADD	A,R7	63	3	XRL	data addr,#data
30	3	JNB	bit addr, code addr	64	2	XRL	A,#data
31	2	ACALL	code addr	65	2	XRL	A,data addr
32	1	RETI		66	1	XRL	A,@R0
33	1	RLC	Α	67	1	XRL	A,@R1

Instruction Opcodes in Hexadecimal Order (continued)

Hex Code	Number of Bytes	Mnemonio	Operands	Hex Code	Number of Bytes	Mnemonic	Operands
68	1	XRL	A,R0	9C	1	SUBB	A,R4
69	1	XRL	A,R1	9D	1	SUBB	A,R5
6A	1	XRL	A,R2	9E	1	SUBB	A,R6
6B	1	XRL	A,R3	9F	1	SUBB	A,R7
6C	1	XRL	A,R4	A0	2	ORL	C,/bit addr
6D	1	XRL	A,R5	A1	2	AJMP	code addr
6E	1	XRL	A,R6	A2	2	MOV	C,bit addr
6F	1	XRL	A,R7	A3	1	INC	DPTR
70	2	JNZ	code addr	A4	1	MUL	AB
71	2	ACALL	code addr	A5		reserved	,
72	2	ORL	C,bit addr	A6	2	MOV	@R0,data addr
73	1	JMP	@A+DPTR	A7	2	MOV	@R1,data addr
74	2	MOV	A,#data	A8	2	MOV	R0,data addr
75	3	MOV	data addr, #data	A9	2	MOV	R1,data addr
76	2	MOV	@R0,#data	AA	2	MOV	R2,data addr
77	2	MOV	@R1,#data	AB	2	MOV	R3,data addr
78	2	MOV	R0,#data	AC	2	MOV	R4,data addr
79	2	MOV	R1,#data	AD	2	MOV	R5,data addr
7A	2	MOV	R2,#data	AE	2	MOV	R6,data addr
7B	2	MOV	R3,#data	AF	2	MOV	R7,data addr
7C	2	MOV	R4,#data	B0	2	ANL	C,/bit addr
7D	2	MOV	R5,#data	B1	2	ACALL	code addr
7E	2	MOV	R6,#data	B2	2	CPL	bit addr
7F	2	MOV	R7,#data	B3	1	CPL	C
80	2	SJMP	code addr	B4	3	CJNE	A,#data,code addr
81	2	AJMP	code addr	B5	3	CJNE	A,data addr.code addr
82	2	ANL	C,bit addr	B6	3	CJNE	@R0,#data,code addr
83	1	MOVC	A,@A+PC	B7	3	CJNE	@R1,#data,code addr
84	1	DIV	AB	B8	3	CJNE	R0,#data,code addr
85	3	MOV	data addr,data addr	B9	3	CJNE	R1,#data,code addr
86	2	MOV	data addr,@R0	BA	3	CJNE	R2,#data.code addr
87	2	MOV	data addr,@R1	ВВ	3	CJNE	R3,#data,code addr
88	2	MOV	data addr,R0	BC	3	CJNE	R4,#data.code addr
89	2	MOV	data addr,R1	BD	3	CJNE	R5,#data,code addr
8A	2	MOV	data addr, R2	BE	3	CJNE	R6,#data.code addr
8B	2	MOV	data addr, R3	BF	3	CJNE	R7,#data,code addr
8C	2	MOV	data addr,R4	CO	2	PUSH	data addr
8D	2	MOV	data addr, R5	C1	2	AJMP	code addr
8E	2	MOV	data addr,R6	C2	2	CLR	bit addr
8F	2	MOV	data addr,R7	C3	1	CLR	C
90	3	MOV	DPTR,#data	C4	1	SWAP	Ä
91	2	ACALL	code addr	C5	2	XCH	A,data addr
92	2	моу	bit addr,C	C6	1	XCH	A,@R0
93	1	MOVC	A,@A+DPTR	C7	1	XCH	A,@R1
94	2	SUBB	A,#data	C8	i	XCH	A,R0
95	2	SUBB	A,data addr	C9	1	XCH	A,R1
96	1	SUBB	A,@R0	CA	i	XCH	A,R2
97	i	SUBB	A,@R1	CB	i	XCH	A,R3
98	i	SUBB	A,R0	CC	i	XCH	A,R4
99	i	SUBB	A,R1	CD	1	XCH	A,R5
9A	i	SUBB	A,R2	CE	1	XCH	A,R6
9B	1	SUBB	A,R3	CF	i l	XCH	A,R7
				0.		7011	A,IV

Instruction Opcodes in Hexadecimal Order (continued)

Hex Code	Number of Bytes	Mnemonic	Operands
D0	2	POP	data addr
D1	2	ACALL	code addr
D2	2	SETB	bit addr
D3	1	SETB	С
D4	1	DA	Α
D5	3	DJNZ	data addr,code addr
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,code addr
D9	2	DJNZ	R1,code addr
DA	2	DJNZ	R2,code addr
DB	2	DJNZ	R3,code addr
DC	2	DJNZ	R4,code addr
DD	2	DJNZ	R5,code addr
DE	2	DJNZ	R6,code addr
DF	2	DJNZ	R7,code addr
E0	1	MOVX	A,@DPTR
E1	2	AJMP	code addr
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,data addr*)
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	code addr
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	data addr,A
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A
	1		L

^{*)} MOV A,ACC is not a valid instruction

Absolute Maximum Ratings¹⁾

Ambient Temperature Under Bias $0 \text{ to } 70^{\circ}\text{C}$ Storage Temperature $-65 \text{ to } +150^{\circ}\text{C}$ Voltage on Any Pin with Respect to Ground (VSS) -0.5 to +7 V Power Dissipation 2 W

D.C. Characteristics

TA = 0 to 70°C; VCC = $5V \pm 10\%$; VSS = 0V

Symbol	Parameter	Lir	Limit Values		Test Condition	
		Min.	Max.			
VIL	Input Low Voltage	-0.5	0.8			
VIH	Input High Voltage (Except RST/VPD and XTAL2)	2.0	1400 - 0.5			
VIH1	Input High Voltage to RST/VPD for Reset, XTAL2	2.5	VCC+0.5		XTAL1 to VSS	
VPD	Power Down Voltage to RST/VPD	4.5	5.5		VCC = 0V	
VOL	Output Low Voltage Ports 1, 2, 3		0.45	v	IOL = 1.6 mA	
VOL1	Output Low Voltage Port 0, ALE, /PSEN	_	0.45		IOL = 3.2 mA	
VOH	Output High Voltage Ports 1, 2, 3	2.4			IOH = -80 μA	
VOH1	Output High Voltage Port 0, ALE, /PSEN	2.4			IOH = -400 μA	
IIL	Logical 0 Input Current Ports 1, 2, 3		-800	μА	VIL = 0.45 V	
IIL2	Logical 0 Input Current XTAL 2		-2.0	mA	XTAL1 = VSS VIL = 0.45 V	
IIH1	Input High Current to RST/VPD for Reset		500	μA	VIN = VCC-1.5 V	
ILI	Input Leakage Current to Port 0,/EA	_	±10		0V < VIN < VCC	
ICC	Power Supply Current SAB 8031A/8051A SAB 8031A-15/8051A-15		125 140	mA	All outputs disconnected	
IPD	Power Down Current		10		VCC = 0V	
CIO	Capacitance of I/O Buffer		10	pF	f _c = 1 MHz	

¹⁾ Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

A.C. Characteristics for SAB 8031A/8051A

TA 0 to 70°C; VCC = 5 V \pm 10%; VSS = 0 V

(CL for Port 0, ALE and PSEN Outputs = 100 pF; CL for All Other Outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	Limit Values				
		12 MHz Clock		Variable Clock 1/TCLCL = 1.2 MHz to 12 MHz		
		Min	Max	Min	Max	
TLHLL	ALE Pulse Width	127		2TCLCL-40		
TAVLL	Address Setup to ALE	53	_	- TCLCL-30	_	
TLLAX1	Address Hold After ALE	48		TCLCL-35		
TLLIV	ALE to Valid Instr In	-	233	_	4TCLCL-100	
TLLPL	ALE to PSEN	58		TCLCL-25		ns
TPLPH	PSEN Pulse Width	215	_	3TCLCL-35	7-	
TPLIV	PSEN to Valid Instr In	-	150	_	3TCLCL-100	
TPXIX	Input Instr Hold After PSEN	0	_	0	-	
TPXIZ*)	Input Instr Float After PSEN	-	63	_	TCLCL-20	
TPXAV*)	Address Valid After PSEN	75	_	TCLCL-8	_	
TAVIV	Address to Valid Instr In	-	302	_	5TCLCL-115	
TAZPL	Address Float to PSEN	0	-	0	_	

External Data Memory Characteristics

Symbol	Parameter		Limit Values				
		12 N	ИНz Clock	Variable Clock 1/TCLCL = 1.2 MHz to 12 MHz			
		Min	Max	Min	Max		
TRLRH	RD Pulse Width	400		6TCLCL-100			
TWLWH	WR Pulse Width	400		OTCLCL-100			
TLLAX 2	Address Hold After ALE	132		2TCLCL-35			
TRLDV	RD to Valid Data In	-	250	-	5TCLCL-165		
TRHDX	Data Hold After RD	0	_	0	_		
TRHDZ	Data Float After RD		97		2TCLCL-70		
TLLDV	ALE to Valid Data In	-	517]-	8TCLCL-150	ns	
TAVDV	Address to Valid Data In		585		9TCLCL-165]	
TLLWL	ALE to WR or RD	200	300	3TCLCL-50	3TCLCL+50		
TAVWL	Address to WR or RD	203	-	4TCLCL-130	_		
TWHLH	WR or RD High to ALE High	43	123	TCLCL-40	TCLCL+40		
TDVWX	Data Valid to WR Transition	33		TCLCL-50			
TQVWH	Data Setup Before WR	433	_	7TCLCL-150]_		
TWHQX	Data Hold After WR	33		TCLCL-50			
TRLAZ	Address Float After RD	_	0	_	0		

^{*)} Interfacing the SAB 8051A to devices with float times up to 75ns is permissible. This limited bus contention will not cause any damage to Port 0 drivers.

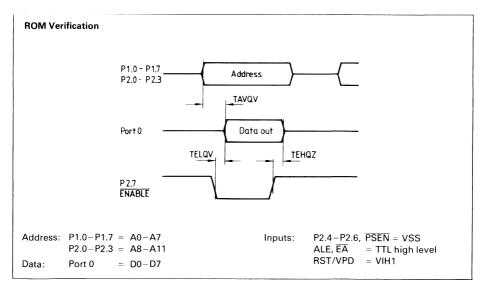
External Clock Drive XTAL2

Symbol	Parameter		Limit Values	
			ariable Clock 1.2 MHz to 12 MHz	
		Min	Max	1
TCLCL	Oscillator Period	83.3	833.3	
тснсх	High Time	20	TCLCL-TCLCX	
TCLCK	Low Time	20	TCLCL-TCHCX	ns
TCLCH	Rise Time		20	
TCHCL	Fall Time		20	

ROM Verification Characteristics for SAB 8051A

 $TA=25^{\circ}C~\pm5^{\circ}C;~VCC=5~V~\pm10\%;~VSS=0~V$

Symbol	Parameter		Limit Values	
		Min	Max	
TAVQV	Address to Valid Data			
TELQV	Enable to Valid Data		48 TCLCL	ns
TEHQZ	Data Float after Enable	0		
1/TCLCL	Oscillator Frequency	4	6	MHz



A.C. Characteristics for SAB 8031A-15/8051A-15

TA 0 to 70°C; VCC = 5 V $\pm 10\%$; VSS = 0 V

(CL for Port 0, ALE and $\overline{\text{PSEN}}$ Outputs = 100 pF; CL for All Other Outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter			Limit Values		Unit
		15 N	ЛНz Clock		ble Clock .2 MHz to 15 MHz	
		Min	Max	Min	Max	
TLHLL	ALE Pulse Width	93		2TCLCL-40		
TAVLL	Address Setup to ALE	37	_	TCLCL-30	_	
TLLAX1	Address Hold After ALE	32		TCLCL-35		
TLLIV	ALE to Valid Instr In	_	167	_	4TCLCL-100	
TLLPL	ALE to PSEN	42		TCLCL-25		ns
TPLPH	PSEN Pulse Width	165		3TCLCL-35		
TPLIV	PSEN to Valid Instr In	_	100	_	3TCLCL-100	
TPXIX	Input Instr Hold After PSEN	0	-	0	-	
TPXIZ*)	Input Instr Float After PSEN	-	52	_	TCLCL-15	
TPXAV*)	Address Valid After PSEN	64	_	TCLCL-3	_	
TAVIV	Address to Valid Instr In	-	243	-	5TCLCL-90	
TAZPL	Address Float to PSEN	0	-	0	-	

External Data Memory Characteristics

Symbol	Parameter			Limit Values		Unit
		15 N	ИНz Clock		Variable Clock 1/TCLCL = 1.2 MHz to 15 MHz	
		Min	Max	Min	Max	
TRLRH	RD Pulse Width	300		6TCLCL-100		
TWLWH	WR Pulse Width	300	_	OTCECE-100	_	
TLLAX 2	Address Hold After ALE	98		2TCLCL-35		
TRLDV	RD to Valid Data In	-	168	-	5TCLCL-165	
TRHDX	Data Hold After RD	0	-	0	_	
TRHDZ	Data Float After RD		63		2TCLCL-70	
TLLDV	ALE to Valid Data In	_	383	_	8TCLCL-150	ns
TAVDV	Address to Valid Data In		435		9TCLCL-165	
TLLWL	ALE to WR or RD	150	250	3TCLCL-50	3TCLCL+50	
TAVWL	Address to WR or RD	137	-	4TCLCL-130	_	
TWHLH	WR or RD High to ALE High	27	107	TCLCL-40	TCLCL+40	
TDVWX	Data Valid to WR Transition	17		TCLCL-50		
TQVWH	Data Setup Before WR	317	-	7TCLCL-150	_	
TWHQX	Data Hold After WR	17		TCLCL-50		
TRLAZ	Address Float After RD		0		0	

^{*)} Interfacing the SAB 8051A-15 to devices with float times up to 60ns is permissible. This limited bus contention will not cause any damage to Port 0 drivers.

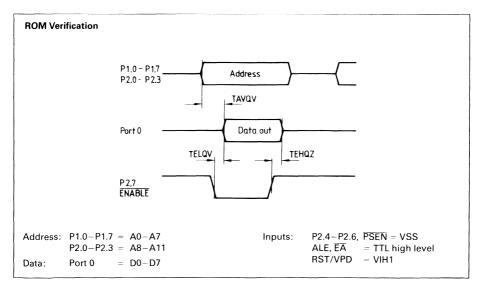
External Clock Drive XTAL2

Symbol	Parameter		Limit Values Variable Clock Freq = 1.2 MHz to 15 MHz	
	Min	Max		
TCLCL	Oscillator Period	66.6	833.3	
TCHCX	High Time	15	TCLCL-TCLCX	
TCLCK	Low Time	13	TCLCL-TCHCX	ns
TCLCH	Rise Time		15	
TCHCL	Fall Time		1.0	

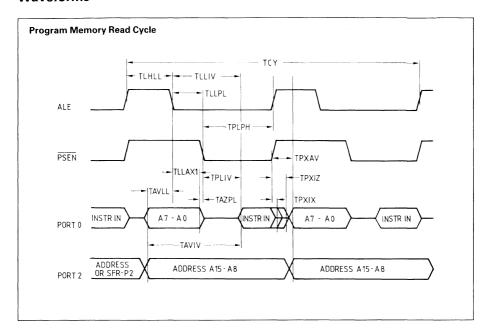
ROM Verification Characteristics for SAB 8051A-15

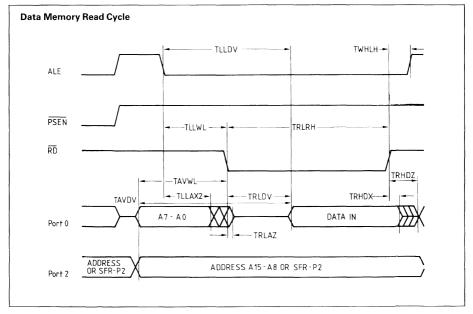
 $TA = 25^{\circ}C \pm 5^{\circ}C$; $VCC = 5V \pm 10\%$; VSS = 0V

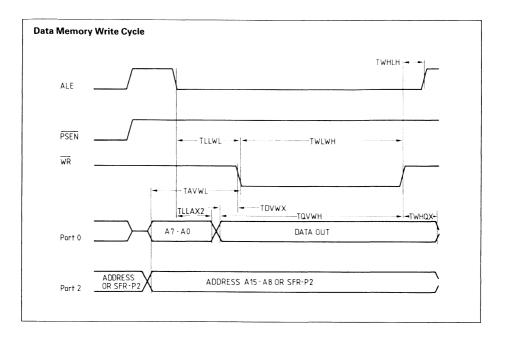
Symbol	Parameter		Limit Values	Unit
		Min	Max	
TAVQV	Address to Valid Data			
TELQV	Enable to Valid Data		48 TCLCL	ns
TEHQZ	Data Float after Enable	0		
1/TCLCL	Oscillator Frequency	4	6	MHz



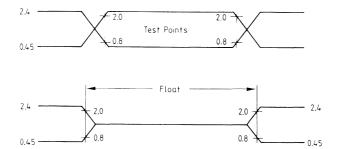
Waveforms



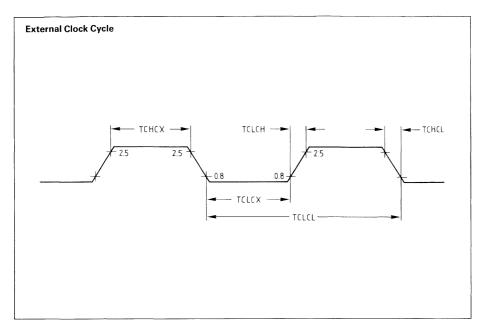


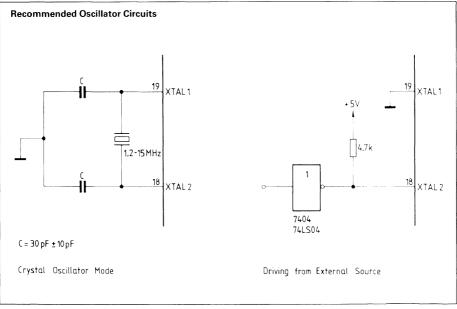


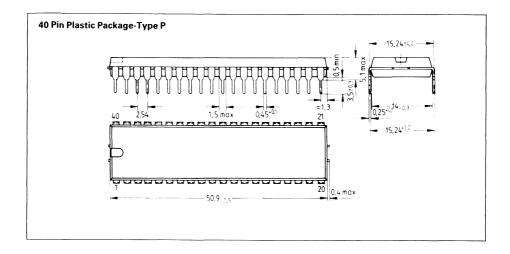




A.C. testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0". For timing purposes, the float state is defined as the point at which a P0 pin sinks 3.2mA or sources $400\,\mu\text{A}$ at the voltage test levels.







SAB 8031A/8051A

Ordering Information

Туре	Description	Ordering code
	8-Bit Single-Chip-Microcomputer	
SAB 8031A-P	for external Memory (Plastic)	Q 67120-C183
SAB 8051A-P	with mask-programmable ROM (Plastic)	Q 67120-C186
SAB 8031A-15-P	for external Memory (Plastic)	Q 67120-C189
SAB 8051A-15-P	with mask-programmable ROM (Plastic)	Q 67120-C214

Preliminary

SAB 8031A/8051A Ext. Temp. 8-Bit Single-Chip Microcontroller

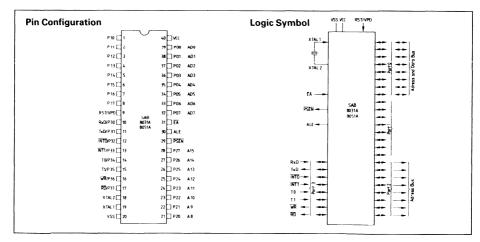
Extended Temperature Range: -40 to + 85°C -40 to +110°C

SAB 8051A-12-P-T40/85 Mask Programmable ROM SAB 8051A-10-P-T40/110

- Advanced Version of the SAB 8031/8051 for Extended Temperature Range
- SAB 8031A/8051A-12-T40/85:
 12 MHz Operation
- SAB 8031A/8051A-10-T40/110:
 10 MHz Operation
- 4K × 8 ROM
- 128 × 8 RAM
- Four 8-bit Ports, 32 I/O Lines

SAB 8031A-12-P-T40/85 External ROM SAB 8031A-10-P-T40/110

- Two 16-bit Timer/Event Counters
- High-Performance Full-Duplex Serial Channel
- External Memory Expandable up to 128K
- Compatible with SAB 8080/8085 Peripherals
- Boolean Processor
- 218 User bit-Addressable Locations
- Most Instructions Execute in 1 us
- 4 us Multiply and Divide



The SAB 8031A/8051A for the two extended temperature ranges (Industrial temperature range: -40 to $+85^{\circ}\text{C}$, Automotive temperature range: -40 to $+110^{\circ}\text{C}$) is fully compatible with the standard SAB 8031A/8051A with respect to architecture, instruction set, and software portability.

The SAB 8031A/8051A is a stand-alone, high-performance single-chip computer fabricated in +5V advanced N-channel, silicon gate Siemens MYMOS technology and packaged in a 40-pin DIP. The SAB 8051A contains a non-volatile 4K × 8 read-only program memory; a volatile 128 × 8 read/write

data memory; 32 I/O lines; two 16-bit timer/counters; a five-source, two-priority-level, nested interrupt structure; a serial I/O port for either multiprocessor communications, I/O expansion, or full duplex UART; and on-chip oscillator and clock circuits. The SAB 8031A is identical, except that it lacks the program memory.

For systems that require extra capability, the SAB 8051A can be expanded using standard TTL compatible memories and the byte oriented SAB 8080 and SAB 8085 peripherals.

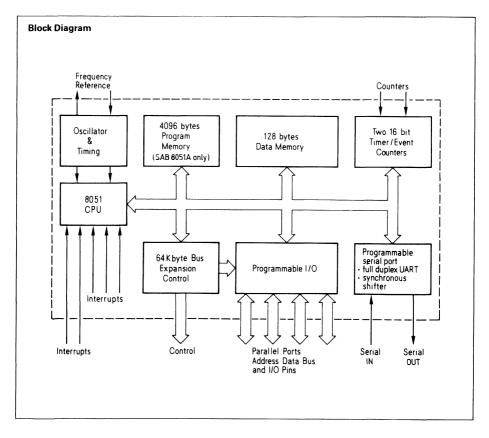
2.85

Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Functions
P1.0-P1.7	1-8	I/O	Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification.
RST/VPD	9	I	A high level on this pin resets the SAB 8051A. A small internal pulldown resistor permits power-on reset using only a capacitor connected to VCC. If VPD is held within its spec while VCC drops below spec, VPD will provide standby power to the RAM. When VPD is low, the RAM's current is drawn from VCC.
P3.0 – P3.7	10-17	1/0	Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and RD and WR pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of Port 3, as follows: RXD/data (P3.0). Serial port's receiver data input (asynchronous) or data input/output (synchronous). TXD/clock (P3.1). Serial port's transmitter data output (asynchronous) or clock output (synchronous). INTO (P3.2). Interrupt 0 input or gate control input for counter 0. INT1 (P3.3). Interrupt 1 input or gate control input for counter 1. TO (P3.4). Input to counter 0. T1 (P3.5). Input to counter 0. T1 (P3.5). Input to counter 1. WR (P3.6). The write control signal latches the data byte from Port 0 into the External Data Memory. RD (P3.7). The read control signal enables External Data Memory to Port 0.
XTAL1 XTAL2	19 18	1	XTAL 1 Input to the oscillator's high gain amplifier. Required when a crystal is used. Connect to VSS when external source is used on XTAL2. XTAL2 Output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal or external source can be used.
P2.0 – P2.7	21-28	I/O	Port 2 is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification.
PSEN	29	0	The Program Store Enable output is a control signal that enables the external Program Memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.
ALE	30	0	Provides Address Latch Enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.

Pin Definitions and Functions (continued)

Symbol	Number	Input (I) Output (O)	Function
ĒĀ	31	1	When held at a high level, the SAB 8051A executes instructions from the internal ROM when the PC is less than 4096. When held at a low level, the SAB 8051A fetches all instructions from external Program Memory. For the SAB 8031A this pin must be tied low.
PØ.Ø-PØ.7	39-32	I/O	Port 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification.
VCC	40		+5V power supply during operation and program verification.
VSS	20		Circuit ground potential.



Instruction Set Description

Mnemonic		Description	Byte	Cycle
Arithmetic ope	rations			
ADD	A, Rn	Add register to Accumulator	1	1
ADD	A, direct	Add direct byte to Accumulator	2	1
ADD	A, @Ri	Add indirect RAM to Accumulator	1	1
ADD	A,#data	Add immediate data to Accumulator	2	1
ADDC	A,Rn	Add register to Accumulator with Carry flag	1	1
ADDC	A,direct	Add direct byte to A with Carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with Carry flag	1	1
ADDC	A,#data	Add immediate data to A with Carry flag	2	1
SUBB	A,Rn	Subtract register from A with Borrow	1	1
SUBB	A,direct	Subtract direct byte from A with Borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A w/Borrow	1	1
SUBB	A,#data	Subtract immediate data from A w/Borrow	2	1
INC	Α	Increment Accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	Α	Decrement Accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment Data Pointer	1	2
MUL	AB	Multiply A & B	1	4
DIV	AB	Divide A & B	1	4
DA	А	Decimal Adjust Accumulator	1	1
Logical operati	ions			
ANL	A,Rn	AND register to Accumulator	1	1
ANL	A,direct	AND direct byte to Accumulator	2	1
ANL	A,@Ri	AND indirect RAM to Accumulator	1	1
ANL	A,#data	AND immediate data to Accumulator	2	1
ANL	direct,A	AND Accumulator to direct byte	2	1

Mnemonic		Description	Byte	Cycle
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to Accumulator	1	1
ORL	A,direct	OR direct byte to Accumulator	2	1
ORL	A,@Ri	OR indirect RAM to Accumulator	1	1
ORL	A,#data	OR immediate data to Accumulator	2	1
ORL	direct,A	OR Accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive-OR register to Accumulator	1	1
XRL	A,direct	Exclusive-OR direct byte to Accumulator	2	1
XRL	A,@Ri	Exclusive-OR indirect RAM to A	1	1
XRL	A,#data	Exclusive-OR immediate data to A	2	1
XRL	direct,A	Exclusive-OR Accumulator to direct byte	2	1
XRL	direct,#data	Exclusive-OR immediate data to direct	3	2
CLR	Α	Clear Accumulator	1	1
CPL	Α	Complement Accumulator	1	1
RL	А	Rotate Accumulator Left	1	1
RLC	А	Rotate A Left through the Carry flag	1	1
RR	Α	Rotate Accumulator Right	1	1
RRC	А	Rotate A Right through Carry flag	1	1
SWAP	Α	Swap nibbles within the Accumulator	1	1

Data transfer

MOV	A,Rn	Move register to Accumulator	1	1
MOV	A,direct *)	Move direct byte to Accumulator	2	1
MOV	A,@Ri	Move indirect RAM to Accumulator	1	1
MOV	A,#data	Move immediate data to Accumulator	2	1
MOV	Rn,A	Move Accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move Accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct	3	2

^{*)} MOV A, ACC is not a valid instruction

Mnemonic		Description	Byte	Cycle
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move Accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load Data Pointer with a 16-bit constant	3	2
Data transfer (c	ont.)			
MOVC	A,@A+DPTR	Move Code byte relative to DPTR to A	1	2
MOVC	A,@A+PC	Move Code byte relative to PC to A	1	2
MOVX	A,@Ri	Move External RAM (8-bit addr) to A	1	2
MOVX	A,@DPTR	Move External RAM (16-bit addr) to A	1	2
MOVX	@Ri,A	Move A to External RAM (8-bit addr)	1	2
MOVX	@DPTR,A	Move A to External RAM (16-bit addr)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with Accumulator	1	1
XCH	A,direct	Exchange direct byte with Accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with A	1	1
XCHD	A,@Ri	Exchange low-order Digit ind. RAM w/A	1	1
Boolean variab	le manipulation			
CLR	С	Clear Carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	С	Set Carry flag	1	1
SETB	bit	Set direct Bit	2	1
CPL	С	Complement Carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to Carry flag	2	2
ANL	C,/bit	AND complement of direct bit to Carry	2	2
ORL	C,bit	OR direct bit to Carry flag	2	2
ORL	C,/bit	OR complement of direct bit to Carry	2	2
MOV	C,bit	Move direct bit to Carry flag	2	1
MOV	bit,C	Move Carry flag to direct bit	2	2

Mnemonic		Description	Byte	Cycle
Program and n	nachine control			
ACALL	addr 11	Absolute Subroutine Call	2	2
LCALL	addr 16	Long Subroutine Call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute Jump	2	2
LJMP	addr 16	Long Jump	3	2
SJMP	rel	Short Jump (relative addr)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if Accumulator is Zero	2	2
JNZ	rel	Jump if Accumulator is Not Zero	2	2
JC	rel	Jump if Carry flag is set	2	2
JNC	rel	Jump if Carry flag not set	2	2
JB	bit,rel	Jump if direct Bit set	3	2
JNB	bit,rel	Jump if direct Bit not set	3	2
JBC	bit,rel	Jump if direct Bit is set & Clear bit	3	2
CJNE	A,direct,rel	Compare direct to A & Jump if Not Equal	3	2
CJNE	A,#data,rel	Comp. immed. to A & Jump if Not Equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. & Jump if Not Equal	3	2
CJNE	@Ri,#data,rel	Comp.immed. to ind. & Jump if Not Equal	3	2
DJNZ	Rn,rel	Decrement register & Jump if Not Zero	2	2
DJNZ	direct,rel	Decrement direct & Jump if Not Zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn

Working register R0–R7

direct - 128 internal RAM locations, any I/O port, control or status register

@Ri — Indirect internal RAM location addressed by register R0 or R1

#data - 8-bit constant included in instruction

#data 16 - 16-bit constant included as bytes 2 & 3 of instruction

bit – 128 software flags, any I/O pin, control or status bit

Notes on program addressing modes:

addr 16 — Destination address for LCALL & LJMP may be anywhere within the 64-Kilobyte

program memory address space.

addr 11 – Destination address for ACALL & AJMP will be within the same 2-Kilobyte page of program memory as the first byte of the following instruction.

rel — SJMP and all conditional jumps include an 8-bit offset byte. Range is +127/-128 bytes relative to first byte of the following instruction.

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Instruction Opcodes in Hexadecimal Order

Hex	Number			Hex	Number		
Code	of Bytes	Mnemonic	Operands	Code	of Bytes	Mnemonic	Operands
00	1	NOP		34	2	ADDC	A,#data
01	2	AJMP	code addr	35	2	ADDC	A,data addr
02	3	LJMP	code addr	36	1	ADDC	A,@R0
03	1	RR	Α	37	1	ADDC	A,@R1
04	li	INC	A	38	1	ADDC	A,R0
05	2	INC	data addr	39	1	ADDC	A,R1
06	1	INC	@R0	3A	1	ADDC	A,R2
07	1	INC	@R1	3B	1	ADDC	A,R3
08	l i	INC	R0	3C	1	ADDC	A,R4
09	1	INC	R1	3D	1	ADDC	A,R5
0A	1	INC	R2	3E	1	ADDC	A,R7
0B	1	INC	R3	3F	1	ADDC	A,R7
OC	1	INC	R4	40	2	JC	code addr
0D	1	INC	R5	41	2	AJMP	code addr
0E	1	INC	R6	42	2	ORL	data addr,A
0E 0F	1	INC	R7	43	3	ORL	data addr,#data
0F 10	3	JBC	bit addr code addr	44	2	ORL	A,#data
			code addr	45	2	ORL	A.data addr
11	2	ACALL		46	1	ORL	A,@R0
12	3	LCALL	code addr	47	1	ORL	A,@R1
13	1	RRC	A	47	1	ORL	A,R0
14	1	DEC	1	48 49	1	ORL	A,R0 A,R1
15	2	DEC	data addr	49 4A	1	ORL	A,R2
16	1	DEC	@R0	4A 4B	1	ORL	A,R3
17	1	DEC	@R1		1	ORL	A,R4
18	1	DEC	R0	4C	1	ORL	A,R4 A,R5
19	1	DEC	R1	4D	1 '	ORL	A,R6
1A	1	DEC	R2	4E	1	ORL	A,R7
1B	1	DEC	R3	4F		1	1 '
1C	1	DEC	R4	50	2	JNC ACALL	code addr code addr
1D	1	DEC	R5	51	2		
1E	1	DEC	R6	52	2	ANL	data addr,A
1F	1	DEC	R7	53	3	ANL	data addr, #data
20	3	JB	bit addr code addr	54	2	ANL	A,#data
21	2	AJMP	code addr	55	2	ANL	A,data addr
22	1	RET		56	1	ANL	A,@R0
23	1	RL	А	57	1	ANL	A,@R1
24	2	ADD	A,#data	58	1	ANL	A,R0
25	2	ADD	A,data addr	59	1	ANL	A,R1
26	1	ADD	A,@R0	5A	1	ANL	A,R2
27	1	ADD	A,@R1	5B	1	ANL	A,R3
28	1	ADD	A,R0	5C	1	ANL	A,R4
29	1	ADD	A,R1	5D	1	ANL	A,R5
2A	1	ADD	A,R2	5E	1	ANL	A,R6
2B	1	ADD	A,R3	5F	1	ANL	A,R7
2C	1	ADD	A,R4	60	2	JZ	code addr
2D	1	ADD	A,R5	61	2	AJMP	code addr
2E	1	ADD	A,R6	62	2	XRL	data addr, A
2F	1	ADD	A,R7	63	3	XRL	data addr,#data
30	3	JNB	bit addr, code addr	64	2	XRL	A,#data
31	2	ACALL	code addr	65	2	XRL	A,data addr
32	1	RETI		66	1	XRL	A,@R0
33	1	RLC	Α	67	1	XRL	A,@R1

Instruction Opcodes in Hexadecimal Order (continued)

Hex Code	Number of Bytes	Mnemonic	Operands	Hex Code	Number of Bytes	Mnemonic	Operands
68	1	XRL	A.R0	9C	1	SUBB	A,R4
69	1	XRL	A,R1	9D	1	SUBB	A,R5
6A	1	XRL	A,R2	9E	1	SUBB	A,R6
6B	1	XRL	A,R3	9F	1	SUBB	A,R7
6C	1	XRL	A,R4	A0	2	ORL	C./bit addr
6D	1	XRL	A,R5	A1	2	AJMP	code addr
6E	1	XRL	A,R6	A2	2	MOV	C,bit addr
6F	1	XRL	A,R7	A3	1	INC	DPTR
70	2	JNZ	code addr	A4	1	MUL	AB
71	2	ACALL	code addr	A5	·	reserved	
72	2	ORL	C,bit addr	A6	2	MOV	@R0,data addr
73	1	JMP	@A+DPTR	A7	2	MOV	@R1,data addr
74	2	MOV	A,#data	A8-	2	MOV	R0,data addr
75	3	MOV	data addr,#data	Α9	2	MOV	R1,data addr
76	2	MOV	@R0,#data	AA	2	MOV	R2,data addr
77	2	MOV	@R1,#data	AB	2	MOV	R3,data addr
78	2	MOV	R0,#data	AC	2	MOV	R4,data addr
79	2	MOV	R1,#data	AD	2	MOV	R5,data addr
7A	2	MOV	R2,#data	AE	2	MOV	R6,data addr
7B	2	MOV	R3,#data	AF	2	MOV	R7,data addr
7C	2	MOV	R4,#data	В0	2	ANL	C,/bit addr
7D	2	MOV	R5,#data	B1	2	ACALL	code addr
7E	2	MOV	R6,#data	B2	2	CPL	bit addr
7F	2	MOV	R7,#data	B3	1	CPL	C
80	2	SJMP	code addr	B4	3	CJNE	A,#data.code addr
81	2	AJMP	code addr	B5	3	CJNE	A.data addr.code addr
82	2	ANL	C,bit addr	B6	3	CJNE	@R0,#data,code addr
83	1	MOVC	A,@A+PC	B7	3	CJNE	@R1,#data,code addr
84	1	DIV	AB	B8	3	CJNE	R0,#data,code addr
85	3	MOV	data addr,data addr	B9	3	CJNE	R1,#data,code addr
86	2	MOV	data addr,@R0	BA	3	CJNE	R2,#data,code addr
87	2	MOV	data addr,@R1	BB	3	CJNE	R3,#data,code addr
88	2	MOV	data addr.R0	BC	3	CJNE	R4,#data,code addr
89	2	MOV	data addr,R1	BD	3	CJNE	R5,#data,code addr
8A	2	MOV	data addr, R2	BE	3	CJNE	R6,#data,code addr
8B	2	MOV	data addr. R3	BF	3	CJNE	R7,#data,code addr
8C	2	MOV	data addr,R4	C0	2	PUSH	data addr
8D	2	MOV	data addr,R5	C1	2	AJMP	code addr
8E	2	MOV	data addr,R6	C2	2	CLR	bit addr
8F	2	MOV	data addr,R7	C3	1	CLR	C
90	3	MOV	DPTR,#data	C4	i	SWAP	A
91	2	ACALL	code addr	C5	2	XCH	A,data addr
92	2	MOV	bit addr,C	C6	1	XCH	A,@R0
93	1	MOVC	A,@A+DPTR	C7	1	XCH	A,@R1
94	2	SUBB	A,#data	C8	1	XCH	A,R0
95	2	SUBB	A,data addr	C9	1	XCH	A,R1
96	1	SUBB	A,@R0	CA	1	XCH	A,R2
97	1	SUBB	A,@R1	CB	1	XCH	A,R3
98	1	SUBB	A,R0	CC	1	XCH	A,R4
99	1	SUBB	A,R1	CD	1	XCH	A,R5
9A	1	SUBB	A,R2	CE	1	XCH	A,R6
9B	1	SUBB	A,R3	CF	1	XCH	A,R7
30	1	3000	A,110	CI.	1	ACH	A,117

Instruction Opcodes in Hexadecimal Order (continued)

		-	
Hex Code	Number of Bytes	Mnemonic	Operands
D0	2	POP	data addr
D1	2	ACALL	code addr
D2	2	SETB	bit addr
D3	1	SETB	С
D4	1	DA	A
D5	3	DJNZ	data addr,code addr
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,code addr
D9	2	DJNZ	R1,code addr
DA	2	DJNZ	R2,code addr
DB	2	DJNZ	R3,code addr
DC	2	DJNZ	R4,code addr
DD	2	DJNZ	R5,code addr
DE	2	DJNZ	R6,code addr
DF	2	DJNZ	R7,code addr
E0	1	MOVX	A,@DPTR
E1	2	AJMP	code addr
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,data addr *)
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	code addr
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	data addr,A
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

^{*)} MOV A,ACC is not a valid instruction

Absolute Maximum Ratings¹⁾

Ambient Temperature Under Bias -40 to + 85°C for T40/85 -40 to +110°C for T40/110

Storage Temperature $$-65\ \text{to} + 150^{\circ}\text{C}$$ Voltage on Any Pin with Respect to Ground (VSS) $-0.5\ \text{to} + 7\ \text{V}$ Power Dissipation $2\ \text{W}$

D.C. Characteristics

VCC = 5 V \pm 10%; VSS = 0 V TA = -40 to + 85°C for T40/85; TA = -40 to +110°C for T40/110

Symbol	Parameter	Limit	Limit Values		Test Conditions	
		Min.	Max.	1		
VIL	Input Low Voltage	-0.5	0.8			
VIH	Input High Voltage except RST/VPD and XTAL2	2.0			_	
VIH1	Input High Voltage to RST/VPD for Reset, XTAL2	2.5	VCC+0.5		XTAL 1 to VSS	
VPD	Power Down Voltage To RST/VPD	4.5	5.5	v	VCC = 0 V	
VOL	Output Low Voltage Ports 1, 2, 3		0.45		IOL = 1.6 mA	
VOL1	Output Low Voltage Port 0, ALE, /PSEN		0.45		IOL = 3.2 mA	
VOH	Output High Voltage Ports 1, 2, 3	2.4	_		IOH = -80 µA	
VOH1	Output High Voltage Port 0, ALE, /PSEN	72.4			IOH = -400 μA	
IIL	Logical 0 Input Current Ports 1, 2, 3		-800	μ A	VIL = 0.45 V	
IIL2	Logical 0 Input Current XTAL2		-2.5	mA	XTAL1 = VSS VIL = 0.45 V	
IIH1	Input High Current to RST/VPD for Reset		500	uА	VIN = VCC - 1.5 V	
ILI	Input Leakage Current to Port 0,/EA		±10	,,,	0 < VIN < VCC	
ICC	Power Supply Current		150	mA		
IPD	Power Down Current		15	<u>'</u>		
CIO	Capacitance of I/O Buffer		10	pF	fc = 1 MHz	

¹⁾ Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

A.C. Characteristics for T40/85

VCC = $5 V \pm 10\%$; VSS = 0 V; TA = $-40 \text{ to } +85^{\circ}\text{C}$

(CL for Port 0, ALE and PSEN Outputs = 100 pF; CL for All Other Outputs = 80 pF)

Program Memory Characteristics

Symbol Pa	Parameter		Limit Values				
		12	12 MHz Clock		Variable Clock 1/TCLCL = 1.2 MHz to 12 MHz		
		Min	Max	Min	Max		
TLHLL	ALE Pulse Width	127		2TCLCL-40			
TAVLL	Address Setup to ALE	53	_	TCLCL-30			
TLLAX1	Address Hold After ALE	48		TCLCL-35			
TLLIV	ALE To Valid Instr In	-	233	_	4TCLCL-100		
TLLPL	ALE TO PSEN	58		TCLCL-25		ns	
TPLPH	PSEN Pulse Width	215	7-	3TCLCL-35	_		
TPLIV	PSEN To Valid Instr In	_	150	_	3TCLCL-100		
TPXIX	Input Instr Hold After PSEN	0	_	0	_		
TPXIZ*)	Input Instr Float After PSEN	-	63	_	TCLCL-20		
TPXAV*)	Address Valid After PSEN	75	-	TCLCL-8	_		
TAVIV	Address To Valid Instr In	-	302	_	5TCLCL-115		
TAZPL	Address Float To PSEN	0	_	0	_		

External Data Memory Characteristics

Symbol	Parameter			Limit Values		Unit
		12 M	ИНz Clock		ble Clock 2 MHz to 12 MHz	
		Min	Max	Min	Max	
TRLRH	RD Pulse Width	400		6TCLCL-100		
TWLWH	WR Pulse Width	400	-	6TCLCL-100	_	
TLLAX 2	Address Hold After ALE	132		2TCLCL-35		
TRLDV	RD To Valid Data In	-	250	_	5TCLCL-165	
TRHDX	Data Hold After RD	0	_	0	_	
TRHDZ	Data Float After RD		97		2TCLCL-70	
TLLDV	ALE To Valid Data In	_	517]-	8TCLCL-150	ns
TAVDV	Address To Valid Data In		585		9TCLCL-165	
TLLWL	ALE To WR or RD	200	300	3TCLCL-50	3TCLCL+50	
TAVWL	Address To WR or RD	203	-	4TCLCL-130	_	
TWHLH	WR or RD High To ALE High	43	123	TCLCL-40	TCLCL+40	
TDVWX	Data Valid To WR Transition	33		TCLCL-50		
TQVWH	Data Setup Before WR	433	_	7TCLCL-150]-	
TWHQX	Data Hold After WR	33		TCLCL-50		
TRLAZ	Address Float After RD	-	0	_	0	

^{*)} Interfacing the SAB 8051A to devices with float times up to 75ns is permissible. This limited bus contention will not cause any damage to Port 0 drivers.

A.C. Characteristics for T40/110

VCC = $5V \pm 10\%$; VSS = 0V; TA = $-40 \text{ to } + 110^{\circ}\text{C}$

(CL for Port 0, ALE and PSEN Outputs = 100 pF; CL for All Other Outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter			Limit Values		Unit
		10	MHz Clock	Variable Clock 1/TCLCL = 1.2 MHz to 10 MHz		
		Min	Max	Min	Max	
TLHLL	ALE Pulse Width	160		2TCLCL-40		
TAVLL	Address Setup to ALE	70	_	TCLCL-30	_	
TLLAX1	Address Hold After ALE	65		TCLCL-35		
TLLIV	ALE To Valid Instr In	-	300	_	4TCLCL-100	
TLLPL	ALE TO PSEN	75		TCLCL-25		ns
TPLPH	PSEN Pulse Width	265		3TCLCL-35		
TPLIV	PSEN To Valid Instr In	-	200	-	3TCLCL-100	
TPXIX	Input Instr Hold After PSEN	0	-	0	_	
TPXIZ*)	Input Instr Float After PSEN	_	80	_	TCLCL-20	
TPXAV*)	Address Valid After PSEN	92	_	TCLCL-8	_	
TAVIV	Address To Valid Instr In	-	385	_	5TCLCL-115	
TAZPL	Address Float To PSEN	0	_	0	_	

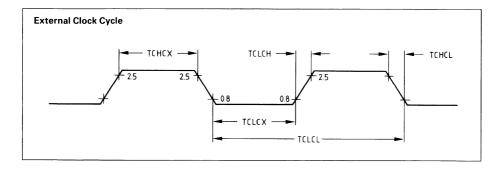
External Data Memory Characteristics

Symbol	Parameter		Limit Values				
		10 (MHz Clock	Variable Clock 1/TCLCL = 1.2 MHz to 10 MHz			
		Min	Max	Min	Max		
TRLRH	RD Pulse Width	500		6TCLCL-100			
TWLWH	WR Pulse Width	500	_	6TCLCL-100]_		
TLLAX 2	Address Hold After ALE	165		2TCLCL-35			
TRLDV	RD To Valid Data In	_	335		5TCLCL-165		
TRHDX	Data Hold After RD	0	_	0	_		
TRHDZ	Data Float After RD		130		2TCLCL-70		
TLLDV	ALE To Valid Data In	_	650	_	8TCLCL-150	ns	
TAVDV	Address To Valid Data In		735		9TCLCL-165		
TLLWL	ALE To WR or RD	250	350	3TCLCL-50	3TCLCL+50		
TAVWL	Address To WR or RD	270	_	4TCLCL-130	_		
TWHLH	WR or RD High To ALE High	60	140	TCLCL-40	TCLCL+40		
TDVWX	Data Valid To WR Transition	50		TCLCL-50			
TQVWH	Data Setup Before WR	550	_	7TCLCL-150]-		
TWHQX	Data Hold After WR	50		TCLCL-50			
TRLAZ	Address Float After RD	_	0	-	0		

^{*)} Interfacing the SAB 8051A to devices with float times up to 92ns is permissible. This limited bus contention will not cause any damage to Port 0 drivers.

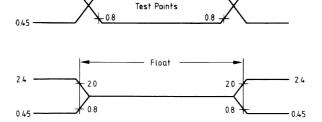
External Clock Drive XTAL2

Symbol	Parameter	Limit Values			
			Variable Clock .2 MHz to 12 MHz (T40/85) .2 MHz to 10 MHz (T40/110)		
		Min	Max		
TCLCL	Oscillator Period T40/85 T40/110	83.3 100	833.3		
TCHCX	High Time	20	TCLCL-TCLCX	1	
TCLCX	Low Time		TCLCL-TCHCX	ns	
TCLCH	Rise Time		20		
TCHCL	Fall Time		20		





2.4



2.0

AC testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".

Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

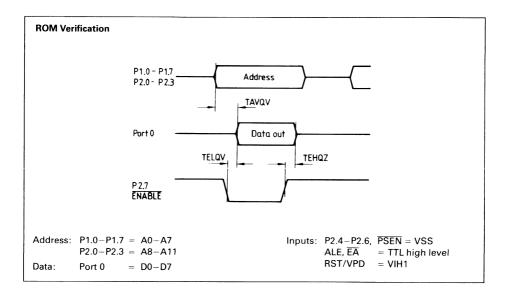
- 2.0

For timing purposes, the float state is defined as the point at which a P0 pin sinks 3.2 mA or sources $400\,\mu\text{A}$ at the voltage test levels.

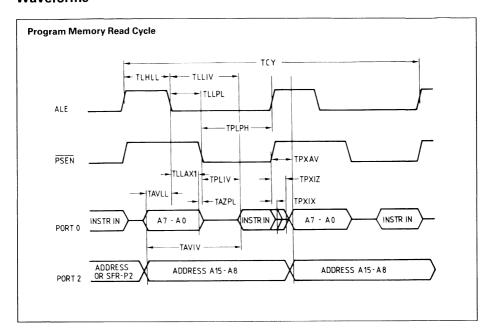
ROM Verification Characteristics —

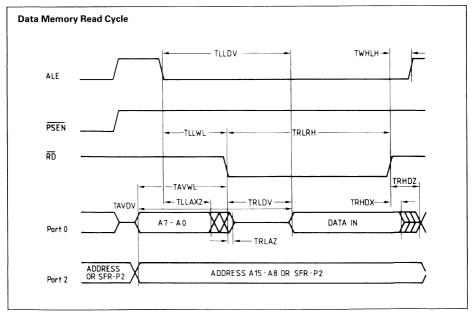
 $TA = 25^{\circ}C \pm 5^{\circ}C$; $VCC = 5V \pm 10\%$; VSS = 0V

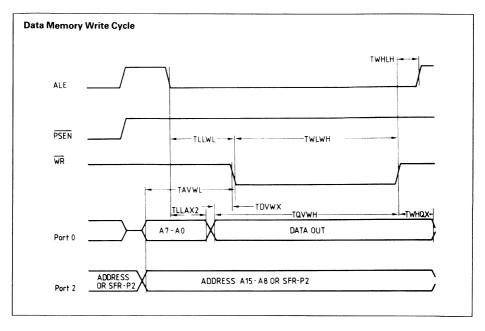
Symbol	Parameter		Unit	
		Min	Max	
TAVQV	Address to Valid Data			
TELQV	Enable to Valid Data	_	48 TCLCL	ns
TEHQZ	Data Float after Enable	0		
1/TCLCL	Oscillator Frequency	4	6	MHz

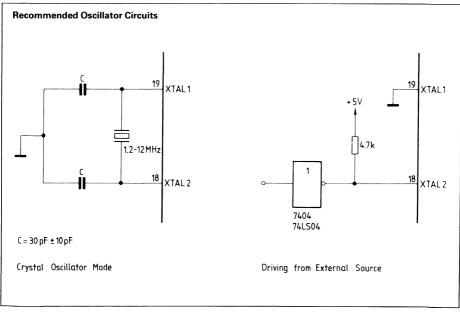


Waveforms

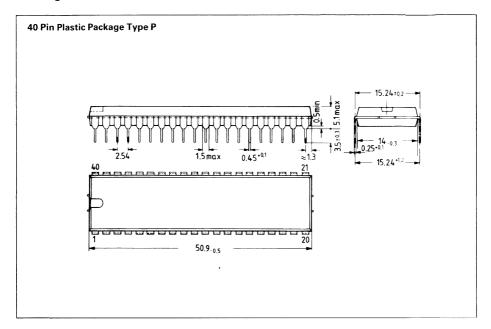








Package Outline



Ordering Information

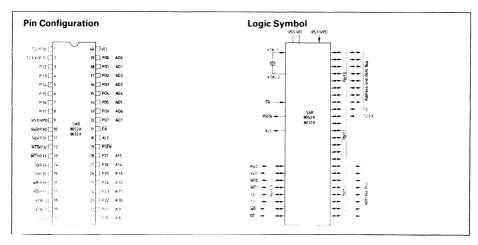
Туре	Description	Ordering Number
The state of the s	8-Bit Single-Chip-Microcomputer	
SAB 8051A-12-P-T40/85	with mask-programmable ROM (Plastic)	Q 67120-C233
SAB 8051A-10-P-T40/110	with mask-programmable ROM (Plastic)	Q 67120-C231
SAB 8031A-12-P-T40/85	for external Memory (Plastic)	Q 67120-C230
SAB 8031A-10-P-T40/110	for external Memory (Plastic)	Q 67120-C232

Preliminary

SAB 8032A/8052A 8-Bit Single-Chip Microcontroller

SAB 8032A Control-oriented CPU with RAM and I/O SAB 8052A A SAB 8032A with factory mask-programmable ROM

- 8K × 8 ROM (SAB 8052A only)
- 256 × 8 RAM
- Four 8-bit ports, 32 I/O lines
- Three 16-bit timer/event counters
- High-performance full-duplex serial channel
- External memory expandable to 128 Kbytes
- Compatible with SAB 8080/8085 peripherals
- Timer 2 capture capability
- Variable transmit/receive baud rate capability
- Boolean processor
- Most instructions execute in 1 µs
- 4 us multiply and divide
- Upward compatible with SAB 8031A/8051A



The SAB 8032A/8052A is a stand-alone, high-performance single-chip microcomputer fabricated in +5V advanced N-channel, silicon gate Siemens MYMOS technology, packaged in a 40-pin DIP. It is upward compatible with the SAB 8031A/8051A. It provides the hardware features, architectural enhancements, and instructions that are necessary to make it a powerful and cost effective controller for applications requiring up to 64 Kbytes of program memory and/or up to 64 Kbytes of data memory.

The SAB 8052A contains a non-volatile 8 K × 8 read-

only program memory; a volatile 256 × 8 read/write data memory; 32 I/O lines; three 16-bit timer/ counters; a six-source, two-priority-level, nested interrupt structure; a serial I/O port for either multiprocessor communications, I/O expansion, or full duplex UART; as well as on-chip oscillator and clock circuits. The SAB 8032A is identical, except that it lacks the program memory.

For systems that require extra capability, the SAB 8052A can be expanded using standard TTL compatible memories and the byte oriented SAB 8080 and SAB 8085 peripherals.

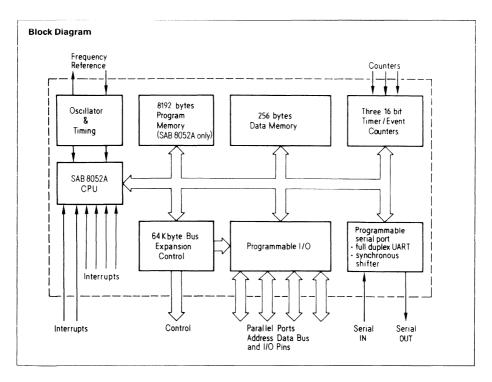
3.85

Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function
P1.0-P1.7	1-8	1/0	Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. Port 1 can sink/source four LS TTL loads. Pins P1.0 and P1.1 also correspond to the special functions T2, external input to Timer 2, and T2EX, Timer 2 trigger input. The output latch on these two special function pins must be programmed to a one (1) for that function to operate.
RST/VPD	9	1	A high level on this pin resets the SAB 8052A. A small internal pulldown resistor permits power-on reset using only a capacitor connected to VCC. If VPD is held within its spec while VCC drops below spec, VPD will provide standby power to the RAM. When VPD is low, the RAM's current is drawn from VCC.
P3.Ø-P3.7	10 – 17	1/0	Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and RD and WR pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source four LS TTL loads. The secondary functions are assigned to the pins of Port 3, as follows: RXD/data (P3.0). Serial port's receiver data input (asynchronous) or data input/output (synchronous). TXD/clock (P3.1). Serial port's transmitter data output (asynchronous) or clock output (synchronous). INTO (P3.2). Interrupt 0 input or gate control input for counter 0. INT1 (P3.3). Interrupt 1 input or gate control input for counter 1. TO (P3.4). Input to counter 0. T1 (P3.5). Input to counter 1. WR (P3.6). The write control signal latches the data byte from port 0 into the external data memory. RD (P3.7). The read control signal enables external data memory to port 0.
XTAL1 XTAL2	19 18	I	XTAL 1 input to the oscillator's high gain amplifier. Required when a crystal is used. Connect to VSS when external source is used on XTAL 2. XTAL 2 output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal or external source can be used.
P2.Ø-P2.7	21-28	I/O	Port 2 is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source four LS TTL loads.
PSEN	29	0	The program store enable output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.

Pin Definitions and Functions (continued)

Symbol	Number	Input (I) Output (O)	Function
ALE	30	0	Provides address latch enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
ĒĀ	31	I	When held at a TTL high level, the SAB 8052A executes instructions from the internal ROM when the PC is less than 8192. When held at a TTL low level, the SAB 8052A fetches all instructions from external program memory. For the SAB 8032A this pin must be tied.low.
P0.0-P0.7	39-32	1/0	Port 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source eight LS TTL loads.
VCC	40		+5V power supply during operation and program verification.
VSS	20		Circuit ground potential.



Instruction Set Description

Mnemonic		Description	Byte	Cycle
Arithmetic ope	erations			
ADD	A, Rn	Add register to Accumulator	1	1
ADD	A, direct	Add direct byte to Accumulator	2	1
ADD	A, @Ri	Add indirect RAM to Accumulator	1	1
ADD	A,#data	Add immediate data to Accumulator	2	1
ADDC	A,Rn	Add register to Accumulator with Carry flag	1	1
ADDC	A,direct	Add direct byte to Accu with Carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to Accu with Carry flag	1	1
ADDC	A,#data	Add immediate data to Accu with Carry flag	2	1 ,
SUBB	A,Rn	Subtract register from Accu with borrow	1	1
SUBB	A,direct	Subtract direct byte from Accu with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	Α	Increment Accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	Α	Decrement Accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A & B	1	4
DIV	АВ	Divide A & B	1	4
DA	А	Decimal adjust Accumulator	1	1
Logical operat	ions			
ANL	A,Rn	AND register to Accumulator	1	1
ANL	A,direct	AND direct byte to Accumulator	2	1
ANL	A,@Ri	AND indirect RAM to Accumulator	1	1
ANL	A,#data	AND immediate data to Accumulator	2	1
ANL	direct,A	AND Accumulator to direct byte	2	1

Mnemonic		Description	Byte	Cycle
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to Accumulator	1	1
ORL	A,direct	OR direct byte to Accumulator	2	1
ORL	A,@Ri	OR indirect RAM to Accumulator	1	1
ORL	A,#data	OR immediate data to Accumulator	2	1
ORL	direct,A	OR Accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive-OR register to Accumulator	1	1
XRL	A,direct	Exclusive-OR direct byte to Accumulator	2	1
XRL	A,@Ri	Exclusive-OR indirect RAM to Accumulator	1	1
XRL	A,#data	Exclusive-OR immediate data to Accumulator	2	1
XRL	direct,A	Exclusive-OR Accumulator to direct byte	2	1
XRL	direct,#data	Exclusive-OR immediate data to direct	3	2
CLR	Α	Clear Accumulator	1	1
CPL	Α	Complement Accumulator	1	1
RL	А	Rotate Accumulator left	1	1
RLC	Α	Rotate A left through the Carry flag	1	1
RR	Α	Rotate Accumulator right	1	1
RRC	А	Rotate A right through Carry flag	1	1
SWAP	А	Swap nibbles within the Accumulator	1	1
		Control Annual Control and Con	1	1

Data transfer

A,Rn	Move register to Accumulator	1	1
A,direct *	Move direct byte to Accumulator	2	1
A,@Ri	Move indirect RAM to Accumulator	1	1
A,#data	Move immediate data to Accumulator	2	1
Rn,A	Move Accumulator to register	1	1
Rn,direct	Move direct byte to register	2	2
Rn,#data	Move immediate data to register		1
direct,A	Move Accumulator to direct byte	2	1
direct,Rn	Move register to direct byte		2
direct,direct	Move direct byte to direct		2
	A,direct * A,@Ri A,#data Rn,A Rn,direct Rn,#data direct,A direct,Rn	A,direct * Move direct byte to Accumulator A,@Ri Move indirect RAM to Accumulator A,#data Move immediate data to Accumulator Rn,A Move Accumulator to register Rn,direct Move direct byte to register Rn,#data Move immediate data to register direct,A Move Accumulator to direct byte direct,Rn Move register to direct byte	A,direct * Move direct byte to Accumulator 2 A,@Ri Move indirect RAM to Accumulator 1 A,#data Move immediate data to Accumulator 2 Rn,A Move Accumulator to register 1 Rn,direct Move direct byte to register 2 Rn,#data Move immediate data to register 2 direct,A Move Accumulator to direct byte 2 direct,Rn Move register to direct byte 2

^{*} Note: MOV A,ACC is not a valid instruction

Mnemonic		Description	Byte	Cycle
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move Accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
Data transfer (co	ont.)			
MOVC	A,@A+DPTR	Move code byte relative to DPTR to Accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to Accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr) to Accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr) to Accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with Accumulator	1	1
XCH	A,direct	Exchange direct byte with Accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with Accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit ind. RAM with Accu	1	1
Boolean variabl	e manipulation			
CLR	С	Clear Carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	С	Set Carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	С	Complement Carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to Carry flag	2	2
ANL	C,/bit	AND complement of direct bit to Carry	2	2
ORL	C,bit	OR direct bit to Carry flag	2	2
ORL	C,/bit	OR complement of direct bit to Carry	2	2
MOV	C,bit	Move direct bit to Carry flag	2	1
MOV	bit,C	Move Carry flag to direct bit	2	2

Mnemonic		Description	Byte	Cycle
Program and r	nachine control			
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if Accumulator is zero	2	2
JNZ	rel	Jump if Accumulator is not zero	2	2
JC	rel	Jump if Carry flag is set	2	2
JNC	rel	Jump if Carry flag is not set	2	2
JB	bit,rel	Jump if direct bit set	3	2
JNB	bit,rel	Jump if direct bit not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct to Accu and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to Accu and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp.immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn - Working register R0-R7 direct - 128 internal RAM locations, any I/O port,

control or status register

@Ri — Indirect internal RAM location addressed

by register R0 or R1
#data - 8-bit constant included in instruction

#data 16 – 16-bit constant included as bytes 2 & 3 of instruction

bit – 128 software flags, any I/O pin, control or status bit

A - Accumulator

All mnemonics copyrighted © Intel Corporation 1979

Notes on program addressing modes:

addr 16 — Destination address for LCALL & LJMP may be anywhere within the 64-Kbyte

program memory address space.

addr 11 — Destination address for ACALL & A.M.

 Destination address for ACALL & AJMP will be within the same 2-Kbyte page of program memory as the first byte of the following instruction.

rel — SJMP and all conditional jumps include an 8-bit offset byte. Range is + 127/–128 bytes relative to first byte of the following

instruction.

Instruction Opcodes in Hexadecimal Order

	,						
Hex Code	Number of Bytes	Mnemonic	Operands	Hex Code	Number of Bytes	Mnemonic	Operands
00	1	NOP		34	2	ADDC	A,#data
01	2	AJMP	code addr	35	2	ADDC	A,data addr
02	3	LJMP	code addr	36	1	ADDC	A,@R0
03	1	RR	A	37	1	ADDC	A,@R1
04	1	INC	A	38	1	ADDC	A,R0
05	2	INC	data addr	39	1	ADDC	A,R1
06	1	INC	@R0	3A	1	ADDC	A,R2
07	1	INC	@R1	3B	l 1	ADDC	A,R3
08	1	INC	R0	3C	1	ADDC	A,R4
09	1	INC	R1	3D	1	ADDC	A,R5
0A	1	INC	R2	3E	1	ADDC	A,R7
0B	1	INC	R3	3F	1	ADDC	A,R7
0C	1	INC	R4	40	2	JC	code addr
0D	1	INC	R5	41	2	AJMP	code addr
0E	1	INC	R6	42	2	ORL	data addr,A
0F	1	INC	R7	43	3	ORL	data addr,#data
10	3	JBC	bit addr code addr	44	2	ORL	A,#data
11	2	ACALL	code addr	45	2	ORL	A.data addr
12	3	LCALL	code addr	46	1	ORL	A,@R0
13	1	RRC	A	47	1	ORL	A,@R1
14	1	DEC	A	48	1	ORL	A.R0
15	2	DEC	data addr	49	1	ORL	A.R1
16	1	DEC	@R0	4A	l i	ORL	A,R2
17	1	DEC	@R1	4B	1	ORL	A,R3
18	1	DEC	R0	4C	1	ORL	A,R4
19	1	DEC	R1	4D	1	ORL	A.R5
1A	1	DEC	R2	4E	1	ORL	A,R6
1B	1	DEC	R3	4F	1	ORL	A,R7
1C	1	DEC	R4	50	2	JNC	code addr
1D	1	DEC	R5	51	2	ACALL	code addr
1E	1	DEC	R6	52	2	ANL	data addr,A
1F	1	DEC	R7	53	3	ANL	data addr,#data
20	3	JB	bit addr code addr	54	2	ANL	A,#data
21	2	AJMP	code addr	55	2	ANL	A,data addr
22	1	RET		56	1	ANL	A,@R0
23	1	RL	Α	57	1	ANL	A,@R1
24	2	ADD	A,#data	58	1	ANL	A,R0
25	2	ADD	A,data addr	59	1	ANL	A,R1
26	1	ADD	A,@R0	5A	1	ANL	A,R2
27	1	ADD	A,@R1	5B	1	ANL	A,R3
28	1	ADD	A,R0	5C	1	ANL	A,R4
29	1	ADD	A,R1	5D	1	ANL	A,R5
2A	1	ADD	A,R2	5E	1	ANL	A,R6
2B	1	ADD	A,R3	5F	1	ANL	A,R7
2C	1	ADD	A,R4	60	2	JZ	code addr
2D	1	ADD	A,R5	61	2	AJMP	code addr
2E	1	ADD	A,R6	62	2	XRL	data addr,A
2F	1	ADD	A,R7	63	3	XRL	data addr,#data
30	3	JNB	bit addr, code addr	64	2	XRL	A,#data
31	2	ACALL	code addr	65	2	XRL	A,data addr
32	1	RETI		66	1	XRL	A,@R0
33	1	RLC	Α	67	1	XRL	A,@R1

Instruction Opcodes in Hexadecimal Order (continued)

Hex Code	Number of Bytes	Mnemonic	Operands	Hex Code	Number of Bytes	Mnemonic	Operands
68	1	XRL	A,R0	9C	1	SUBB	A,R4
69	1	XRL	A,R1	9D	1	SUBB	A,R5
6A	1	XRL	A,R2	9E	1	SUBB	A.R6
6B	1	XRL	A,R3	9F	1	SUBB	A,R7
6C	1	XRL	A.R4	A0	2	ORL	C,/bit addr
6D	1	XRL	A,R5	A1	2	AJMP	code addr
6E	1	XRL	A,R6	A2	2	MOV	C,bit addr
6F	1	XRL	A,R7	A3	1	INC	DPTR
70	2	JNZ	code addr	A4	1	MUL	AB
71	2	ACALL	code addr	A5		reserved	,
72	2	ORL	C,bit addr	A6	2	MOV	@R0,data addr
73	1	JMP	@A+DPTR	A7	2	MOV	@R1,data addr
74	2	MOV	A,#data	A8	2	MOV	R0,data addr
75	3	MOV	data addr,#data	A9	2	MOV	R1,data addr
75 76	2	MOV	@R0.#data	AA	2	MOV	R2,data addr
70 77	2	MOV	O ,		2		•
			@R1,#data	AB		MOV	R3,data addr
78	2	MOV	R0,#data	AC	2	MOV	R4,data addr
79	2	MOV	R1,#data	AD	2	MOV	R5,data addr
7A	2	MOV	R2,#data	ΑE	2	MOV	R6,data addr
7B	2	MOV	R3,#data	ΑF	2	MOV	R7,data addr
7C	2	MOV	R4,#data	B0	2	ANL	C,/bit addr
7D	2	MOV	R5,#data	B1	2	ACALL	code addr
7E	2	MOV	R6,#data	B2	2	CPL	bit addr
7F	2	MOV	R7,#data	B3	1	CPL	С
80	2	SJMP	code addr	B4	3	CJNE	A,#data,code addr
81	2	AJMP	code addr	B5	3	CJNE	A,data addr,code addr
82	2	ANL	C,bit addr	B6	3	CJNE	@R0,#data,code addr
83	1	MOVC	A,@A+PC	B7	3	CJNE	@R1,#data.code addr
84	1	DIV	AB	B8	3	CJNE	R0,#data,code addr
85	3	MOV	data addr,data addr	B9	3	CJNE	R1,#data,code addr
86	2	MOV	data addr,@R0	BA	3	CJNE	R2,#data,code addr
87	2	MOV	data addr,@R1	BB	3	CJNE	R3,#data,code addr
88	2	MOV	data addr,R0	BC	3	CJNE	R4,#data.code addr
89	2	MOV	data addr,R1	BD	3	CJNE	R5,#data,code addr
8A	2	MOV	data addr, R2	BE	3	CJNE	R6,#data.code addr
8B	2	MOV	data addr, R3	BF	3	CJNE	R7,#data,code addr
8C	2	моу	data addr,R4	C0	2	PUSH	data addr
8D	2	MOV	data addr, R5	C1	2	AJMP	code addr
8E	2	MOV	data addr, R6	C2	2	CLR	bit addr
8F	2	MOV	data addr,R7	C3	1	CLR	C
90	3	MOV	DPTR,#data	C4	1	SWAP	A
91	2	ACALL	code addr	C5	2	XCH	A,data addr
92	2	MOV	bit addr.C	C6	1	XCH	A,@R0
93	1	MOVC	A,@A+DPTR	C7	1	XCH	A,@R1
94	2	SUBB	A,#data	C8		XCH	A,@h i A,R0
95	2	SUBB	A,#uala A,data addr	C9	1	XCH	A,R1
96	1	SUBB	A,@R0	CA	1	XCH	
96 97			, _				A,R2
	1	SUBB	A,@R1	CB	1	XCH	A,R3
98	1	SUBB	A,R0	CC	1	XCH	A,R4
99	1	SUBB	A,R1	CD	1	XCH	A,R5
9A	1	SUBB	A,R2	CE	1	XCH	A,R6
9B	1	SUBB	A,R3	CF	1	XCH	A,R7

Instruction Opcodes in Hexadecimal Order (continued)

		-	
Hex Code	Number of Bytes	Mnemonic	Operands
D0	2	POP	data addr
D1	2	ACALL	code addr
D2	2	SETB	bit addr
D3	1	SETB	С
D4	1	DA	Α
D5	3	DJNZ	data addr,code addr
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,code addr
D9	2	DJNZ	R1,code addr
DA	2	DJNZ	R2,code addr
DB	2	DJNZ	R3,code addr
DC	2	DJNZ	R4,code addr
DD	2	DJNZ	R5,code addr
DE	2	DJNZ	R6,code addr
DF	2	DJNZ	R7,code addr
E0	1	MOVX	A,@DPTR
E1	2	AJMP	code addr
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	Α
E5	2	MOV	A,data addr *
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	code addr
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	data addr,A
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

^{*} Note: MOV A,ACC is not a valid instruction

Absolute Maximum Ratings¹⁾

Ambient Temperature under Bias 0 to 70° C Storage Temperature -65 to $+150^{\circ}$ C Voltage on Any Pin with Respect to Ground (VSS) -0.5 to +7 V Power Dissipation 2 W

D.C. Characteristics

TA = 0 to 70°C; VCC = $5 V \pm 10\%$; VSS = 0 V

Symbol	Parameter	Lir	nit Values	Unit	Test Condition
		Min.	Max.	1	
VIL	Input Low Voltage	-0.5	0.8		
VIH	Input High Voltage (Except RST/VPD and XTAL2)	2.0	1400.05		_
VIH1	Input High Voltage to RST/VPD for Reset, XTAL2	2.5	VCC+0.5		XTAL1 to VSS
VPD	Power Down Voltage to RST/VPD	4.5	5.5		VCC = 0V
VOL	Output Low Voltage Ports 1, 2, 3		0.45	v	IOL = 1.6 mA
VOL1	Output Low Voltage Port 0, ALE, PSEN		0.45		IOL = 3.2 mA
VOH	Output High Voltage Ports 1, 2, 3	2.4			IOH = -80 μA
VOH1	Output High Voltage Port 0, ALE, PSEN	2.4			$IOH = -400 \mu A$
IIL	Logical 0 Input Current Ports 1, 2, 3		-800	μА	VIL = 0.45 V
IIL2	Logical 0 Input Current XTAL 2		-2.0	mA	XTAL1 = VSS VIL = 0.45 V
IIH1	Input High Current to RST/VPD for Reset		500		VIN = VCC-1.5 V
ILI	Input Leakage Current to Port 0, EA		±10	μΑ	0V < VIN < VCC
ICC	Power Supply Current		175	mA	All outputs disconnected
IPD	Power Down Current		15	1 1114	VCC = 0V
CIO	Capacitance of I/O Buffer		10	pF	$f_c = 1 \text{ MHz}$

¹⁾ Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

A.C. Characteristics

TA = 0° C to 70° C; VCC = $5 \text{ V} \pm 10\%$; VSS = 0 V

(CL for Port 0, ALE and PSEN Outputs = 100 pF; CL for All Other Outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	:		Limit Values		Unit
		12 [MHz Clock	Variable Clock 1/TCLCL = 1.2 MHz to 12 MHz		
		Min.	Max.	Min.	Max.	
TLHLL	ALE Pulse Width	127		2TCLCL-40		
TAVLL	Address Setup to ALE	53	_	TCLCL-30	_	
TLLAX1	Address Hold after ALE	48		TCLCL-35		
TLLIV	ALE to Valid Instr In	-	233	_	4TCLCL-100	
TLLPL	ALE to PSEN	58		TCLCL-25		ns
TPLPH	PSEN Pulse Width	215	7-	3TCLCL-35	7-	
TPLIV	PSEN to Valid Instr In	_	150	-	3TCLCL-100	
TPXIX	Input Instr Hold after PSEN	0	-	0	_	
TPXIZ*)	Input Instr Float after PSEN	_	63	_	TCLCL-20	
TPXAV*)	Address Valid after PSEN	75	-	TCLCL-8	_	
TAVIV	Address to Valid Instr In	_	302	-	5TCLCL-115	
TAZPL	Address Float to PSEN	0	-	0	_	

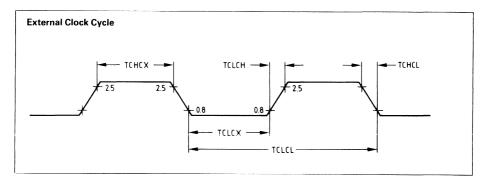
External Data Memory Characteristics

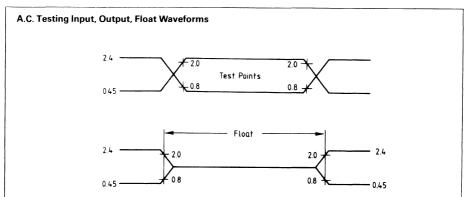
Symbol	Parameter			Limit Values		Unit
		12 N	1Hz Clock		ole Clock 2 MHz to 12 MHz	
		Min.	Max.	Min.	Max.	
TRLRH	RD Pulse Width	400		6TCLCL-100		
TWLWH	WR Pulse Width	400	-	BICECE-100	-	
TLLAX 2	Address Hold after ALE	132		2TCLCL-35		
TRLDV	RD to Valid Data In	_	250	_	5TCLCL-165	
TRHDX	Data Hold after RD	0	_	0	-	1
TRHDZ	Data Float after RD		97		2TCLCL-70	
TLLDV	ALE to Valid Data In	_	517	7-	8TCLCL-150	ns
TAVDV	Address to Valid Data In		585		9TCLCL-165	
TLLWL	ALE to WR or RD	200	300	3TCLCL-50	3TCLCL+50	
TAVWL	Address to WR or RD	203	_	4TCLCL-130	-	
TWHLH	WR or RD High to ALE High	43	123	TCLCL-40	TCLCL+40	
TDVWX	Data Valid to WR Transition	33		TCLCL-50		
TQVWH	Data Setup before WR	433	_	7TCLCL-150]_	1
TWHQX	Data Hold after WR	33		TCLCL-50]	
TRLAZ	Address Float after RD	-	0		0	_

^{*)} Interfacing the SAB 8052A to devices with float times up to 75ns is permissible. This limited bus contention will not cause any damage to Port 0 drivers.

External Clock Drive XTAL2

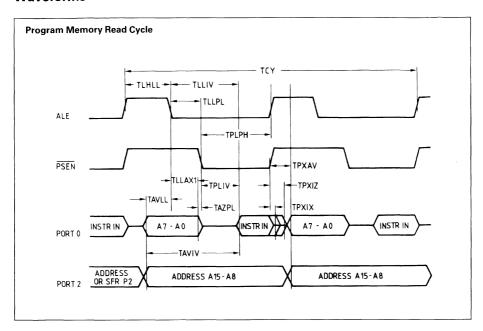
Symbol Parameter	Parameter		Unit	
		Variable Clock Freq = 1.2 MHz to 12 MHz		
			Min.	Max.
TCLCL	Oscillator Period	83.3	833.3	
TCHCX	High Time	20	TCLCL-TCLCX	
TCLCX	Low Time	20	TCLCL-TCHCX	ns
TCLCH	Rise Time		20	
TCHCL	Fall Time		20	

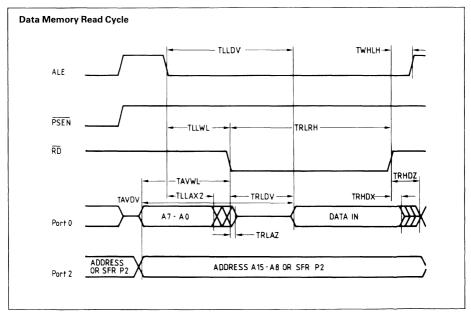


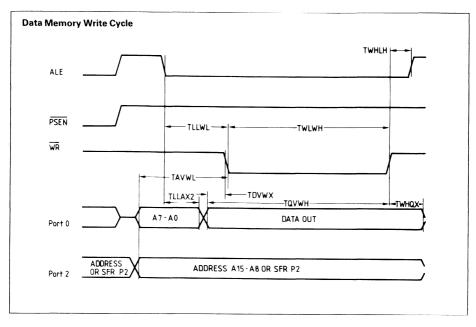


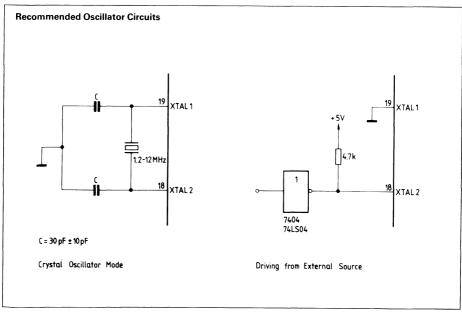
A.C. testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0". For timing purposes, the float state is defined as the point at which a P0 pin sinks 3.2mA or sources 400 $\upmu{\rm A}$ at the voltage test levels.

Waveforms







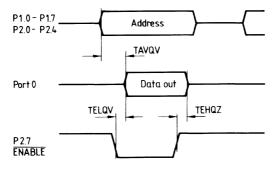


ROM Verification Characteristics

 $TA = 25^{\circ}C \pm 5^{\circ}C; \ VCC = 5 V \pm 10\%; \ VSS = 0 V$

Symbol	Parameter	Limit Values		Unit	
		Min.	Max.		
TAVQV	Address to Valid Data				
TELQV	Enable to Valid Data		48 TCLCL	ns	
TEHQZ	Data Float after Enable	0			
1/TCLCL	Oscillator Frequency	4	6	MHz	





Address: P1.0-P1.7 = A0-A7

P2.0-P2.4 = A8-A12

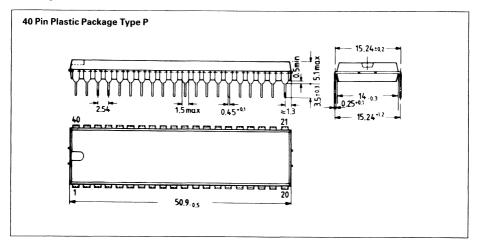
Data: Port 0 = D0-D7

P2.5-P2.6, $\overline{PSEN} = VSS$ ALE, $\overline{EA} = TTL$ high level

RST/VPD = VIH1

Inputs:

Package Outline



SAB 8032A/8052A

Ordering Information

Туре	Description	Ordering code
	8-Bit Single-Chip Microcomputer	
SAB 8052A-P	with mask-programmable ROM (Plastic)	Q 67120-C195
SAB 8032A-P	for external Memory (Plastic)	Q 67120-C196



SAB 8032A/8052A Ext.Temp. 8-Bit Single-Chip Microcontroller

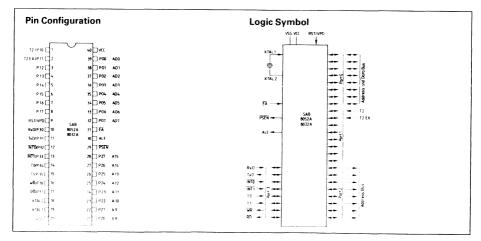
Extended Temperature Range: -40° to + 85°C -40° to +100°C

SAB 8052A-T40/85 SAB 8052A-T40/100 Mask-programmable ROM

- 8K × 8 ROM (SAB 8052A only)
- 256 × 8 RAM
- Four 8-bit ports, 32 I/O lines
- Three 16-bit timer/event counters
- High-performance full-duplex serial channel
- External memory expandable to 128 Kbyte
- Compatible with SAB 8080/8085 peripherals

SAB 8032A-T40/85 SAB 8032A-T40/100 External ROM

- Timer 2 capture capability
- Variable transmit/receive baud rate capability
- Boolean processor
- Most instructions execute in 1 µs
- 4 µs multiply and divide
- Upward-compatible with SAB 8031A/8051A



The SAB 8032A/8052A for the two extended temperature ranges -40 to $+85^{\circ}\text{C}$ and -40 to $+100^{\circ}\text{C}$ is fully compatible with the standard SAB 8032A/8052A with respect to architecture, instruction set, and software portability.

The SAB 8032A/8052A is a stand-alone, high-performance single-chip microcontroller fabricated in +5V advanced N-channel, silicon gate Siemens MYMOS technology, packaged in a 40-pin DIP package.

The SAB 8052A contains a non-volatile 8×8 readonly program memory; a volatile 256×8 read/write data memory; 32 I/O lines; three 16-bit timer/counters; a six-source, two-priority level, nested interrupt structure; a serial I/O port for either multiprocessor communications, I/O expansion, or full-duplex UART; as well as on-chip oscillator and clock circuits. The SAB 8032A is identical, except that it lacks the program memory.

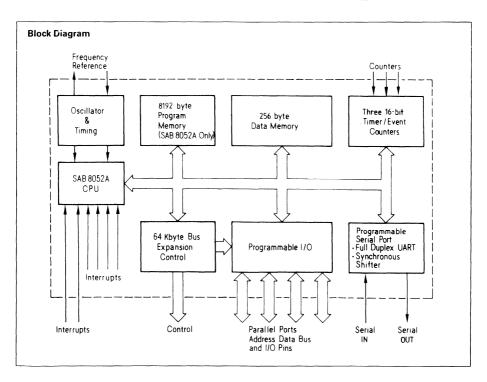
For systems that require extra capability, the SAB 8052A can be expanded using standard TTL-compatible memories and the byte-oriented SAB 8080 and SAB 8085 peripherals.

Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
P1.0-P1.7	1-8	1/0	Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. Port 1 can sink/source four LS TTL loads. Pins P1.0 and P1.1 also correspond to the special functions T2, external input to Timer 2, and T2EX, Timer 2 trigger input. The output latch on these two special function pins must be programmed to a one (1) for that function to operate.
RST/VPD	9	I	A high level on this pin resets the SAB 8052A. A small internal pulldown resistor permits power-on reset using only a capacitor connected to VCC. If VPD is held within its spec while VCC drops below spec, VPD will provide standby power to the RAM. When VPD is low, the RAM's current is drawn from VCC.
P3.0-P3.7	10-17	1/0	Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and RD and WR pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source four LS TTL loads. The secondary functions are assigned to the pins of Port 3, as follows: — R×D/data (P3.0). Serial port's receiver data input (asynchronous) or data input/output (synchronous). — T×D/clock (P3.1). Serial port's transmitter data output (asynchronous) or clock output (synchronous). — INTO (P3.2). Interrupt 0 input or gate control input for counter 0. — INTT (P3.3). Interrupt 1 input or gate control input for counter 1. — T0 (P3.4). Input to counter 0. — T1 (P3.5). Input to counter 0. — WR (P3.6). The write control signal latches the data byte from port 0 into the external data memory. — RD (P3.7). The read control signal enables external data memory to port 0.
XTAL1 XTAL2	19 18	I	XTAL 1 input to the oscillator's high-gain amplifier. Required when a crystal is used. Connect to VSS when external source is used on XTAL 2. XTAL 2 output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal or external source can be used.
P2.0-P2.7	21-28	1/0	Port 2 is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source four LS TTL loads.
PSEN	29	0	The program store enable output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
ALE	30	0	Provides address latch enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
ĒĀ	31	l	When held at a TTL high level, the SAB 8052A executes instructions from the internal ROM when the PC is less than 8192. When held at a TTL low level, the SAB 8052A fetches all instructions from external program memory. For the SAB 8032A this pin must be tied low.
P0.0-P0.7	39-32	1/0	Port 0 is an 8-bit open-drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source eight LS TTL loads.
VCC	40		+5V power supply during operation and program verification.
VSS	20		Ground (0 V).



Instruction Set Summary

Mnemonic		Description	Byte	Cycle
Arithmetic ope	erations			
ADD	A, Rn	Add register to Accumulator	1	1
ADD	A, direct	Add direct byte to Accumulator	2	1
ADD	A, @Ri	Add indirect RAM to Accumulator	1	1
ADD	A,#data	Add immediate data to Accumulator	2	1
ADDC	A,Rn	Add register to Accumulator with Carry flag	1	1
ADDC	A,direct	Add direct byte to A with Carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with Carry flag	1	1
ADDC	A,#data	Add immediate data to A with Carry flag	2	1
SUBB	A,Rn	Subtract register from A with borrow	1	1
SUBB	A,direct	Subtract direct byte from A with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	А	Increment Accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	А	Decrement Accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	А	Decimal adjust Accumulator	1	1
Logical operati	ons			
ANL	A,Rn	AND register to Accumulator	1	1
ANL	A,direct	AND direct byte to Accumulator	2	1
ANL	A,@Ri	AND indirect RAM to Accumulator	1	1
ANL	A,#data	AND immediate data to Accumulator	2	1
ANL	direct,A	AND Accumulator to direct byte	2	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Logical opera	tions (cont'd)			
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to Accumulator	1	1
ORL	A,direct	OR direct byte to Accumulator	2	1
ORL	A,@Ri	OR indirect RAM to Accumulator	1	1
ORL	A,#data	OR immediate data to Accumulator	2	1
ORL	direct,A	OR Accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive OR register to Accumulator	1	1
XRL	A,direct	Exclusive OR direct byte to Accumulator	2	1
XRL	A,@Ri	Exclusive OR indirect RAM to Accumulator	1	1
XRL	A,#data	Exclusive OR immediate data to Accumulator	2	1
XRL	direct,A	Exclusive OR Accumulator to direct byte	2	1
XRL	direct,#data	Exclusive-OR immediate data to direct byte	3	2
CLR	Α	Clear Accumulator	1	1
CPL	Α	Complement Accumulator	1	1
RL	Α	Rotate Accumulator left	1	1
RLC	Α	Rotate A left through the Carry flag	1	1
RR	А	Rotate Accumulator right	1	1
RRC	Α	Rotate A right through Carry flag	1	1
SWAP	Α	Swap nibbles within the Accumulator	1	1
Data transfer				
MOV	A,Rn	Move register to Accumulator	1	1
MOV	A direct *1	Mayo direct byte to Assumulator	2	1

MOV	A,Rn	Move register to Accumulator	1	1
MOV	A,direct *)	Move direct byte to Accumulator	2	1
MOV	A,@Ri	Move indirect RAM to Accumulator	1	1
MOV	A,#data	Move immediate data to Accumulator	2	1
MOV	Rn,A	Move Accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move Accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct byte	3	2

^{*)} MOV A,ACC is not a valid instruction

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Data transfer (c	ont'd)			
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move Accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move code byte relative to DPTR to Accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to Accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr) to Accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr) to Accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct _	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with Accumulator	1	1
XCH	A,direct	Exchange direct byte with Accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with Accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit ind. RAM with A	1	1
Boolean variabl	le manipulation			
CLR	С	Clear Carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	С	Set Carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	С	Complement Carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to Carry flag	2	2
ANL	C,/bit	AND complement of direct bit to Carry	2	2
ORL	C,bit	OR direct bit to Carry flag	2	2
ORL	C,/bit	OR complement of direct bit to Carry	2	2
MOV	C,bit	Move direct bit to Carry flag	2	1
MOV	bit,C	Move Carry flag to direct bit	2	2

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Program and m	achine control			
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr)	2	2
JMP	@A + DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if Accumulator is zero	2	2
JNZ	rel	Jump if Accumulator is not zero	2	2
JC	rel	Jump if Carry flag is set	2	2
JNC	rel	Jump if Carry flag is not set	2	2
JB	bit,rel	Jump if direct bit is set	3	2
JNB	bit,rel	Jump if direct bit is not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct to A and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to A and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp.immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn – Working register R0-R7

direct - 128 internal RAM locations, any I/O port, control or status register

@Ri – Indirect internal RAM location addressed by register R0 or R1

#data - 8-bit constant included in instruction #data 16 - 16-bit constant included as bytes 2 and 3 of instruction

bit – 128 software flags, any I/O pin, control or status bit

A - Accumulator

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Notes on program addressing modes:

addr 16 – Destination address for LCALL and LJMP may be anywhere within the 64 Kbyte program memory address space.

addr 11 – Destination address for ACALL and AJMP will be within the same 2 Kbyte page of program memory as the first byte of the following instruction.

rel — SJMP and all conditional jumps include an 8-bit offset byte. Range is +127/-128 bytes relative to first byte of the following instruction.

Instruction Op Codes in Hexadecimal Order

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Hex Code	Number of Bytes	Mnemonic	Operands	Hex Code	Number of Bytes	Mnemonic	Operands
00	1	NOP		34	2	ADDC	A,#data
01	2	AJMP	code addr	35	2	ADDC	A,data addr
02	3	LJMP	code addr	36	1	ADDC	A,@R0
03	1	RR	A	37	1	ADDC	A,@R1
04	l i	INC	Α	38	1	ADDC	A,R0
05	2	INC	data addr	39	1	ADDC	A,R1
06	1	INC	@R0	3A	1	ADDC	A,R2
07	1	INC	@R1	3B	1	ADDC	A,R3
08	1	INC	R0	3C	1	ADDC	A,R4
09	1	INC	R1	3D	1	ADDC	A,R5
0A	1	INC	R2	3E	1	ADDC	A,R7
0B	1	INC	R3	3F	1	ADDC	A,R7
0C	1	INC	R4	40	2	JC	code addr
0D	l i	INC	R5	41	2	AJMP	code addr
0E	ĺ	INC	R6	42	2	ORL	data addr.A
0F	1	INC	R7	43	3	ORL	data addr,#data
10	3	JBC	bit addr code addr	44	2	ORL	A,#data
11	2	ACALL	code addr	45	2	ORL	A,data addr
12	3	LCALL	code addr	46	1	ORL	A,@R0
13	1	RRC	A	47	1	ORL	A,@R1
14	1	DEC	Â	48	l i	ORL	A,R0
15	2	DEC	data addr	49	l i	ORL	A.R1
16	1	DEC	@R0	4A	l i	ORL	A,R2
17	1	DEC	@R1	4B	1	ORL	A,R3
18	i	DEC	R0	4C	1	ORL	A,R4
19	l i	DEC	R1	4D	1	ORL	A,R5
1A	l i	DEC	R2	4E	l i	ORL	A,R6
1B	1	DEC	R3	4F	1	ORL	A,R7
1C	1	DEC	R4	50	2	JNC	code addr
1D	1	DEC	R5	51	2	ACALL	code addr
1E	1	DEC	R6	52	2	ANL	data addr.A
1F	1	DEC	R7	53	3	ANL	data addr,#data
20	3	JB	bit addr code addr	54	2	ANL	A,#data
21	2	AJMP	code addr	55	2	ANL	A,data addr
22	1	RET	Code addi	56	1	ANL	A,@R0
23	l i	RL	A	57	1	ANL	A,@R1
24	2	ADD	A,#data	58	1	ANL	A,R0
25	2	ADD	A,data addr	59	1	ANL	A,R1
26	1	ADD	A,@R0	5A	i	ANL	A,R2
27	l i	ADD	A,@R1	5B	1	ANL	A,R3
28	1	ADD	A,R0	5C	1	ANL	A,R4
29	1	ADD	A,R1	5D	1	ANL	A,R5
2A	1	ADD	A,R2	5E	1	ANL	A,R6
2B	l i	ADD	A,R3	5F	1	ANL	A,R7
2C	1	ADD	A,R4	60	2	JZ	code addr
2D	1	ADD	A,R5	61	2	AJMP	code addr
2E	1	ADD	A,R6	62	2	XRL	data addr.A
2F	1	ADD	A,R7	63	3	XBL	data addr,#data
30	3	JNB	bit addr, code addr	64	2	XRL	A,#data
31	2	ACALL	code addr	65	2	XRL	A,data addr
32	1	RETI	COUC GOO!	66	1	XRL	A,@R0
33	li i	RLC	A	67	1	XRL	A,@R1
	<u> </u>	INLO	^		1'	I AITE	1,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,

Instruction Op Codes in Hexadecimal Order (cont'd)

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Hex Code	Number of Bytes	Mnemonic	Operands	Hex Code	Number of Bytes	Mnemonic	Operands
68	1	XRL	A,R0	9C	1	SUBB	A,R4
69	1	XRL	A,R1	9D	1	SUBB	A,R5
6A	1	XRL	A,R2	9E	1	SUBB	A,R6
6B	1	XRL	A,R3	9F	1	SUBB	A.R7
6C	1	XRL	A.R4	A0	2	ORL	C,/bit addr
6D	1	XRL	A,R5	A1	2	AJMP	code addr
6E	1	XRL	A,R6	A2	2	MOV	C,bit addr
6F	1	XRL	A.R7	A3	1	INC	DPTR
70	2	JNZ	code addr	A4	1	MUL	AB
71	2	ACALL	code addr	A5		reserved	
72	2	ORL	C,bit addr	A6	2	MOV	@R0,data addr
73	1	JMP	@A+DPTR	A7	2	MOV	@R1,data addr
74	2	MOV	A,#data	A8	2	MOV	R0,data addr
75	3	MOV	data addr.#data	A9	2	MOV	R1,data addr
76	2	MOV	@R0,#data	AA	2	MOV	R2,data addr
77	2	MOV	@R1,#data	AB	2	MOV	R3,data addr
78	2	MOV	R0,#data	AC	2	MOV	R4,data addr
79	2	MOV	R1,#data	AD	2	MOV	R5,data addr
7A	2	MOV	R2,#data	AE	2	MOV	R6,data addr
7B	2	MOV	R3,#data	AF	2	MOV	R7,data addr
7C	2	MOV	R4,#data	B0	2	ANL	C./bit addr
7D	2	MOV	R5,#data	B1	2	ACALL	code addr
7E	2	MOV	R6,#data	B2	2	CPL	bit addr
7F	2	MOV	R7,#data	B3	1	CPL	C
80	2	SJMP	code addr	B4	3	CJNE	A,#data,code addr
81	2	AJMP	code addr	B5	3	CJNE	A,data addr,code addr
82	2	ANL	C,bit addr	B6	3	CJNE	@R0,#data,code addr
83	1	MOVC	A,@A+PC	B7	3	CJNE	@R1,#data,code addr
84	1	DIV	AB	B8	3	CJNE	R0,#data.code addr
85	3	MOV	data addr.data addr	B9	3	CJNE	R1,#data,code addr
86	2	MOV	data addr.@R0	BA	3	CJNE	R2,#data,code addr
87	2	MOV	data addr,@R1	BB	3	CJNE	R3,#data,code addr
88	2	MOV	data addr, R0	ВС	3	CJNE	R4,#data.code addr
89	2	MOV	data addr.R1	BD	3	CJNE	R5,#data,code addr
8A	2	MOV	data addr, R2	BE	3	CJNE	R6,#data,code addr
8B	2	MOV	data addr, R3	BF	3	CJNE	R7,#data.code addr
8C	2	MOV	data addr,R4	CO	2	PUSH	data addr
8D	2	MOV	data addr, R5	C1	2	AJMP	code addr
8E	2	MOV	data addr, R6	C2	2	CLR	bit addr
8F	2	MOV	data addr,R7	C3	1	CLR	C
90	3	MOV	DPTR,#data	C4	1	SWAP	A
91	2	ACALL	code addr	C5	2	XCH	A,data addr
92	2	MOV	bit addr,C	C6	1	XCH	A,@R0
93	1	MOVC	A,@A+DPTR	C7	1	XCH	A,@R1
94	2	SUBB	A,#data	C8	1	XCH	A,R0
95	2	SUBB	A,data addr	C9	1	XCH	A,R1
96	1	SUBB	A,@R0	CA	1	XCH	A,R2
97	1	SUBB	A,@R1	CB	1	XCH	A,R3
98	1	SUBB	A,R0	CC	1	XCH	A,R4
99	1	SUBB	A,R1	CD	1	XCH	A,R5
9A	1	SUBB	A,R2	CE	1	XCH	A,R6
9B	1	SUBB	A,R3	CF	i	XCH	A,R7
		1333	,		L'	,,,,,,	

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex Code	Number of Bytes	Mnemonic	Operands
D0	2	POP	data addr
D1	2	ACALL	code addr
D2	2	SETB	bit addr
D3	1	SETB	С
D4	1	DA	A
D5	3	DJNZ	data addr,code addr
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,code addr
D9	2	DJNZ	R1,code addr
DA	2	DJNZ	R2,code addr
DB	2	DJNZ	R3,code addr
DC	2	DJNZ	R4,code addr
DD	2	DJNZ	R5,code addr
DE	2	DJNZ	R6,code addr
DF	2	DJNZ	R7,code addr
E0	1	MOVX	A,@DPTR
E1	2	AJMP	code addr
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,data addr*
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	ĺ	MOV	A,R0
E9	ĺ	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	code addr
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	data addr,A
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	RO,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC		MOV	R4,A
FD FD		MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A
	L'	IVIOV	111,7

^{*)} MOV A,ACC is not a valid instruction

Absolute Maximum Ratings 1)

Ambient Temperature under Bias $-40 \text{ to} + 85^{\circ}\text{C} \text{ for T40/85} \\ -40 \text{ to} + 100^{\circ}\text{C} \text{ for T40/100}$

Storage Temperature -65 to +150°C

Voltage on Any Pin with Respect to Ground (VSS) $-0.5\ to\ +\ 7\ V$ Power Dissipation 2 W

DC Characteristics

 $VCC = 5 V \pm 10\%$; VSS = 0 V; $TA = -40 \text{ to} + 85^{\circ}C \text{ for } T40/85$; $TA = -40 \text{ to} + 100^{\circ}C \text{ for } T40/100$;

Symbol	Parameter	Lir	Limit Values		Test Condition
		min.	max.		
VIL	Input Low Voltage	-0.5	0.8		
VIH	Input High Voltage (Except RST/VPD and XTAL2)	2.0	1100 0 5		
VIH1	Input High Voltage to RST/VPD for Reset, XTAL2	2.5	VCC+0.5		XTAL1 to VSS
VPD	Power Down Voltage to RST/VPD	4.5	5.5		VCC = 0 V
VOL	Output Low Voltage Ports 1, 2, 3		0.45	v	IOL = 1.6 mA
VOL1	Output Low Voltage Port 0, ALE, PSEN		0.45		IOL = 3.2 mA
VOH	Output High Voltage Ports 1, 2, 3	2.4			ΙΟΗ – –80 μΑ
VOH1	Output High Voltage Port 0, ALE, PSEN	2.4	-		IOH = -400 µA
IIL	Logical 0 Input Current Ports 1, 2, 3		-800	μА	VIL = 0.45 V
IIL2	Logical 0 Input Current XTAL 2		-2.5	mA	XTAL1 = VSS VIL = 0.45 V
IIH1	Input High Current to RST/VPD for Reset		500		VIN = VCC-1.5 V
ILI	Input Leakage Current to Port 0, EA		±10	μA	0V < VIN < VCC
ICC	Power Supply Current		175	mA	All outputs disconnected
IPD	Power Down Current		15	I	VCC = 0 V
CIO	Capacitance of I/O Buffer		10	pF	f _c = 1 MHz

¹⁾ Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC Characteristics for T40/85

VCC = 5V \pm 10%; VSS = 0V; TA = -40° to $+85^{\circ}$ C (CL for Port 0, ALE and \overline{PSEN} Outputs = 100 pF; CL for All Other Outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter		Limit Values				
		12 MHz Clock		1	ble Clock .2 MHz to 12 MHz		
		min.	max.	min.	max.		
TLHLL	ALE Pulse Width	127		2TCLCL-40			
TAVLL	Address Setup to ALE	53	_	TCLCL-30	_		
TLLAX1	Address Hold after ALE	48		TCLCL-35			
TLLIV	ALE to Valid Instruction In	_	233	_	4TCLCL-100		
TLLPL	ALE to PSEN	58		TCLCL-25		ns	
TPLPH	PSEN Pulse Width	215		3TCLCL-35	_		
TPLIV	PSEN to Valid Instruction In	_	150	_	3TCLCL-100		
TPXIX	Input Instr Hold after PSEN	0		0	_		
TPXIZ*)	Input Instr Float after PSEN	_	63	_	TCLCL-20		
TPXAV*)	Address Valid after PSEN	75	-	TCLCL-8	_		
TAVIV	Address to Valid Instruction In	-	302	-	5TCLCL-115		
TAZPL	Address Float to PSEN	0	-	0	_		

External Data Memory Characteristics

Symbol	Parameter			Limit Values		Unit
			1Hz Clock	Variable Clock 1/TCLCL = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
TRLRH	RD Pulse Width	400		6TCLCL-100		
TWLWH	WR Pulse Width	400	-	BICECE-100	_	
TLLAX 2	Address Hold after ALE	132		2TCLCL-35		
TRLDV	RD to Valid Data In	_	250	_	5TCLCL-165	
TRHDX	Data Hold after RD	0	_	0	_	
TRHDZ	Data Float after RD		97		2TCLCL-70	
TLLDV	ALE to Valid Data In	_	517]-	8TCLCL-150	ns
TAVDV	Address to Valid Data In		585		9TCLCL-165	
TLLWL	ALE to WR or RD	200	300	3TCLCL-50	3TCLCL+50	
TAVWL	Address to WR or RD	203	-	4TCLCL-130	_	
TWHLH	WR or RD High to ALE High	43	123	TCLCL-40	TCLCL+40	ì
TDVWX	Data Valid to WR Transition	33		TCLCL-50		
TQVWH	Data Setup before WR	433	_	7TCLCL-150	_	
TWHQX	Data Hold after WR	33		TCLCL-50		
TRLAZ	Address Float after RD	_	0	_	0	

^{*)} Interfacing the SAB 8052A to devices with float times up to 75ns is permissible. This limited bus contention will not cause any damage to Port 0 drivers.

AC Characteristics for T40/100

VCC = 5 V $\pm 10\%$; VSS = 0 V; TA = -40° to $+100^{\circ}C$

(CL for Port 0, ALE and PSEN Outputs = 100 pF; CL for All Other Outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter		Limit Values			
		12 MHz Clock		Variable Clock 1/TCLCL = 1.2 MHz to 10 MHz		
		min.	max.	min.	max.	
TLHLL	ALE Pulse Width	160		2TCLCL-40		
TAVLL	Address Setup to ALE	70]-	TCLCL-30	_	
TLLAX1	Address Hold after ALE	65		TCLCL-35		
TLLIV	ALE to Valid Instruction In		300	-	4TCLCL-100	
TLLPL	ALE to PSEN	75		TCLCL-25		ns
TPLPH	PSEN Pulse Width	265	_	3TCLCL-35	_	
TPLIV	PSEN to Valid Instructrion In	_	200	_	3TCLCL-100	
TPXIX	Input Instruction Hold after PSEN	0	-	0	_	
TPXIZ*)	Input Instruction Float after PSEN	-	80	_	TCLCL-20	
TPXAV*)	Address Valid after PSEN	92	-	TCLCL-8	_	
TAVIV	Address to Valid Instruction In		385	_	5TCLCL-115	
TAZPL	Address Float to PSEN	0	-	0	_	

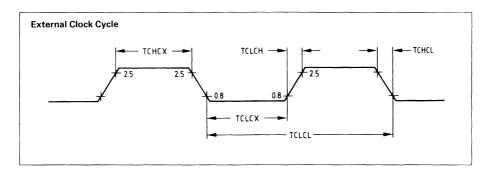
External Data Memory Characteristics

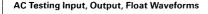
Symbol	ymbol Parameter		Limit Values				
		12 MHz Clock		Variable Clock 1/TCLCL = 1.2 MHz to 10 MHz			
		min.	max.	min.	max.		
TRLRH	RD Pulse Width	500		CTC C 100			
TWLWH	WR Pulse Width	500	-	6TCLCL-100	_		
TLLAX 2	Address Hold after ALE	165		2TCLCL-35	1		
TRLDV	RD to Valid Data In	-	335	_	5TCLCL-165		
TRHDX	Data Hold after RD	0	-	0	-		
TRHDZ	Data Float after RD		130		2TCLCL-70		
TLLDV	ALE to Valid Data In	_	650]_	8TCLCL-150	ns	
TAVDV	Address to Valid Data In		735		9TCLCL-165		
TLLWL	ALE to WR or RD	250	350	3TCLCL-50	3TCLCL+50		
TAVWL	Address to WR or RD	270	-	4TCLCL-130	-		
TWHLH	WR or RD High to ALE High	60	140	TCLCL-40	TCLCL+40		
TDVWX	Data Valid to WR Transition	50		TCLCL-50			
TQVWH	Data Setup before WR	550	_	7TCLCL-150]_		
TWHQX	Data Hold after WR	50		TCLCL-50			
TRLAZ	Address Float after RD	-	0	_	0		

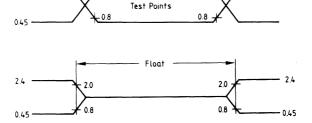
^{*)} Interfacing the SAB 8052A to devices with float times up to 92 ns is permissible. This limited bus contention will not cause any damage to Port 0 drivers.

External Clock Drive XTAL2

Symbol	Parameter		Limit Values		
			Variable Clock Freq. = 1.2 MHz to 12 MHz (T40/85) Freq. = 1.2 MHz to 10 MHz (T40/100)		
		min.	max.		
TCLCL	Oscillator Period T40/85 T40/100	83.3 100	833.3		
TCHCX	High Time	20	TCLCL-TCLCX		
TCLCX	Low Time	20	TCLCL-TCHCX	ns	
TCLCH	Rise Time		20		
TCHCL	Fall Time		20		



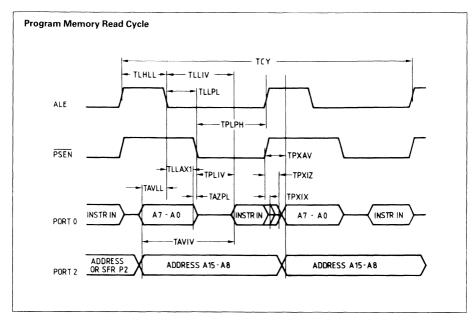


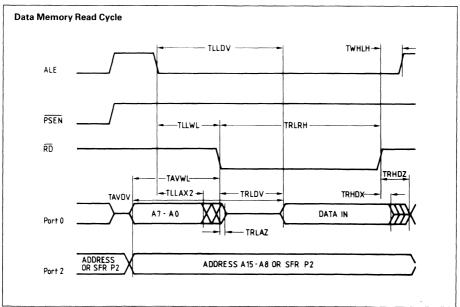


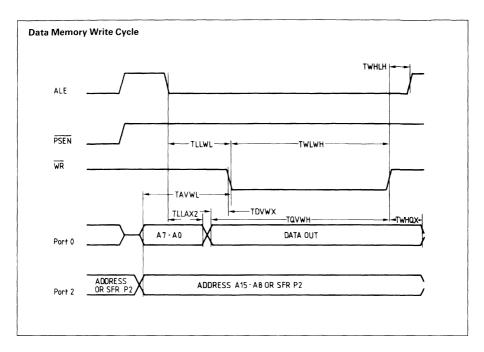
- 2.0

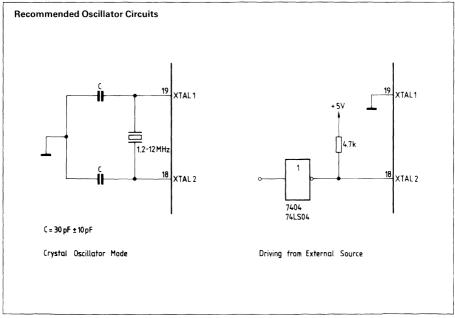
AC testing inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0". For timing purposes, the float state is defined as the point where a P0 pin sinks 3.2 mA or sources 400 μ A at the voltage test levels.

Waveforms





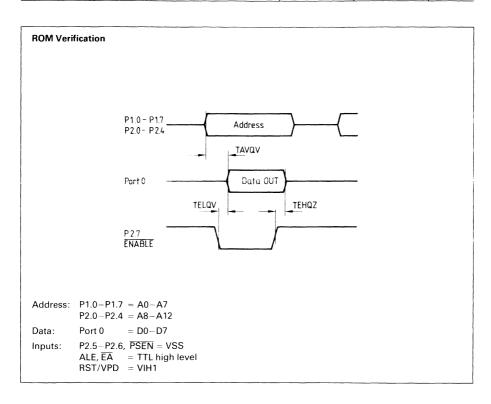




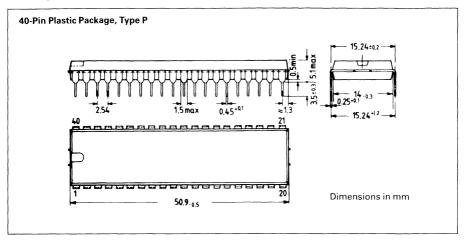
ROM Verification Characteristics

 $TA = 25^{\circ}C \pm 5^{\circ}C$; $VCC = 5V \pm 10\%$; VSS = 0V

Symbol Parameter			Limit Values	
		min.	max.	
VDVAT	Address to Valid Data			
TELQV	ENABLE to Valid Data		48 TCLCL	ns
TEHQZ	Data Float after ENABLE	0		
1/TCLCL	Oscillator Frequency	4	6	MHz



Package Outline



Ordering Information

Туре	Description	Ordering Code
	8-bit single-chip microcontroller	
SAB 8052A-P-T40/85	with mask-programmable ROM (plastic)	Q 67120-C247
SAB 8052A-P-T40/100	with mask-programmable ROM (plastic)	Q 67120-C248
SAB 8032A-P-T40/85	for external memory (plastic)	Q67120-C235
SAB 8032A-P-T40/100	for external memory (plastic)	Q67120-C239

Preliminary

SAB 8035/8048 8-Bit Single-Chip Microcontroller

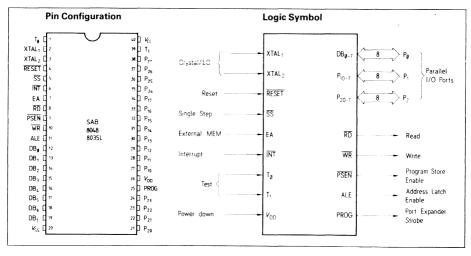
Extended Temperature Range: -40 to + 85°C -40 to +110°C

SAB 8048-P-T40/85 SAB 8048-P-T40/110 SAB 8035L-P-T40/85 Mask Programmable ROM Mask Programmable ROM

SAB 8035L-P-T40/85 External ROM

• 8-Bit CPU, ROM, RAM, I/O in Single Package

- 8-Bit Internal Timer/Event Counter
- Instructions 1 or 2 Cycles, 2.5 us or 5.0 us Cycle Time
- 96 Instructions: 70% Single Byte
- Compatible with SAB 8080/8085 Peripherals
- 1K×8 ROM 64×8 RAM 27 I/O Lines
- 2 Single Level Interrupts: Internal Timer/Counter and External
- Single 5V Supply
- Power Down Mode: Standby Current for Internal RAM 15mA



The SAB 8048/8035L are 8-Bit Single-Chip-Microcomputers implemented in $+5\,\text{Volts}$, depletion load, N channel, silicon gate Siemens MYMOS technology packaged in a 40 pin package. It is 100% compatible with the industry standard 8048.

The SAB 8048 contains a 1K \times 8 program memory, a 64 \times 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on board oscillator and clock circuits. For systems that require extra capability, the SAB 8048 can be expanded using standard memories and SAB 8080/8085 peripherals. The

SAB 8035L is the equivalent of an SAB 8048 without program memory and can be used with external ROM and RAM.

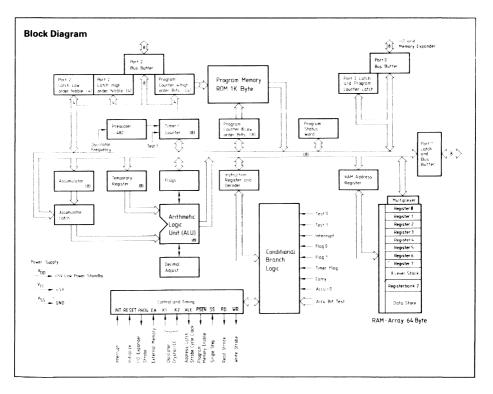
These microcomputers are designed to be efficient controllers as well as arithmetic processors. They have extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single bit instructions and no instructions over 2 bytes in length.

3.83

Pin Description

Symbol	Pin No.	1/0	Function
Tø	1	1/0	Input pin testable using the conditional transfer instructions JT0 and JNT0. T_0 can be designated as a clock output using ENT0 CLK instruction
XTAL _{1,} XTAL ₂	2,3	0	Inputs for internal oscillator with crystal or external source (non TTL VIH)
RESET	4	1	Input which is used to initialize the processor (Activ low). Also used during power down (non TTL VIH)
SS	5	I	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction (active low)
INT	6	1	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction (active low)
EA	7	1	External access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification (active high)
RD	8	0	Output strobe activated during a BUS read. Can be used to enable data on the bus from an external device. Used as a read strobe to external data memory (active low)
PSEN	9	0	Program store enable. This output occurs only during a fetch to external program memory (active low)
WR	10	0	Output strobe during a bus write (active low). Used as a write strobe to external data memory
ALE	11	0	Address latch enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory
DB ₀ –DB ₇	12-19	1/0	Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of PSEN. Also contains the address and data during an external RAM data store instruction, under control of ALE, RD, and WR

Symbol	Pin No.	1/0	Function
P ₂₀ -P ₂₇	21-24 35-38	1/0	8-Bit quasi-bidirectional I/O-Port. $P_{20}-P_{23} \ contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for SAB 8243$
PROG	25	0	Output strobe for SAB 8243 I/O expander
P ₁₀ -P ₁₇	27-34	I/O	8-Bit quasi-bidirectional I/O-Port.
Т,	39	I	Input pin testable using the JT1 and JTN1 instructions. Can be designated the timer/counter input using the STRT CNT instruction
V _{cc}	40		5V Main power supply
V _{DD}	26		5V Power Down Voltage
V _{ss}	20		GND potential



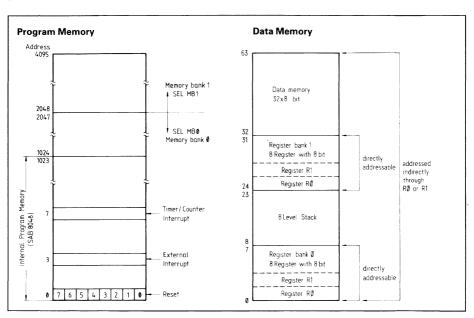
Functional Description

Program Memory

Program memory of SAB 8048 consists of 1024 words 8-bit wide which are adressed by the program counter. Program memory can be used to store constants as well as program instructions. Three locations in Program Memory are reserved to service the two Interrupts (Timer/Counter and external) and the Reset.

Data Memory

Data memory of SAB 8048 is organized as 64 words, 8-bits wide containing the stack and 2 register banks of 8 directly addressable registers.



Timer/Counter

The internal 8-bit binary up-counter can be used to count external events and to generate accurate time delays. The increment from maximum count FF to 00 (overflow) results in the setting of an overflow flag flip-flop and in the generation of interrupt request if the interrupt is enabled.

Depending upon the type of START-Instruction used the timer/counter is clocked by the oscillator frequency: 480 or an external clock.

The timer/counter is presettable and readable with two MOV instructions.

Interrupts

The two interrupts (timer/counter and external) have the same priority. They can be enabled or disabled under program control.

Input/Output

The SAB 8048 has 27 lines which can be used for I/O functions. These lines are grouped as three 8-bit ports and three test inputs.

Port 1 and 2 are called quasi-bidirectional because each line can serve as an input, an output, or both. Port \emptyset is a true bidirectional port with associated input and output strobes. Input and output lines on this port cannot be mixed however.

With 4 control and strobe lines, port 0 can be used as a bidirectional bus port to interface external memory and I/O devices. The three pins T0, T1, and \overline{INT} serve as inputs and are testable with conditional jump instructions.

Symbols and Abbreviations used

Α	Accumulator
AC	Auxiliary Carry
Adr	12-Bit Program Memory Address
An	Accumulator Bit n
BS	Bank Switch
BUS	Bus Port
CY	Carry
CLK	Clock
CNT	Event Counter
Data	8-Bit Number or Expression
DBF	Memory Bank Flip-Flop
FØ, F1	Flag 0, 1
INT	Interrupt
PC	Program Counter
PCn	Program Counter Bit n
Рр	Port 4-7 (for I/O-Extension with SAB 8243)
Pr	Port 1 or Port 2
PSW	Program Status Word
Rn	Register Bit n
Rr	Register Ø−7
SP	Stackpointer
T	Timer
TF	Timer Flag
TØ, T1	Test Ø, Test 1
X	Mnemonic for External RAM
#	Immediate Data Prefix
@	Indirect Address Prefix
Page	Memory Block of 256 Byte
()	Contents
→	is moved to
↔	is exchanged with
^	logical UND
V	logical OR
∀	logical EXCLUSIV OR
_	Complement

Instruction Set

Mnemo	onic	Function	Description	Hex Code	Flag	Bytes	Cycles
Accum	ulator and R	egister Move Instru	ctions			•	
MOV	A, Rr	(Rr) → A	Move Register Contents	F8-FF		1	1
MOV	A, @ Rr	$((Rr)) \rightarrow A$	Move Data Memory Contents to Accumulator	FØF1		1	1
MOV	A, # Data	Data → A	Move Immediate Data Data to Accumulator	23		2	2
MOV	A, PSW	(PSW) → A	Move PSW Contents to Accumulator	C7		1	1
MOV	PSW, A	(A) → PSW	Move Accumulator Contents to PSW	D7	CY, AC	1	1
MOV	Rr, A	$(A) \rightarrow Rr$	Move AccumulatorContents to Register	A8-AF		1	1
MOV	@ Rr, A	$(A) \rightarrow (Rr)$	Move Accumulator Contents to Data Memory	AØ-A1		1	1
MOV	Rr, # Data	Data → Rr	Move Immediate Data to Register	B8-BF		2	2
MOV	@ Rr, # Data	Data → (Rr)	Move Immediate Data to Data Memory	BØ-B1		2	2
MOVX	A, @ Rr	$((Rr)) \rightarrow A$	Move External-Data-Memory Contents to Accumulator	80-81		1	2
MOVX	@ Rr, A	$(A) \rightarrow (Rr)$	Move Accumulator Contents to External Data Memory	90-91		1	2
XCH	A, Rr	(Rr) ↔ (A)	Exchange Accumulator and Register Contents	28-2F		1	1
XCH	A, @ Rr	((Rr)) ↔ (A)	Exchange Accumulator and Data Memory Contents	20-21		1	1
XCHD	A, @ Rr	$((Rr))_{0-3} \leftrightarrow (A)_{0-3}$	Exchange Accumulator and Data Memory 4-Bit Data	30-31		1	1
MOVP3	3 А, @ А	$ \begin{array}{l} (PC) \ save \\ (A) \rightarrow PC_{\emptyset^{-7}} \\ 011 \rightarrow PC_{B-11} \\ ((PC)) \rightarrow A \\ PC \ restore \end{array} $	Move Page 3 Data to Accumulator	E3		1	2
MOVP	А, @ А	(PC) save $(A) \rightarrow PC_{0-7}$ $((PC)) \rightarrow A$ PC restore	Move Current Page Data to Accumulator	А3		1	2
SWAP	Α	$(A)_{\emptyset-3} \leftrightarrow (A)_{4-7}$	Swap Nibbles within Accumulator	47		1	1
Timer/	Counter Mov	ve Instructions					
MOV	Α, Τ	(T) → A	Move Timer/Counter Contents to Accumulator	42		1	1
MOV	T, A	(A) → T	Move Accumulator Contents to Timer/Counter	62		1	1

Mnem	onic	Function	Description	Hex Code	Flag	Bytes	Cycles
Port M	ove Instructi	ons					
IN	A, Pr	(Pr) → A	Input Port 1 or 2 Data to Accumulator	Ø9-ØA		1	2
OUTL	Pr, A	(A) → Pr	Output Accumulator Data to Port 1 or 2	39-3A		1	2
ANL	Pr, # Data	(Pr) ∧ Data → Pr	Logical AND Port 1–2 with Immediate Mask	99-9A		2	2
ORL	Pr, # Data	(Pr) ∨ Data → Pr	Logical OR Port 1–2 with Immediate Mask	89-8A		2	2
INS	A, BUS	(BUS) → A	Strobed Input of BUS-Data to Accumulator	Ø8		1	2
OUTL	BUS, A	(A) → BUS	Output Accumulator Data to BUS	Ø 2		1	2
ANL	BUS, # Data	(BUS) ∧ Data → BUS	Logical AND BUS with Immediate Mask	98		2	2
ORL	BUS, # Data	(BUS) ∨ Data → BUS	Logical OR BUS with Immediate Mask	88		2	2
MOVD	A, P _P	$(P_P) \to A_{0-3}$ $\emptyset \to A_{4-7}$	Move Port 4 – 7 of SAB 8243 5 to Accumulator 6 7	ØC ØD ØE ØF		1 1 1	2 2 2 2
MOVD	P _p , A	$(A)_{\emptyset-3} \rightarrow P_p$	Move Accumulator Port 4 to Port 4-7 5 of SAB 8243 6 7	3C 3D 3E 3F		1 1 1	2 2 2 2
ANLD	P _p , A	$(A)_{0-3} \wedge (P_p) \to P_p$	Logical AND Port 4 Port 4-7 of 5 SAB 8243 with 6 Accumulator Mask 7	9C 9D 9E 9F		1 1 1	2 2 2 2
ORLD	P _P , A	$(A)_{\emptyset-3} \vee (P_P) \to P_P$	Logical OR Port 4 Port 4-7 of 5 SAB 8243 with 6 Accumulator Mask 7	8C 8D 8E 8F		1 1 1	2 2 2 2
Arithm	etic Accumu	lator Instructions					
ADD	A, R,	$(A)+(R_r) \rightarrow A$	Add Register Contents to Accumulator	68-6F	AC, CY	1	1
ADD	A, @ R,	$(A)+((R_r)) \rightarrow A$	Add Data Memory Contents to Accumulator	6Ø 61	AC, CY	1	1
ADD	A, # Data	(A)+Data → A	Add Immediate Data to Accumulator	Ø3	AC, CY	2	2
ADDC	A, R,	$(A)+(R_r)+(CY) \rightarrow A$	Add Carry and Register Contents to Accumulator	78-7F	AC, CY	1	1
ADDC	A, @ R,	$(A)+((R_r))+(CY)$ $\rightarrow A$	Add Carry and Data Memory Contents to Accumulator	7Ø 71	AC, CY	1	1
ADDC	A, # Data	(A)+Data+(CY) → A	Add Carry and Immediate Data to Accumulator	13	AC, CY	2	2

Mnem	nonic	Function	Description	Hex Code	Flag	Bytes	Cycles
INC	Α	(A)+1 → A	Increment Accumulator	17		1	1
DEC	Α	(A)−1 → A	Decrement Accumulator	Ø7		1	1
DA	Α		Decimal Adjust Accumulator	57	AC, CY	1	1
Arithn	netic Registe	r Instructions					
INC	R,	$(R_r)+1 \rightarrow R_r$	Increment Register	18-1F		1	1
DEC	R,	$(R_r)-1 \rightarrow R_r$	Decrement Register	C8-CF		1	1
INC	@ R _r	$((R_r))+1 \to (R_r)$	Increment Data Memory Location	10-11		1	1
DJNZ	R _r , Adr	$(R_r)-1 \rightarrow R_r$ if $(R_r) \neq \emptyset$ Adr $\rightarrow PC_{0-7}$	Decrement Register and Test Register if Zero	E8-EF		2	2
Logica	l Accumulate	or and Register Inst	ructions				
ANL	A, R,	$(A) \wedge (R_r) \rightarrow A$	Logical AND Accumulator with Register Mask	58-5F		1	1
ANL	A, @ R _r	$(A) \wedge ((R_r)) \rightarrow A$	Logical AND Accumulator with Memory Mask	50 51		1	1
ANL	A, # Data	(A) ∧ Data → A	Logical AND Accumulator with Immediate Mask	53		2	2
ORL	A, R _r	$(A) \lor (R_r) \rightarrow A$	Logical OR Accumulator with Register Mask	48-4F		1	1
ORL	A, @ R _r	$(A) \vee ((R_r)) \to A$	Logical OR Accumulator with Memory Mask	40 41		1	1
ORL	A, # Data	(A) ∨ Data → A	Logical OR Accumulator with Immediate Mask	43		2	2
XRL	A, R,	$(A) \forall (R_r) \rightarrow A$	Logical XOR Accumulator with Register Mask	D8-DF		1	1
XRL	A, @ R,	$(A) \forall ((R_r)) \rightarrow A$	Logical XOR Accumulator with Memory Mask	DØ D1		1	1
XRL	A, # Data	(A) → Data → A	Logical XOR Accumulator with Immediate Mask	D3		2	2
CLR	Α	$\emptyset \to A$	Clear Accumulator	27		1	1
CPL	Α	$(\overline{A}) \to A$	Complement Accumulator	37		1	1
Rotate	Instructions	i					
RL	Α	$(An) \rightarrow An+1$	Rotate Accumulator Left without Carry	E7		1	1
RLC	Α	$(An) \rightarrow An+1$ $(A_7) \rightarrow CY$ $(CY) \rightarrow A_0$	Rotate Accumulator Left through Carry	F7	CY	1	1
RR	Α	$(An+1) \rightarrow An$	Rotate Accumulator Right without Carry	77		1	1
RRC	Α	$(An+1) \rightarrow An$ $(A_0) \rightarrow CY$ $(CY) \rightarrow A_7$	Rotate Accumulator Right through Carry	67	CY	1	1

Mnem	onic	Function	Description	Hex Code	Flag	Bytes	Cycles
Flag In	structions						
CLR	С	Ø → CY	Clear Carry Bit	97	CY	1	1
CPL	С	$(\overline{CY}) \to CY$	Complement Carry Bit	A7	CY	1	1
CLR	FØ	Ø → FØ	Clear FlagØ	85		1	1
CPL	FØ	$(\overline{F0}) \to F0$	Complement Flag Ø	95		1	1
CLR	F1	Ø → F1	Clear Flag 1	A 5		1	1
CPL	F1	$(\overline{F1}) \rightarrow F1$	Complement Flag 1	B5		1	1
Branci	h Instruction	s					
JMP	Adr	$\begin{array}{c} Adr_{\emptyset-7} \rightarrow PC_{\emptyset-7} \\ Adr_{B-10} \rightarrow PC_{B-10} \\ DBF \rightarrow PC_{11} \end{array}$	Direct Jump Page Ø within 2K-Block 1 2 3 4 5 6 6 7	Ø4 24 44 64 84 A4 C4 E4		2 2 2 2 2 2 2 2 2	2 2 2 2 2 2 2 2 2 2 2
JMPP	@ A	$((A)) \rightarrow PC_{\emptyset-7}$	Indirect Jump within Page	В3		1	2
JC	Adr	$ \begin{aligned} &\text{If (CY)} = 1\\ &\text{Adr} \rightarrow \text{PC}_{0-7} \end{aligned} $	Jump if Carry is set	F6		2	2
JNC	Adr	$ \begin{aligned} &\text{If } (CY) = \emptyset \\ &\text{Adr} \to PC_{0-7} \end{aligned} $	Jump if Carry is not set	E6		2	2
JZ	Adr	If $(A) = \emptyset$ Adr $\rightarrow PC_{0-7}$	Jump if Accumulator is Zero	C6		2	2
JNZ	Adr	If (A) $\neq \emptyset$ Adr $\rightarrow PC_{0-7}$	Jump if Accumulator is not Zero	96		2	2
JTØ	Adr	If $T\emptyset = 1$ Adr $\rightarrow PC_{0-7}$	Jump if Test Ø is High	36		2	2
JNTØ	Adr	$ \begin{aligned} &\text{If } T\emptyset = \emptyset \\ &Adr \to PC_{0-7} \end{aligned} $	Jump if Test Ø is Low	26		2	2
JT1	Adr	$ \begin{aligned} &\text{If T1 = 1} \\ &\text{Adr} \rightarrow PC_{0-7} \end{aligned} $	Jump if Test 1 is High	56		2	2
JNT1	Adr	$ \begin{aligned} &\text{If T1} = \emptyset \\ &\text{Adr} \to PC_{0-7} \end{aligned} $	Jump if Test 1 is Low	46		2	2
JFØ	Adr	If $F\emptyset = 1$ Adr $\rightarrow PC_{\emptyset-7}$	Jump if Flag ∅ is set	В6		2	2
JF1	Adr	$ \begin{aligned} \text{If F1} &= 1 \\ \text{Adr} &\to PC_{0-7} \end{aligned} $	Jump if Flag 1 is set	76		2	2
JTF	Adr	If TF = 1 Adr \rightarrow PC ₀₋₇ $\emptyset \rightarrow$ TF	Jump if Timer Flag is set	16	TF	2	2
JNI	Adr	If $\overline{INIT} = \emptyset$ Adr $\to PC_{\emptyset-7}$	Jump if Interrupt input is Low	86		2	2

SAB 8035/8048 Ext. Temp.

Mnemonic	Function	Description		Hex Code	Flag	Bytes	Cycles
JBn Adr	If Bit n = 1 Adr \rightarrow PC ₀₋₇	Jump if Accumulator Bit n is set	n = Ø 1 2 3 4 5 6 7	12 32 52 72 92 82 D2 F2		2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2

Subroutine Instructions

CALL Adr	$ \begin{array}{l} (PC_{\theta-11},PSW) \\ \rightarrow (SP) \\ (SP)+1 \rightarrow SP \\ Adr_{\theta-7} \rightarrow PC_{\theta-7} \\ Adr_{B-10} \rightarrow PC_{8-10} \\ DBF \rightarrow PC_{11} \end{array} $	Subroutine Call Page Ø 1 2 3 4 5 6 7	14 34 54 74 94 B4 D4 F4		2 2 2 2 2 2 2 2 2 2	2 2 2 2 2 2 2 2 2 2
RET	$(SP)-1 \rightarrow SP$ $((SP)) \rightarrow PC$	Return without PSW Restore	83		1	2
RETR	$ \begin{array}{c} (SP) - 1 \to SP \\ ((SP)) \to PC \\ ((SP)) \to PSW_{4-7} \end{array} $	Return with PSW Restore	93	AC, CY	1	2

Control Instructions

STRT	Т		Start Timer	55	1	1
STRT	CNT		Start Event Counter	45	1	1
STOP	TCNT		Stop Timer/Event-Counter	65	1	1
EN	TCNTI		Enable Timer/Counter Interrupt	25	1	1
DIS	TCNTI		Disable Timer/Counter Interrupt	35	1	1
EN	I		Enable External Interrupt	Ø5	1	1
DIS	1		Disable External Interrupt	15	1	1
SEL	RBØ	$\emptyset \to BS$	Select Register Bank Ø	C5	1	1
SEL	RB1	1 → BS	Select Register Bank 1	D5	1	1
SEL	MBØ	Ø → DBF	Select Memory Bank Ø	E5	1	1
SEL	MB1	1 → DBF	Select Memory Bank 1	F5	1	1
ENTØ	CLK		Enable Clock Output	75	1	1
NOP			The NOP Instruction	ØØ	1	1

Absolute Maximum Ratings*

Ambient Temperature Under Bias -40 to + 85°C for T40/85 -40 to +110°C for T40/110

Storage Temperature $-65 \text{ to} + 150^{\circ}\text{C}$

Voltage On Any Pin With Respect to Ground $-0.5 \text{ to} + 7 \text{ V}$ Power Dissipation 1.5 W

D.C. and Operating Characteristics

 $V_{\rm CC} = V_{\rm DD} = +5 \mbox{V} \pm 10\%$; $V_{\rm SS} = 0 \mbox{V}$; $T_{\rm A} - 40 \mbox{ to} + 85 \mbox{C}$ for T40/85 $T_{\rm A} - 40 \mbox{ to} + 110 \mbox{ C}$ for T40/110

Symbol	Parameter	L	imit va	lues	Unit	Test Conditions
		min.	typ.	max.		
V _{IL}	Input Low Voltage (All Except RESET, XTAL1, XTAL2)	0.5		0.8		
V _{IL1}	Input Low Voltage (RESET, XTAL1, XTAL2)	-0.5		0.6		
V _{IH}	Input High Voltage (All Except XTAL1, XTAL2, RESET)	2.0				
V _{IH1}	Input High Voltage (XTAL1, XTAL2, RESET)	3.8		V _{cc}		
V _{OL}	Output Low Voltage (BUS)					$I_{OL} = 2.0 \text{ mA}$
V _{OL1}	Output Low Voltage (RD, WR, PSEN, ALE)			0.45	v	I _{OL} = 1.8 mA
V _{OL2}	Output Low Voltage (PROG)					$I_{\rm OL}=1.0~{\rm mA}$
V _{OL3}	Output Low Voltage (All Other Outputs)		_			$I_{\rm OL}=1.6~{\rm mA}$
V _{OH}	Output High Voltage (BUS)					$I_{OH} = 400 \mu\text{A}$
V _{OH1}	Output High Voltage (RD, WR, PSEN, ALE)	2.4		_		$I_{OH} = 100 \mu\text{A}$
V _{OH2}	Output High Voltage (All Other Outputs)					$I_{OH}=40~\mu A$
I _{L1}	Input Leakage Current (T1, INT)			±10		$V_{\rm SS} \leq V_{\rm IN} \leq V_{\rm CC}$
I _{LI1}	Input Leakage Current (P10–P17, P20–P27, EA, SS)			-500	μΑ	
I _{LO}	Output Leakage Current (BUS, TO) (High Impedance State)]-		±10		$V_{\rm SS} + 0.45 \le V_{\rm IN} \le V_{\rm CC}$
I _{DD}	V _{DD} Supply Current		5	15		
$I_{\text{DD}} + I_{\text{CC}}$	Total Supply Current		60	135	mA	_

^{*)} Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

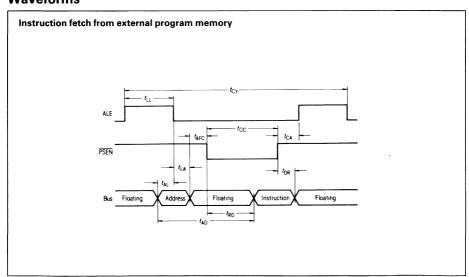
A.C. Characteristics

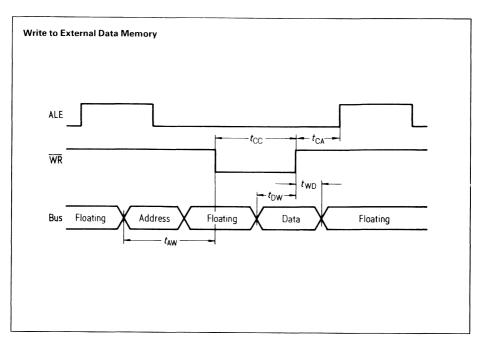
$$V_{\rm CC} = V_{\rm DD} = +5 \rm V \pm 10\%$$
; $V_{\rm SS} = 0 \rm V$; $T_{\rm A} - 40 \, \rm to + 85^{\circ} C$ for T40/85 $T_{\rm A} - 40 \, \rm to + 110^{\circ} C$ for T40/110

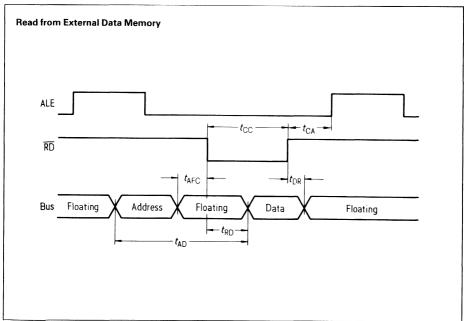
Symbol	Parameter	Li	Limit Values		Test Conditions *		
		min.	max.				
t _{LL}	ALE Pulse Width	400					
t _{AL}	Address Setup to ALE	120					
t _{LA}	Address Hold from ALE	80					
$t_{\rm CC}$	Control Pulse Width (PSEN, RD, WR)	700	-	ns	-		
t_{DW}	Data Setup before WR	500					
t_{WD}	Data Hold After WR	120			$C_L = 20 \text{ pF}$		
$\overline{t_{CY}}$	Cycle Time	2.5	15.0	μs	6 MHz Crystal = 2.5 μs		
t _{DR}	Data Hold	0	200				
t_{RD}	PSEN, RD to Data In	-	500				
t _{AW}	Address Setup to WR	230	-				
t_{AD}	Adsress Setup to Data In	-	950	ns	_		
t _{AFC}	Address Float to RD, PSEN	0	_				
t_{CA}	Control Pulse to ALE	10					

^{*} Control outputs: $C_L = 80 \text{ pF}$; BUS outputs: $C_L = 150 \text{ pF}$

Waveforms



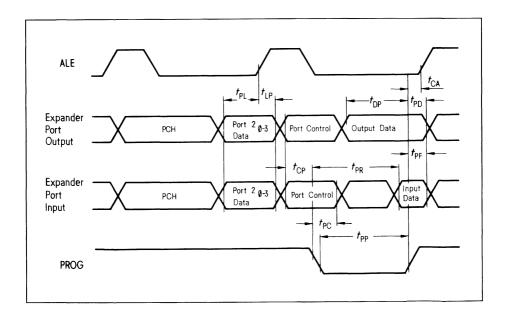




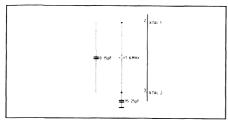
A.C. Characteristics (Port 2 Timing)

$$V_{\rm CC} = V_{\rm DD} = +5 \rm V \pm 10\% \, ; \, V_{\rm SS} = 0 \rm V ; \, T_A - 40 \, to + \, 85^{\circ} C \, for \, T40/85 \\ T_A - 40 \, to + 110^{\circ} C \, for \, T40/110 \, column{2}{c}$$

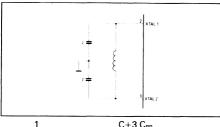
Symbol	Parameter	Limi	Limit Values		
		min.	max.		
t _{CP}	Port Control Setup Before Falling Edge of PROG	110			
t _{PC}	Port Control Hold After Falling Edge of PROG	100			
t _{PR}	PROG to Time P2 Input Must Be Valid	_	810		
t _{PF}	Input Data Hold Time	0	150	ns	
t _{DP}	Output Data Setup Time	250			
t _{PD}	Output Data Hold Time	65	1		
t _{PP}	PROG Pulse Width	1200	_		
t _{PL}	Port 2 I/O Data Setup	350			
t _{LP}	Port 2 I/O Data Hold	150	1		



Connecting the Oscillator Inputs

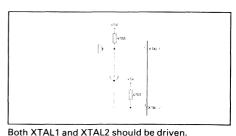


Crystal series resistance should be < 75 Ω at 6 MHz and < 180 Ω at 3.6 MHz.



 $f = \frac{1}{2 \pi \sqrt{LC'}} \qquad C' =$

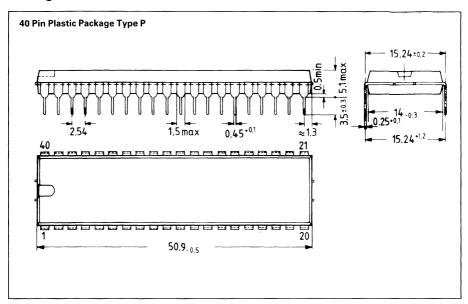
 $C_{pp} \approx 5 - 10 \, pF$ pin-to-pin capacitance



Resistors to V_{CC} are needed to ensure $V_{\text{IH}} = 3.8\,\text{V}$ if TTL circuitry is used.

XTAL1 and XTAL2 must be high 35-65% of the period.

Package Outline



Ordering Information

Туре	Description	Ordering code
SAB 8048-P-T40/85 SAB 8048-P-T40/110	8 Bit Single-Chip-Microcomputer with maskprogrammable ROM (Plastic) with maskprogrammable ROM (Plastic)	Q67120-C133 Q67120-C162
SAB 8035L-P-T40/85	with external ROM (Plastic)	Q67120-C140

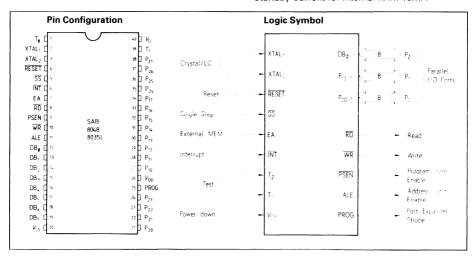
SAB 8035/8048 8-Bit Single-Chip Microcontroller

SAB 8048 Mask Programmable ROM

- 8-Bit CPU, ROM, RAM, I/O in Single Package
- 8-Bit Internal Timer/Event Counter
- Instructions 1 or 2 Cycles, 2.5 μs or 5.0 μs Cycle Time
- 96 Instructions: 70% Single Byte
- Compatible with SAB 8080/8085 Peripherals

SAB 8035L External ROM/EPROM

- 1K×8 ROM 64×8 RAM 27 I/O Lines
- 2 Single Level Interrupts: Internal Timer/Counter and External
- Single 5V Supply
- Power Down Mode: Standby Current for Internal RAM 15mA



The SAB 8048/8035L are 8-Bit Single-Chip-Micro-computers implemented in +5 Volts, depletion load, N channel, silicon gate Siemens MYMOS technology packaged in a 40 pin package. It is 100% compatible with the industry standard 8048.

The SAB 8048 contains a 1 K \times 8 program memory, a 64 \times 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on board oscillator and clock circuits. For systems that require extra capability, the SAB 8048 can be expanded using standard memories and SAB 8080/8085 peripherals. The SAB 8035L is the equivalent of an SAB 8048 without program memory and can be used with external ROM and RAM. To reduce development problems to a minimum and provide maximum flexibility,

two pin-compatible versions of this single component microcomputer exist: the SAB 8048 with factory-programmed mask ROM program memory for low cost, high volume production, and the SAB 8035 without program memory for use with external program memories.

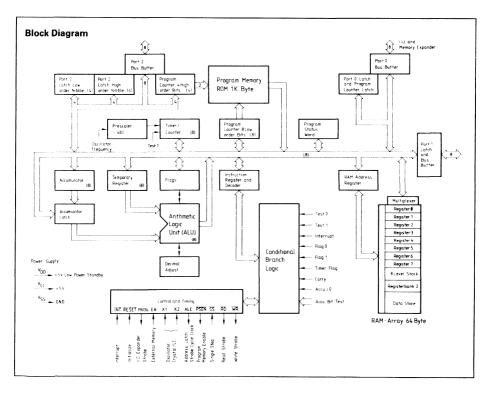
These microcomputers are designed to be efficient controllers as well as arithmetic processors. They have extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single bit instructions and no instructions over 2 bytes in length.

9.82

Pin Description

Symbol	Pin No.	1/0	Function
Tø	1	I/O	Input pin testable using the conditional transfer instructions JTØ and JNTØ. To can be designated as a clock output using ENTØ CLK instruction
XTAL ₁ , XTAL ₂	2,3	I O	Inputs for internal oscillator with crystal or external source (non TTL VIH)
RESET	4	I	Input which is used to initialize the processor (Activ low). Also used during power down (non TTL VIH)
SS	5	I	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction (active low)
INT	6	l	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction (active low)
EA	7	1	External access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification (active high)
RD	8	0	Output strobe activated during a BUS read. Can be used to enable data on the bus from an external device. Used as a read strobe to external data memory (active low)
PSEN	9	0	Program store enable. This output occurs only during a fetch to external program memory (active low)
WR	10	0	Output strobe during a bus write (active low). Used as a write strobe to external data memory
ALE	11	0	Address latch enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory
DB ₀ –DB ₇	12-19	I/O	Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of PSEN. Also contains the address and data during an external RAM data store instruction, under control of ALE, RD, and WR

Symbol	Pin No.	1/0	Function
P ₂₀ -P ₂₇	21-24 35-38	1/0	8-Bit quasi-bidirectional I/O-Port. $P_{20}-P_{23}$ contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for SAB 8243
PROG	25	0	Output strobe for SAB 8243 I/O expander
P ₁₀ -P ₁₇	27-34	1/0	8-Bit quasi-bidirectional I/O-Port.
T ₁	39	ı	Input pin testable using the JT1, and JTN1 instructions. Can be designated the timer/counter input using the STRT CNT instruction
V _{cc}	40		5V Main power supply
V_{DD}	26		5V Power Down Voltage
V _{SS}	20		GND potential



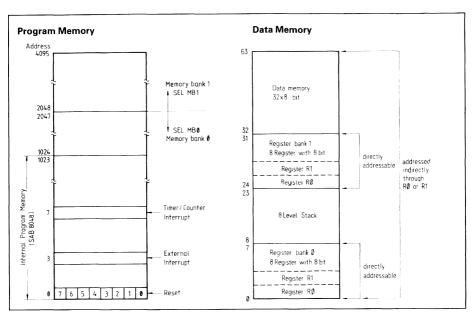
Functional Description

Program Memory

Program memory of SAB 8048 consists of 1024 words 8-bit wide which are adressed by the program counter. Program memory can be used to store constants as well as program instructions. Three locations in Program Memory are reserved to service the two Interrupts (Timer/Counter and external) and the Reset.

Data Memory

Data memory of SAB 8048 is organized as 64 words, 8-bits wide containing the stack and 2 register banks of 8 directly addressable registers.



Timer/Counter

The internal 8-bit binary up-counter can be used to count external events and to generate accurate time delays. The increment from maximum count FF to 00 (overflow) results in the setting of an overflow flag flip-flop and in the generation of interrupt request if the interrupt is enabled.

Depending upon the type of START-Instruction used the timer/counter is clocked by the oscillator frequency: 480 or an external clock.

The timer/counter is presettable and readable with two MOV instructions.

Interrupts

The two interrupts (timer/counter an external) have the same priority. They can be enabled or disabled under program control.

Input/Output

The SAB 8048 has 27 lines which can be used for I/O functions. These lines are grouped as three 8-bit ports and three test inputs.

Port 1 and 2 are called quasi-bidirectional because each line can serve as an input, an output, or both. Port \emptyset is a true bidirectional port with associated input and output strobes. Input and output lines on this port cannot be mixed however.

With 4 control and strobe lines, port 0 can be used as a bidirectional bus port to interface external memory and I/O devices. The three pins T0, T1, and INT serve as inputs and are testable with conditional jump instructions.

Symbols and Abbreviations used

A	Accumulator
AC	Auxiliary Carry
Adr	12-Bit Program Memory Address
An	Accumulator Bit n
BS	Bank Switch
BUS	Bus Port
CY	Carry
CLK	Clock
CNT	Event Counter
Data	8-Bit Number or Expression
DBF	Memory Bank Flip-Flop
FØ, F1	Flag Ø, 1
INT	Interrupt
PC	Program Counter
PCn	Program Counter Bit n
Рр	Port 4-7 (for I/O-Extension with SAB 8243)
Pr	Port 1 or Port 2
PSW	Program Status Word
Rn	Register Bit n
Rr	Register Ø−7
SP	Stackpointer
Т	Timer
TF	Timer Flag
TØ, T1	Test Ø, Test 1
X	Mnemonic for External RAM
#	Immediate Data Prefix
@	Indirect Address Prefix
Page	Memory Block of 256 Byte
()	Contents
→	is moved to
↔	is exchanged with
٨	logical UND
V	logical OR
∀	logical EXCLUSIV OR
_	Complement

Instruction Set

				Ι	Ι	Γ	T
Mnemo	onic	Function	Description	Hex Code	Flag	Bytes	Cycles
Accum	ulator and R	egister Move Instru	ctions				
MOV	A, Rr	(Rr) → A	Move Register Contents	F8-FF		1	1
MOV	A, @ Rr	$((Rr)) \rightarrow A$	Move Data Memory Contents to Accumulator	FØ-F1		1	1
MOV	A, # Data	Data → A	Move Immediate Data Data to Accumulator	23		2	2
MOV	A, PSW	$(PSW) \rightarrow A$	Move PSW Contents to Accumulator	C7		1	1
MOV	PSW, A	(A) → PSW	Move Accumulator Contents to PSW	D7	CY, AC	1	1
MOV	Rr, A	$(A) \rightarrow Rr$	Move Accumulator Contents to Register	A8-AF		1	1
MOV	@ Rr, A	$(A) \rightarrow (Rr)$	Move Accumulator Contents to Data Memory	AØ-A1		1	1
MOV	Rr, # Data	Data → Rr	Move Immediate Data to Register	B8-BF		2	2
MOV	@ Rr, # Data	Data → (Rr)	Move Immediate Data to Data Memory	BØ-B1		2	2
MOVX	A, @ Rr	$((Rr)) \rightarrow A$	Move External-Data-Memory Contents to Accumulator	8Ø-81		1	2
MOVX	@ Rr, A	$(A) \rightarrow (Rr)$	Move Accumulator Contents to External Data Memory	90-91		1	2
XCH	A, Rr	(Rr) ↔ (A)	Exchange Accumulator and Register Contents	28-2F		1	1
XCH	A, @ Rr	((Rr)) ↔ (A)	Exchange Accumulator and Data Memory Contents	20-21		1	1
XCHD	A, @ Rr	$((Rr))_{\emptyset-3} \leftrightarrow (A)_{\emptyset-3}$	Exchange Accumulator and Data Memory 4-Bit Data	30-31		1	1
MOVP3	3 A, @ A	$ \begin{array}{l} (PC) \ save \\ (A) \rightarrow PC_{0-7} \\ 011 \rightarrow PC_{8-11} \\ ((PC)) \rightarrow A \\ PC \ restore \end{array} $	Move Page 3 Data to Accumulator	E3		1	2
MOVP	А, @ А	(PC) save $(A) \rightarrow PC_{0-7}$ $((PC)) \rightarrow A$ PC restore	Move Current Page Data to Accumulator	А3		1	2
SWAP	Α	$(A)_{0-3} \leftrightarrow (A)_{4-7}$	Swap Nibbles within Accumulator	47		1	1
Timer/	Counter Mov	ve Instructions					
MOV	A, T	(T) → A	Move Timer/Counter Contents to Accumulator	42		1	1
MOV	T, A	(A) → T	Move Accumulator Contents to Timer/Counter	62		1	1

Mnemo	onic	Function	Description	Hex Code	Flag	Bytes	Cycles
Port M	ove Instructi	ons					
IN	A, Pr	(Pr) → A	Input Port 1 or 2 Data to Accumulator	Ø9-ØA		1	2
OUTL	Pr, A	(A) → Pr	Output Accumulator Data to Port 1 or 2	39-3A		1	2
ANL	Pr, # Data	(Pr) ∧ Data → Pr	Logical AND Port 1–2 with Immediate Mask	99-9A		2	2
ORL	Pr, # Data	(Pr) ∨ Data → Pr	Logical OR Port 1–2 with Immediate Mask	89-8A		2	2
INS	A, BUS	(BUS) → A	Strobed Input of BUS-Data to Accumulator	Ø8		1	2
OUTL	BUS, A	(A) → BUS	Output Accumulator Data to BUS	Ø 2		1	2
ANL	BUS, # Data	(BUS) ∧ Data → BUS	Logical AND BUS with Immediate Mask	98		2	2
ORL	BUS, # Data	(BUS) ∨ Data → BUS	Logical OR BUS with Immediate Mask	88		2	2
MOVD	A, P _P	$ \begin{pmatrix} (P_p) \to A_{0-3} \\ 0 \to A_{4-7} \end{pmatrix} $	Move Port 4-7 Port 4 of SAB 8243 5 to Accumulator 6 7	ØC ØD ØE ØF		1 1 1	2 2 2 2
MOVD	P _p , A	$(A)_{0-3} \rightarrow P_p$	Move Accumulator to Port 4 to Port 4-7 5 of SAB 8243 6 7	3C 3D 3E 3F		1 1 1	2 2 2 2
ANLD	P _p , A	$(A)_{\emptyset-3} \wedge (P_p) \to P_p$	Logical AND Port 4 Port 4–7 of 5 SAB 8243 with 6 Accumulator Mask 7	9C 9D 9E 9F		1 1 1	2 2 2 2
ORLD	P _P , A	$(A)_{\emptyset-3} \vee (P_P) \to P_P$	Logical OR Port 4 Port 4-7 of 5 SAB 8243 with 6 Accumulator Mask 7	8C 8D 8E 8F		1 1 1	2 2 2 2
Arithm	etic Accumu	lator Instructions					
ADD	A, R _r	$(A)+(R_r) \rightarrow A$	Add Register Contents to Accumulator	68-6F	AC, CY	1	1
ADD	A, @ R,	$(A)+((R_r))\to A$	Add Data Memory Contents to Accumulator	60 61	AC, CY	1	1
ADD	A, # Data	(A)+Data → A	Add Immediate Data to Accumulator	Ø3	AC, CY	2	2
ADDC	A, R,	$(A)+(R_r)+(CY) \rightarrow A$	Add Carry and Register Contents to Accumulator	78-7F	AC, CY	1	1
ADDC	A, @ R,	$(A)+((R_r))+(CY)$ $\rightarrow A$	Add Carry and Data Memory Contents to Accumulator	7Ø 71	AC, CY	1	1
ADDC	A, # Data	(A)+Data+(CY) → A	Add Carry and Immediate Data to Accumulator	13	AC, CY	2	2

Mnemonics © Intel Corporation, USA.

							
Mnem	ionic	Function	Description	Hex Code	Flag	Bytes	Cycles
INC	Α	$(A)+1 \rightarrow A$	Increment Accumulator	17		1	1
DEC	А	(A)−1 → A	Decrement Accumulator	Ø 7		1	1
DA	Α		Decimal Adjust Accumulator	57	AC, CY	1	1
Arithn	netic Registe	r Instructions					
INC	R,	$(R_r)+1 \rightarrow R_r$	Increment Register	18-1F		1	1
DEC	R,	$(R_r)-1 \rightarrow R_r$	Decrement Register	C8-CF		1	1
INC	@ R,	$((R_r))+1 \to (R_r)$	increment Data Memory Location	10-11		1	1
DJNZ	R _r , Adr	$(R_r)-1 \rightarrow R_r$ if $(R_r) \neq \emptyset$ Adr $\rightarrow PC_{\emptyset-7}$	Decrement Register and Test Register if Zero	E8-EF		2	2
Logica	I Accumulate	or and Register Inst	ructions				
ANL	A, R _r	$(A) \wedge (R_r) \rightarrow A$	Logical AND Accumulator with Register Mask	58-5F		1	1
ANL	A, @ R,	$(A) \wedge ((R_r)) \rightarrow A$	Logical AND Accumulator with Memory Mask	5Ø 51		1	1
ANL	A, # Data	(A) ∧ Data → A	Logical AND Accumulator with Immediate Mask	53		2	2
ORL	A, R,	$(A) \vee (R_r) \rightarrow A$	Logical OR Accumulator with Register Mask	48-4F		1	1
ORL	A, @ R _r	$(A) \lor ((R_r)) \to A$	Logical OR Accumulator with Memory Mask	40 41		1	1
ORL	A, # Data	(A) ∨ Data → A	Logical OR Accumulator with Immediate Mask	43		2	2
XRL	A, R,	$(A) \forall (R_r) \rightarrow A$	Logical XOR Accumulator with Register Mask	D8-DF		1	1
XRL	A, @ R,	$(A) \forall ((R_r)) \rightarrow A$	Logical XOR Accumulator with Memory Mask	DØ D1		1	1
XRL	A, # Data	(A) → Data → A	Logical XOR Accumulator with Immediate Mask	D3		2	2
CLR	Α	$\emptyset \to A$	Clear Accumulator	27		1	1
CPL	Α	$(\overline{A}) \to A$	Complement Accumulator	37		1	1
Rotate	Instructions	•					
RL	Α	$(An) \rightarrow An+1$	Rotate Accumulator Left without Carry	E7		1	1
RLC	А	$(An) \rightarrow An+1$ $(A_7) \rightarrow CY$ $(CY) \rightarrow A_0$	Rotate Accumulator Left through Carry	F7	CY	1	1
RR	Α	(An+1) → An	Rotate Accumulator Right without Carry	77		1	1
RRC	Α	$(An+1) \rightarrow An$ $(A_0) \rightarrow CY$ $(CY) \rightarrow A_7$	Rotate Accumulator Right through Carry	67	CY	1	1

Mnem	nonic	Function	Description	Hex Code	Flag	Bytes	Cycles
Flag Ir	nstructions						
CLR	С	Ø → CY	Clear Carry Bit	97	CY	1	1
CPL	С	$(\overline{CY}) \to CY$	Complement Carry Bit	A7	CY	1	1
CLR	FØ	Ø → FØ	Clear FlagØ	85		1	1
CPL	FØ	$(\overline{F0}) \to F0$	Complement Flag Ø	95		1	1
CLR	F1	Ø → F1	Clear Flag 1	A5		1	1
CPL	F1	(F1) → F1	Complement Flag 1	B5		1	1
Branc	h Instructio	ens					
JMP	Adr	$\begin{array}{c} Adr_{\theta-7} \rightarrow PC_{\theta-7} \\ Adr_{\theta-10} \rightarrow PC_{\theta-10} \\ DBF \rightarrow PC_{11} \end{array}$	Direct Jump Page Ø within 2K-Block 1 2 3 4 5 6 6 7	Ø4 24 44 64 84 A4 C4 E4		2 2 2 2 2 2 2 2 2 2	2 2 2 2 2 2 2 2 2 2
JMPP	@ A	$((A)) \rightarrow PC_{0-7}$	Indirect Jump within Page	В3		1	2
JC	Adr	If $(CY) = 1$ Adr $\rightarrow PC_{0-7}$	Jump if Carry is set	F6		2	2
JNC	Adr	$ \begin{aligned} &\text{If } (CY) = \emptyset \\ &\text{Adr} \to PC_{0-7} \end{aligned} $	Jump if Carry is not set	E6		2	2
JZ	Adr	$ \begin{aligned} If(A) &= \emptyset \\ Adr &\to PC_{0-7} \end{aligned} $	Jump if Accumulator is Zero	C6		2	2
JNZ	Adr	If $(A) \neq \emptyset$ Adr $\rightarrow PC_{\emptyset-7}$	Jump if Accumulator is not Zero	96		2	2
JTØ	Adr	If $T\emptyset = 1$ Adr $\rightarrow PC_{\emptyset-7}$	Jump if Test Ø is High	36		2	2
JNTØ	Adr	If $T\emptyset = \emptyset$ Adr $\rightarrow PC_{\emptyset-7}$	Jump if Test Ø is Low	26		2	2
JT1	Adr	$ \begin{aligned} &\text{If T1} = 1\\ &\text{Adr} \to PC_{0-7} \end{aligned} $	Jump if Test 1 is High	56		2	2
JNT1	Adr	$ \begin{aligned} &\text{If T1} = \emptyset \\ &\text{Adr} \to PC_{0-7} \end{aligned} $	Jump if Test 1 is Low	46		2	2
JFØ	Adr	If $F\emptyset = 1$ Adr $\rightarrow PC_{0-7}$	Jump if Flag Ø is set	В6		2	2
JF1	Adr	$ \begin{aligned} &\text{If F1} = 1\\ &\text{Adr} \to PC_{0-7} \end{aligned} $	Jump if Flag 1 is set	76		2	2
JTF	Adr	If TF = 1 Adr \rightarrow PC ₀₋₇ $\emptyset \rightarrow$ TF	Jump if Timer Flag is set	16	TF	2	2
JNI	Adr	If $\overline{INIT} = \emptyset$ Adr $\rightarrow PC_{0-7}$	Jump if Interrupt input	86		2	2

SAB 8048

Mnemonic	Function	Description		Hex Code	Flag	Bytes	Cycles
JBn Adr	If Bit $n = 1$ Adr $\rightarrow PC_{\theta-7}$	Jump if Accumulator Bit n is set	n = Ø 1 2 3 4 5 6 7	12 32 52 72 92 B2 D2 F2		2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2

Subroutine Instructions

CALL Adr	$\begin{array}{l} (PC_{\emptyset-11},PSW) \\ \to (SP) \\ (SP) + 1 \to SP \\ Adr_{\emptyset-7} \to PC_{\emptyset-7} \\ Adr_{B-10} \to PC_{B-10} \\ DBF \to PC_{11} \end{array}$	Subroutine Call Page 0 1 2 3 4 5 6 7	14 34 54 74 94 B4 D4 F4		2 2 2 2 2 2 2 2 2 2	2 2 2 2 2 2 2 2 2 2
RET	$(SP)-1 \rightarrow SP$ $((SP)) \rightarrow PC$	Return without PSW Restore	83		1	2
RETR	$ \begin{array}{c} (SP) - 1 \to SP \\ ((SP)) \to PC \\ ((SP)) \to PSW_{4-7} \end{array} $	Return with PSW Restore	93	AC, CY	1	2

Control Instructions

STRT	Т		Start Timer	55	1	1
STRT	CNT		Start Event Counter	45	1	1
STOP	TCNT		Stop Timer/Event-Counter	65	1	1
EN	TCNTI		Enable Timer/Counter Interrupt	25	1	1
DIS	TCNTI		Disable Timer/Counter Interrupt	35	1	1
EN	I		Enable External Interrupt	Ø5	1	1
DIS	I		Disable External Interrupt	15	1	1
SEL	RBØ	$\emptyset \to BS$	Select Register Bank Ø	C5	1	1
SEL	RB1	1 → BS	Select Register Bank 1	D5	1	1
SEL	MBØ	$\emptyset \to DBF$	Select Memory Bank Ø	E5	1	1
SEL	MB1	1 → DBF	Select Memory Bank 1	F5	1	1
ENTØ	CLK		Enable Clock Output	75	1	1
NOP			The NOP Instruction	00	1	1

Absolute Maximum Ratings*

Ambient Temperature Under Bias $0 \text{ to} + 70^{\circ}\text{C}$ Storage Temperature $-65 \text{ to} + 150^{\circ}\text{C}$ Voltage On Any Pin With Respect to Ground -0.5 to + 7 V

to Ground -0.5 to + 7 VPower Dissipation 1.5 W

D.C. and Operating Characteristics

 $T_A = 0 - 70^{\circ}\text{C}$; $V_{CC} = V_{DD} = +5\text{V} \pm 10\%$; $V_{SS} = 0\text{V}$

Symbol	Parameter	L	imit va	lues	Unit	Test Conditions	
		min.	typ.	max.	1		
V _{IL}	Input Low Voltage (All Except RESET, XTAL1, XTAL2)	0.5		0.8			
V _{IL1}	Input Low Voltage (RESET, XTAL1, XTAL2)	-0.5		0.6		_	
V _{IH}	Input High Voltage (All Except XTAL1, XTAL2, RESET)	2.0					
V _{IH1}	Input High Voltage (XTAL1, XTAL2, RESET)	3.8		V _{cc}			
V _{OL}	Output Low Voltage (BUS)		1		1	I _{OL} = 2.0 mA	
V _{OL1}	Output Low Voltage (RD, WR, PSEN, ALE)]_		0.45	v	I _{OL} = 1.8 mA	
V _{OL2}	Output Low Voltage (PROG)]				I _{OL} = 1.0 mA	
V _{OL3}	Output Low Voltage (All Other Outputs)		-			I _{OL} = 1.6 mA	
V _{OH}	Output High Voltage (BUS)]		1	$I_{OH} = 400 \mu A$	
V _{OH1}	Output High Voltage (RD, WR, PSEN, ALE)	2.4		_		$I_{OH} = 100 \mu\text{A}$	
V _{OH2}	Output High Voltage (All Other Outputs)					$I_{OH} = 40~\muA$	
I _{L1}	Input Leakage Current (T1, INT)			±10		$V_{\rm SS} \leq V_{\rm IN} \leq V_{\rm CC}$	
I _{LI1}	Input Leakage Current (P10-P17, P20-P27, EA, SS)			-500	μΑ		
I _{LO}	Output Leakage Current (BUS, TO) (High Impedance State)	_		±10		$V_{\rm SS} + 0.45 \le V_{\rm IN} \le V_{\rm CC}$	
I_{DD}	V _{DD} Supply Current		5	15			
$I_{\text{DD}} + I_{\text{CC}}$	Total Supply Current		60	135	mA	-	

^{*)} Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

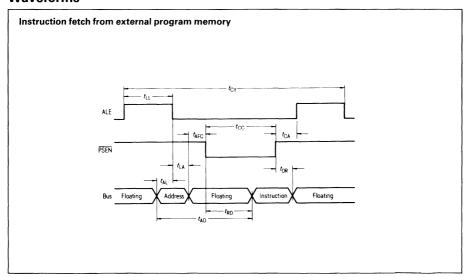
A.C. Characteristics

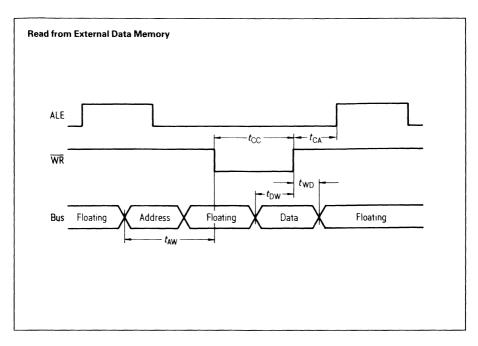
 $T_{\rm A}=0$ to 70°C; $V_{\rm CC}=V_{\rm DD}=5~{
m V}\pm10\%$; $V_{\rm SS}=0~{
m V}$

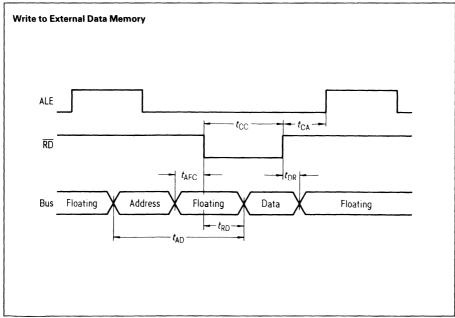
Symbol	Parameter	Li	imit Values	Unit	Test Conditions *	
		min.	max.			
t _{LL}	ALE Pulse Width	400				
t _{AL}	Address Setup to ALE	120				
t _{LA}	Address Hold from ALE	80				
t _{CC}	Control Pulse Width (PSEN, RD, WR)	700	-	ns	_	
t_{DW}	Data Setup before WR	500				
t _{wD}	Data Hold After WR	120			$C_{L} = 20 \text{ pF}$	
t _{CY}	Cycle Time	2.5	15.0	μs	6 MHz Crystal = 2.5 μs	
t _{DR}	Data Hold	0	200			
t _{RD}	PSEN, RD to Data in	-	500			
t _{AW}	Address Setup to WR	230	-			
t_{AD}	Adsress Setup to Data In	-	950	ns	_	
t _{AFC}	Address Float to RD, PSEN	0	_			
t _{CA}	Control Pulse to ALE	10				

^{*} Control outputs: $C_L = 80 \text{ pF}$; BUS outputs: $C_L = 150 \text{ pF}$

Waveforms



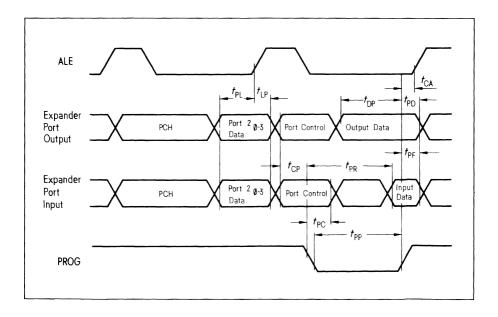




A.C. Characteristics (Port 2 Timing)

$$T_{\rm A}=0$$
 to 70°C; $V_{\rm CC}=V_{\rm DD}=5~{
m V}\pm10\%$; $V_{\rm SS}=0~{
m V}$

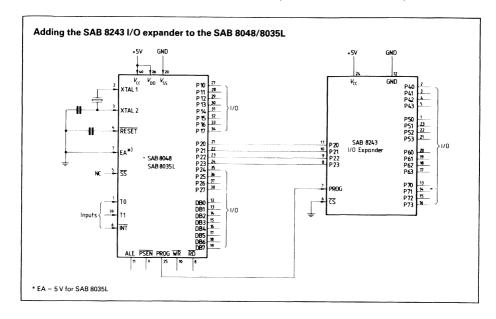
Symbol	Parameter	Limit	Values	Unit
		min.	max.	1
t_{CP}	Port Control Setup Before Falling Edge of PROG	110		
t _{PC}	Port Control Hold After Falling Edge of PROG	100]	
t _{PR}	PROG to Time P2 Input Must Be Valid	_	810	
t _{PF}	Input Data Hold Time	0	150	ns
t _{DP}	Output Data Setup Time	250		
t _{PD}	Output Data Hold Time	65	1	
t _{PP}	PROG Pulse Width	1200	_	
t _{PL}	Port 2 I/O Data Setup	350		
t _{LP}	Port 2 I/O Data Hold	150		



I/O Expansion with I/O Expander SAB 8243

The SAB 8243 is an input/output expander designed specifically for the SAB 8048 family. The I/O ports of

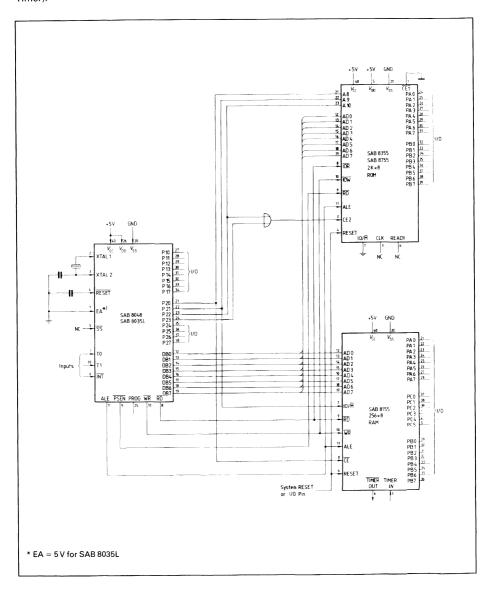
the SAB 8243 serve as a direct extension of the SAB 8048 ports and can be addressed by own instructions.



Expansion of Program Memory and Data Memory

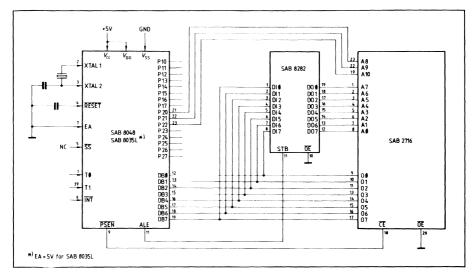
The application example shows the expansion of Program Memory, Data Memory, and I/O lines using the SAB 8355/8755 (2 K \times 8 ROM, 16 I/O lines) and the SAB 8155 (256 \times 8 RAM, 22 I/O lines, 14 Bit Timer).

The SAB 8048 Port-I/O lines are reduced from 24 to 12 by adding 38 I/O lines of the external devices.

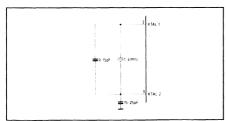


Adding External Program Memory with EPROM SAB 2716

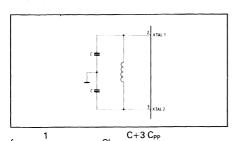
The SAB 8282 serves as a latch to separate addresses from the data bus



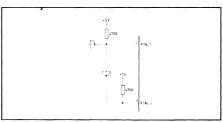
Connecting the Oscillator Inputs



Crystal series resistance should be < 75 Ω at 6 MHz and < 180 Ω at 3.6 MHz.



 $C_{pp} \approx 5-10\,pF$ pin-to-pin capacitance

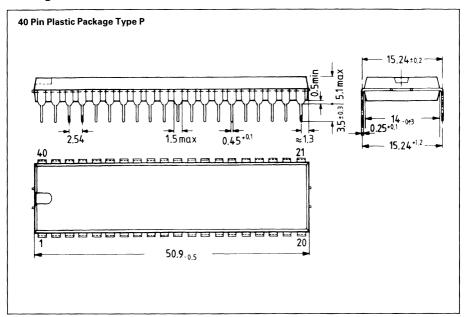


Both XTAL1 and XTAL2 should be driven.

Resistors to $V_{\rm CC}$ are needed to ensure $V_{\rm IH}=3.8\,{\rm V}$ if TTL circuitry is used.

XTAL1 and XTAL2 must be high 35-65% of the period.

Package Outline



Ordering Information

Туре	Description	Ordering code
SAB 8048-P	8 Bit Single-Chip-Microcomputer with maskprogrammable ROM (Plastic)	Q67120-C32
SAB 8035L-P	with external ROM (Plastic)	Q67120-C43



SAB 8085A 8-Bit Microprocessor

SAB 8085A (3 MHz)

- Single +5V Power Supply
- 100% Software Compatible with SAB 8080A
- 1.3 µs Instruction Cycle (SAB 8085A);
 0.8 µs (SAB 8085A-2)
- On-Chip Clock Generator (with External Crystal, LC or RC Network)
- On-Chip System Controller; Advanced Cycle Status Information Available for Large System Control

SAB 8085A-2 (5 MHz)

- Four Vectored Interrupt Inputs (one is Non-Maskable) Plus an SAB 8080A Compatible Interrupt
- Serial In/Serial Out Port
- Decimal, Binary and Double Precision Arithmetic
- Direct Addressing Capability to 64Kb of Memory
- Compatible with Industry Standard SAB 8085A

Pin Configuration				
N	A ₈ -A ₁₅ AD ₀ -AD ₇ ALE S ₀ , S ₁ , IO/M RD WR READY HOLD HLDA INTR	Address Bus Mux. Address/ Data Bus Address Latch Enable Machine Cycle Status Read Control Write Control Ready Hold Hold Acknowledge Interrupt Request	INTA RST 5.5, 6.5, 7.5 TRAP RESET IN RESET OUT X ₁ , X ₂ CLK SID SOD V _{CC} V _{SS}	Interrupt Acknowledge Restart Interrupts Trap Reset in Reset out Crystal/Clock Input Clock Output Serial Input Data Serial Output Data +5V Ground (OV)

SAB 8085A is a complete 8 bit parallel Central Processing Unit (CPU). Its instruction set is 100% software compatible with the SAB 8080A microprocessor. Its high level of system integration allows a minimum of three ICs [SAB 8085A (CPU), SAB 8156 (RAM/IO) and SAB 8355/SAB 8755A (ROM/PROM/IO)] while maintaining total system expandability. The SAB 8085A-2 is a faster version of the SAB 8085A.

The SAB 8085A incorporates all of the features that the SAB 8224 (clock generator) and SAB 8228

(system controller) provided for the SAB 8080A, thereby offering a high level of system integration.

The SAB 8085A uses a multiplexed data bus. The address is split between the 8 bit address bus and the 8 bit data bus. The on-chip address latches of SAB 8155/SAB 8156/SAB 8355/SAB 8755A memory products allow a direct interface with the SAB 8085A.

SAB 8085A is implemented in +5V advanced N-channel, silicon gate Siemens MYMOS technology.

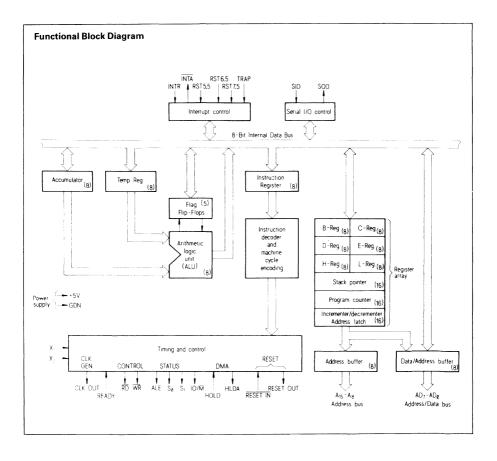
2.85

Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function
X ₁ , X ₂	1, 2	1	X_1 AND X_2 – Are connected to a crystal, LC, or RC network to drive the internal clock generator. X_1 can also be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency.
RESET OUT	3	0	RESET OUT – Reset Out indicates CPU is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.
SOD	4	0	SERIAL OUTPUT DATA LINE – The output SOD is set or reset as specified by the SIM instruction.
SID	5	I	SERIAL INPUT DATA LINE – The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.
TRAP	6	I	TRAP – Trap interrupt is a nonmaskable RESTART interrupt. It is recognized at the same time as INTR or RST 5.5-7.5. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt (see following table).
RST 5.5 RST 6.5 RST 7.5	9 8 7	1	RESTART INTERRUPTS – These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted. The priority of these interrupts is ordered as shown in the following table. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction.
INTR	10	I	INTERRUPT REQUEST – Is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an INTA will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.
INTA	11	0	INTERRUPT ACKNOWLEDGE – Is used instead of (and has the same timing as) RD during the instruction cycle after an INTR is accepted. It can be used to activate an SAB 8259A Interrupt chip or some other interrupt port.
AD ₀ -AD ₇	12-19	I/O	MULTIPLEXED ADDRESS/DATA BUS – Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.
A ₈ -A ₁₅	21-28	0	ADDRESS BUS – The most significant 8 bits of the memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.

Symbol	Number	Input (I) Output (O)	Function		
S_0 , S_1 , and IO/\overline{M}	29, 33	0	MACHINE CYCLE STATUS –		
	34		IO/M S ₁ S ₀ Status		
			0		
			* = 3-state (high impedance)		
			$X=$ unspecified S_1 can be used as an advanced R/\overline{W} status. IO/\overline{M} , S_0 and S_1 become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines.		
ALE	30	О	ADDRESS LATCH ENABLE – It occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never 3-stated.		
WR	31	0	WRITE CONTROL – A low level on WR indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of WR. 3-stated during Hold and Halt modes and during RESET.		
RD	32	0	READ CONTROL – A low level on \overline{RD} indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer, 3-stated during Hold and Halt modes and during RESET.		
READY	35	l	READY – If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the CPU will wait an integral number of clock cycles for READY to go high before completing the read or write cycle. READY must conform to specified setup and hold times.		
RESETIN	36	1	RESET IN – Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. RESET IN is a Schmitt-triggered input, allowing connection to an RC network for power-on RESET delay. The CPU is held in the reset condition as long as RESET IN is applied.		
CLK	37	0	$CLOCK-Clock$ output for use as a system clock. The period of CLK is twice the X_1, X_2 input period.		

Symbol	Number	Input (I) Output (O)	Function
HLDA	38	0	HOLD ACKNOWLEDGE – Indicates that the CPU has received the HOLD request and that it will relinquish the bus in the next clock cycle. HLDA goes low after the Hold request is removed. The CPU takes the bus one half clock cycle after HLDA goes low.
HOLD	39	ı	HOLD – Indicates that another master is requesting the use of the address and data buses. The CPU, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data $\overline{\text{RD}}$, $\overline{\text{WR}}$, and $\overline{\text{IO}}/\overline{\text{M}}$ lines are 3-stated.
V _{cc}	40		POWER SUPPLY (+5V)
V _{SS}	20		GROUND (OV)



Interrupt Priority	Restart Address	, and Sensitivity
--------------------	-----------------	-------------------

Name	Priority	Address Branched To ¹⁾ When Interrupt Occurs	Type Trigger
TRAP	1	24H	Rising edge AND high level until sampled
RST 7.5	2	зсн	Rising edge (latched)
RST 6.5	3	34H	High level until sampled
RST 5.5	4	2CH	High level until sampled
INTR	5	see Note 2	High level until sampled

NOTES

- 1. The processor pushes the PC on the stack before branching to the indicated address.
- The address branched to depends on the instruction provided to the CPU when the interrupt is acknowledged.

Functional Description

The SAB 8085A is a complete 8-bit parallel central processor. It is designed with N-channel depletion loads and requires a single +5 volt supply. Its basic clock speed is 3 MHz (SAB 8085A) or 5 MHz (SAB 8085A-2), thus improving on SAB 8080A's performance with higher system speed. Also it is designed to fit into a minimum system of three ICs: The CPU (SAB 8085A), a RAM/IO (SAB 8156), and a ROM or EPROM/IO chip (SAB 8355 or SAB 8755A).

The SAB 8085A has twelve addressable 8-bit registers. Four of them can function only as two 16-bit register pairs. Six others can be used interchangeably as 8-bit registers or as 16-bit register pairs. The SAB 8085A register set is as follows:

Mnemonic	Register	Contents
ACC or A	Accumulator	8 bits
PC	Program Counter	16-bit address
BC, DE, HL	General-Purpose Registers; data pointer (HL)	8 bits × 6 or 16 bits × 3
SP	Stack Pointer	16-bit address
Flags or F	Flag Register	5 flags (8-bit space)

The SAB 8085A uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first T state (clock cycle) of a machine cycle the low order address is sent out on the Address/Data bus. These lower 8 bits may be latched externally by the Address Latch Enable signal (ALE). During the rest of the machine cycle the data bus is used for memory or I/O data.

The SAB 8085A provides $\overline{\text{RD}}$, $\overline{\text{WR}}$, S_{ϕ} , S_{1} , and $IO/\overline{\text{M}}$ signals for bus control. An Interrupt Acknowledge signal ($\overline{\text{INTA}}$) is also provided. HOLD and all Interrupts are synchronized with the processor's internal clock. The SAB 8085A also provides Serial Input Data (SID) and Serial Output Data (SOD) lines for simple serial interface.

In addition to these features, the SAB 8085A has three maskable, vector interrupt pins and one nonmaskable TRAP interrupt.

Interrupt and Serial I/O

The SAB 8085A has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP. INTR is identical in function to the SAB 8080A INT. Each of the three RESTART inputs, 5.5, 6.5, and 7.5, has a programmable mask. TRAP is also a RESTART interrupt but it is nonmaskable.

The three maskable interrupts cause the internal execution of RESTART (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The non-maskable TRAP causes the internal execution of a RESTART vector independent of the state of the interrupt enable or masks (see table above).

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are **high level-sensitive** like INTR (and INT on the SAB 8080) and are recognized with the same timing as INTR. RST 7.5 is **rising edge-sensitive**.

For RST 7.5, only a pulse is required to set an internal flip-flop which generates the internal interrupt request. The RST 7.5 request flip-flop remains set until the request is serviced. Then it is reset automatically. This flip-flop may also be reset

by using the SIM instruction or by issuing a RESET IN to the SAB 8085A. The RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

The status of the three RST interrupt masks can only be affected by the SIM instruction and $\overline{\text{RESET IN}}$.

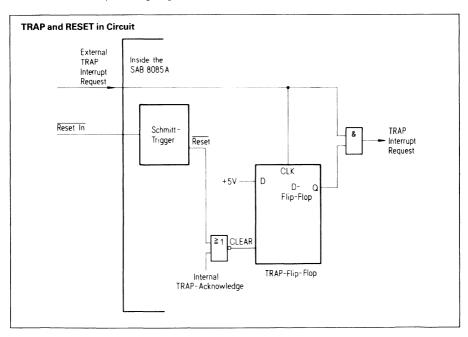
The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending as follows: TRAP – highest priority, RST 7.5, RST 6.5, RST 5.5, INTR – lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt an RST 7.5 routine if the interrupts are re-enabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic events such as power failure or bus error. The TRAP input is recognized just as any other interrupt but has the highest priority. It is not affected by any flag or mask. The TRAP input is both edge and level sensitive. The TRAP input must go high and

remain high until it is acknowledged. It will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches. The following figure illustrates the TRAP interrupt request circuitry within the SAB 8085A. Note that the servicing of any interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5, INTR) disables all future interrupts (except TRAPs) until an El instruction is executed.

The TRAP interrupt is special in that it disables interrupts, but preserves the previous interrupt enable status. Performing the first RIM instruction following a TRAP interrupt allows you to determine whether interrupts were enabled or disabled prior to the TRAP. All subsequent RIM instructions provide current interrupt enable status. Performing a RIM instruction following INTR or RST 5.5 – 7.5 will provide current Interrupt Enable status, revealing that Interrupts are disabled.

The serial I/O system is also controlled by the RIM and SIM instructions. SID is read by RIM, and SIM sets the SOD data.



Driving the X₁ and X₂ Inputs

You may drive the clock inputs of the SAB 8085A or SAB 8085A-2 with a crystal, an LC tuned circuit, an RC network, or an external clock source. The driving

frequency must be at least 1 MHz, and must be twice the desired internal clock frequency; hence, the SAB 8085A is operated with a 6 MHz crystal (for 3 MHz clock), and the SAB 8085A-2 can be operated with a 10 MHz crystal (for 5 MHz clock).

If a crystal is used, it must have the following characteristics:

Parallel resonance at twice the clock frequency desired

 C_L (load capacitance) $\leq 30 \text{ pF}$

 C_s (shunt capacitance) $\leq 7 \text{ pF}$

 R_s (equivalent shunt resistance) ≤ 75 ohms

Drive level: 10 mW

Frequency tolerance: ±.005% (suggested)

Note the use of the 20 pF capacitor between X_2 and ground. This capacitor is required with crystal frequencies below 4 MHz to assure oscillator startup at the correct frequency. A parallel-resonant LC circuit may be used as the frequency-determining network for the SAB 8085A, providing that its frequency tolerance of approximately $\pm 10\%$ is acceptable. The components are from the formula:

$$f = \frac{1}{2 \pi \sqrt{L (C_{ext} + C_{int})}}$$

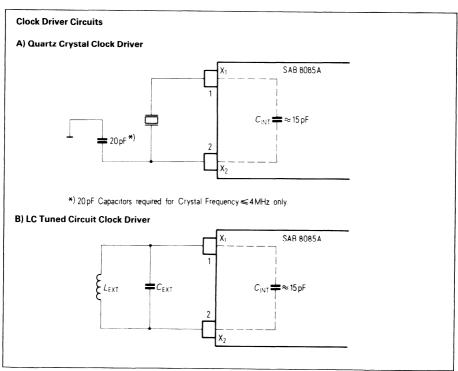
To minimize variations in frequency, it is recommended that you choose a value for C_{ext} that is at least twice that of C_{intr} or 30 pF. The use of an LC

circuit is not recommended for frequencies higher than approximately 5 MHz.

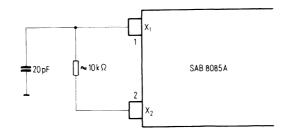
An RC circuit may be used as the frequency-determining network for the SAB 8085A if maintaining a precise clock frequency is of no importance. Variations in the on-chip timing generation can cause a wide variation in frequency when using the RC mode. Its advantage is its low component costs. The driving frequency generated by the circuit shown is approximately 3 MHz. It is not recommended that frequencies greatly higher or lower than this be attempted.

The following figures show the recommended clock driver circuits. Note in D and E that pullup resistors are required to assure that the high level voltage of the input is at least 4V.

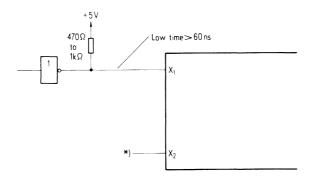
For driving frequencies up to and including 6 MHz you may supply the driving signal to X_1 and leave X_2 opencircuited (Figure D). If the driving frequency is from 6 MHz to 10 MHz, stability of the clock generator will be improved by driving both X_1 and X_2 with a pushpull source (Figure E). To prevent self-oscillation of the SAB 8085A, be sure that X_2 is not coupled back to X_1 through the driving circuit.



C) RC Circuit Clock Driver

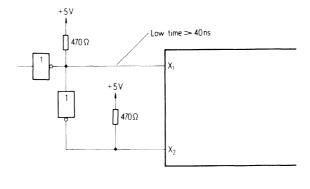


D) 1 - 6 MHz Input Frequency External Clock Driver Circuit



*) X₂ left floating

E) 1 – 10 MHz Input Frequency External Clock Driver Circuit



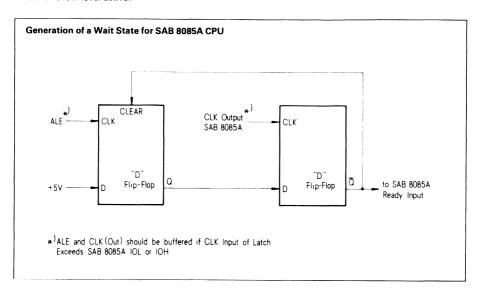
Generating Wait State

If your system requirements are such that slow memories or peripheral devices are being used, the circuit shown in the following figure may be used to insert one WAIT state in each SAB 8085 machine cycle.

The D flip-flops should be chosen so that

- CLK is rising edge-triggered
- CLEAR is low-level active.

As in the SAB 8080, the READY line is used to extend the read and write pulse lengths so that the SAB 8085A can be used with slow memory. HOLD causes the CPU to relinquish the bus when it is through with it by floating the Address and Data Buses.



System Interface

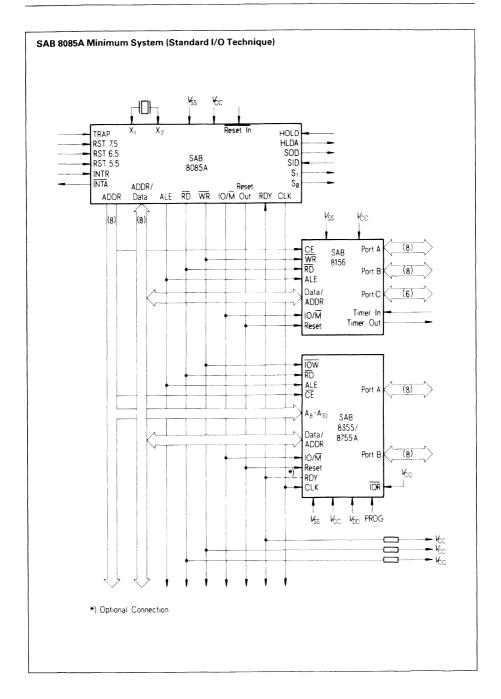
The SAB 8085A family includes memory components, which are directly compatible with the SAB 8085A CPU. For example, a system consisting of the three chips, SAB 8085A, SAB 8156, and SAB 8355 will have the following features:

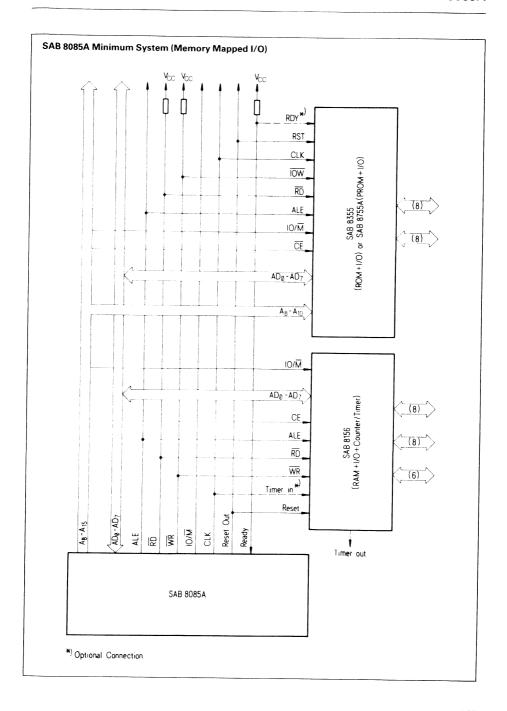
- 2K bytes ROM.
- 256 bytes RAM
- 1 Timer/Counter
- 4 8-bit I/O Ports
- 1 6-bit I/O Port
- 4 Interrupt Levels
- Serial In/Serial Out Ports

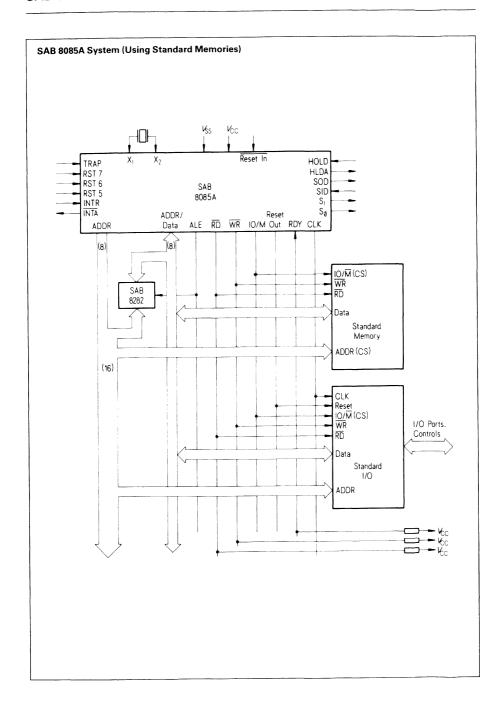
This minimum system, using the standard I/O technique is as shown in the following figure.

In addition to standard I/O, the memory mapped I/O offers an efficient I/O addressing technique. With this technique, an area of memory address space is assigned for I/O address, thereby, using the memory address for I/O manipulation. The figure on page 11 shows the system configuration of Memory Mapped I/O using SAB 8085A.

The SAB 8085A CPU can also interface with the standard memory that does **not** have the multiplexed address/data bus. It will require a simple SAB 8282 (8-bit latch) as shown in the figure on page 12.



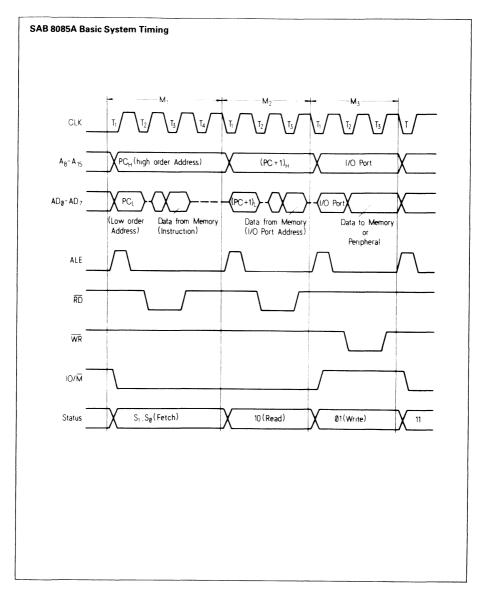




Basic System Timing

The SAB 8085A has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8-bits of address on the Data Bus. The following figure shows an instruction fetch, memory read and I/O write

cycle (as would occur during processing of the OUT instruction). Note that during the I/O write and read cycle the I/O port address is copied on both, the upper and lower half of the address.



There are seven possible types of machine cycles. Which of these seven takes place is defined by the status of the three status lines (IO/\overline{M} , S_1 , S_0) and the three control signals (\overline{RD} , \overline{WR} , and \overline{INTA}); (see following table). The status lines can be used as advanced controls (for device selection, for example),

since they become active at the T_1 state, at the outset of each maching cycle. Control lines \overline{RD} and \overline{WR} become active later, at the time when the transfer of data is to take place, so are used as command lines

SAB 8085A Machine Cycle Chart

		Status			Contro	Control		
Machine Cycle	IO/M	S1	SØ	RD	WR	ĪNTA		
Opcode Fetch	(OF)	Ø	1	1	0	1	1	
Memory Read		Ø	1	Ø	Ø	1	1	
Memory Write		Ø	Ø	1	1	Ø	1	
I/O Read	(IOR)	1	1	Ø	Ø	1	1	
/O Write	(IOW)	1	0	1	1	Ø	1	
Acknowledge for INTR	(INA)	1.	1	1	1	1	Ø	
Bus Idle	(BI): DAD	Ø	1	Ø	1	1	1	
	ACK of							
	RST, TRAP	1	1	1	1	1	1	
	HALT	TS	Ø	Ø	TS	TS	1	

0 = Logic "0"; 1 = Logic "1"; TS = High Impedance

A machine cycle normally consists of three T states, with the exception of OPCODE FETCH, which normally has either four or six T states (unless WAIT

or HOLD states are forced by the receipt of READY or HOLD inputs). Any T state must be one of ten possible states, as summarized in the following table.

SAB 8085A Machine State Chart

Machine	Status an	d Buses	Control				
State	S1, SØ	IO/M	A ₈ -A ₁₅	AD ₀ -AD ₇	RD, WR	ĪNTA	ALE
Τ,	X	X	X	X	1	1	1 ¹)
T ₂	X	X	×	×	X	X	Ø
T _{WAIT}	X	X	×	×	X	×	Ø
T ₃	X	X	×	×	×	×	Ø
T.	1	Ø 2)	X	TS	1	1	Ø
T ₅	1	0 2)	X	TS	1	1	Ø
. 5 Т ₆	1	(Ø ²)	×	TS	1	1	Ø
T _{reset}	×	TS	TS	TS	TS	1	Ø
THALT	0	TS	TS	TS	TS	1	Ø
T _{HOLD}	ĺx	TS	TS	TS	TS	1	Ø

 $[\]emptyset = Logic "\emptyset"$; 1 = Logic "1"; TS = High Impedance; X = Unspecified.

¹⁾ ALE not generated during 2nd and 3nd machine cycles of DAD instruction.

²) $IO/\overline{M} = 1$ during $T_4 - T_6$ of INA machine cycle.

Instruction Set Summary

			I	nstruc	ction (Code			Operations
Mnemonic	D ₇	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Description
MOVE, LOAD,	AND :	STOR	E						
MOVr1 r2	Ø	1	D	D	D	S	S	S	Move register to register
MOV M.r	Ø	1	1	1	Ø	S	S	S	Move register to memory
MOV r.M	Ø	1	D	D	D	1	1	Ø	Move memory to register
MVIr	Ø	Ø	D	D	D	1	1	Ø	Move immediate register
MVIM	Ø	Ø	1	1	Ø	1	1	ø	Move immediate memory
LXI B	Ø	Ø	Ø	Ø	Ø	Ø	0	1	Load immediate register Pair B & C
LXID	0	Ø	Ø	1	Ø	Ø	Ø	1	Load immediate register Pair D & E
LXIH	0	Ø	1	0	Ø	0	Ø	1	Load immediate register Pair H & L
STAX B	0	0	Ø	Ø	ø	ø	1	Ö	Store A indirect
STAX D	0	Ø	Ø	1	ō	ø	1	Ø	Store A indirect
LDAX B	0	Ø	Ø	ø	1	ø	1	ø	Load A indirect
LDAX D	0	Ø	ø	1	1	ø	1	ő	Load A indirect
STA	0	ø	1	1	ø	Ø	1	Ø	Store A direct
LDA	o	ø	1	1	1	Ø	1	Ø	Load A direct
SHLD	o	ő	1	ø	ø	Ø	1	Ø	Store H & L direct
LHLD	0	Ø	1	Ö	1	Ø	i	Ø	Load H & L direct
XCHG	1	1	1	Ø	i	Ø	1	1	Exchange D & E, H & L Registers
	+			-					Exchange D & E, H & E Registers
STACK OPS									
PUSH B	1	1	Ø	Ø	Ø	1	Ø	1	Push register Pair B & C on stack
PUSH D	1	1	Ø	1	Ø	1	Ø	1	Push register Pair D & E on stack
PUSH H	1	1	1	Ø	Ø	1	Ø	1	Push register Pair H & L on stack
PUSH PSW	1	1	1	1	Ø	1	Ø	1	Push A and Flags on stack
POP B	1	1	Ø	Ø	Ø	Ø	Ø	1	Pop register Pair B & C off stack
POP D	1	1	Ø	1	Ø	Ø	Ø	1	Pop register Pair D & E off stack
POP H	1	1	1	Ø	Ø	Ø	Ø	1	Pop register Pair H & L off stack
POP PSW	1	1	1	1	Ø	Ø	Ø	1	Pop A and Flags off stack
XTHL	1	1	1	Ø	Ø	Ø	1	1	Exchange top of stack, H & L
SPHL	1	1	1	1	1	Ø	Ø	1	H & L to stack pointer
LXI SP	Ø	Ø	1	1	Ø	Ø	0	1	Load immediate stack pointer
INX SP	Ø	Ø	1	1	Ø	Ø	1	1	Increment stack pointer
DCX SP	Ø	Ø	1	1	1	Ø	1	1	Decrement stack pointer
JUMP									
JMP	1	1	Ø	Ø	Ø	Ø	1	1	Jump unconditional
JC	1	1	ø	1	1	Ø	1	ø	Jump on carry
JNC	1	1	Ø	1	ø	Ø	1	Ø	Jump on no carry
JZ	l i	i	Ø	ø	1	Ø	1	Ø	Jump on zero
JNZ	;	1	Ø	Ø	ø	Ø	1	Ø	Jump on no zero
JP	1	1	1	1	Ø	Ø	1	Ø	Jump on no zero Jump on positive
JM	1	1	1	1	1	Ø	1	Ø	, , ,
JPE	1	1	1	ó	1	Ø	1	Ø	Jump on minus
JPO	1	1	1	Ø		Ø			Jump on parity even
PCHL		1	1	Ø	Ø 1	Ø	1	0	Jump on perity odd
CITE		1	- 1	Ų	· ·	Ų	Ø	1	H & L to program counter

SAB 8085A

Instruction Set Summary (Cont'd)

			In	struc	tion (Code			Operations
Mnemonic	D ₇	D_6	D_5	D_4	D_3	D_2	D_1	D_{\emptyset}	Description
CALL									
CALL	1	1	Ø	Ø	1	1	Ø	1	Call unconditional
CC	1	1	Ø	1	1	1	Ø	ø	Call on carry
CNC	1	1	ø	1	ø	1	ø	ő	Call on no carry
CZ	1	1	ø	Ø	1	1	ø	ø	Call on zerro
CNZ	1	1	Ø	Ø	Ø	1	Ø	Ø	Call on no zerro
CP	1	1	1	1	Ø	1	Ø	Ø	Call on positive
CM	1	1	1	1	1	1	Ø	Ø	Call on minus
CPE	1	1	1	Ø	1	1	Ø	Ø	Call on parity even
СРО	1	1	1	Ø	Ø	1	Ø	Ø	Call on parity odd
RETURN									
RET	1	1	Ø	Ø	1	Ø	Ø	1	Return
RC	1	1	Ø	1	1	Ø	Ø	Ø	Return on carry
RNC	1	1	Ø	1	Ø	Ø	Ø	Ø	Return on no carry
RZ	1	1	Ø	Ø	1	Ø	Ø	Ø	Return on zero
RNZ	1	1	Ø	Ø	Ø	Ø	Ø	Ø	Return on no zero
RP	1	1	1	1	Ø	Ø	Ø	Ø	Return on positive
RM	1	1	1	1	1	Ø	Ø	Ø	Return on minus
RPE	1	1	1	Ø	1	Ø	Ø	Ø	Return on parity even
RPO	1	1	1	Ø	Ø	Ø	Ø	Ø	Return on parity odd
RESTART									
RST	1	1	Α	Α	Α	1	1	1	Restart
INPUT/OUTPUT									
IN	1	1	Ø	1	1	Ø	1	1	Input
OUT	1	1	ø	1	ø	ø	1	1	Output
INCREMENT AN	D DE	CREM	IENT						
INR r	l ø	Ø	D	D	D	1	Ø	Ø	Increment register
DCR r	ő	Ø	D	D	D	1	Ø	1	Decrement register
INR M	ø	Ø	1	1	Ø	i	ø	ø	Increment memory
DCR M	ő	Ø	i	i	Ø	i	Ø	1	Decrement memory
INX B	ő	Ø	ø	ø	Ø	ø	1	i	Increment B & C registers
INX D	ø	ø	Ø	1	Ø	Ø	1	i	Increment D & E registers
INX H	ø	ø	1	ø	Ø	ø	1	i	Increment H & L registers
DCX B	ő	ø	ø	ø	1	ø	1	i	Decrement B & C
DCX D	ø	ø	ø	1	1	Ø	1	i	Decrement D & E
DCX H	ø	Ø	1	ø	1	ø	1	1	Decrement H & L
ADD									
ADD r	1	Ø	Ø	Ø	Ø	S	S	S	Add register to A
ADC r	1	Ø	Ø	Ø	1	S	S	S	Add register to A Add register to A with carry
ADD M	'1	Ø	Ċ	Ø	ø	1	1	0	Add memory to A
ADC M	1	Ø	Ø	Ø	ש 1	1	1	Ø	Add memory to A with carry
ADI		1	Ø	Ø	ø	1	1	Ø	Add immediate to A
ACI		1	Ø	Ø	1	1	1	Ø	Add immediate to A with carry
DAD B	ó	ø	Ø	Ø	1	ø	ø	1	Add B & C to H & L
DAD D	lő	Ø	Ø	1	1	Ø	Ø	1	Add D & E to H & L
DAD H	ø	Ø	1	ø	1	Ø	Ø	1	Add H & L to H & L
DAD SP	ő	Ø	1	1	1	Ø	Ø	1	Add stack pointer to H & L
							· ·		Add stack pointer to H & E

Instruction Set Summary (Cont'd)

Mnemonic SUBTRACT SUB r SBB r SUB M SBB M SUI SBI LOGICAL	D ₇ 1 1 1 1 1 1 1 1	D ₆ Ø Ø Ø	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	Description
SUB r SBB r SUB M SBB M SUI SBI	1 1 1 1	Ø Ø Ø	Ø		Ø				
SBB r SUB M SBB M SUI SBI	1 1 1 1	Ø Ø Ø	Ø		Ø				
SUB M SBB M SUI SBI	1 1 1	Ø		4	v	S	S	S	Subtract register from A
SBB M SUI SBI	1	Ø	Ø	1	1	S	S	S	Subtract register from A with borrow
SUI SBI	1	-	v	1	Ø	1	1	Ø	Subtract memory from A
SBI			Ø	1	1	1	1	Ø	Subtract memory from A with borrow
	1	1	Ø	1	Ø	1	1	Ø	Subtract immediate from A
LOGICAL	'	1	Ø	1	1	1	1	Ø	Subtract immediate from A with borrow
ANA r	1	Ø	1	Ø	Ø	S	S	S	And register with A
XRA r	1	ø	1	ø	1	s	S	S	Exclusive OR register with A
ORA r	1	ő	1	1	ø	S	s	S	OR register with A
CMP r	1	ø	1	i	1	S	s	S	Compare register with A
ANA M	1	Ø	i	ø	ø	1	1	0	And memory with A
XRA M	1	ø	1	ø	1	1	1	Ø	Exclusive OR memory with A
ORA M	1	Ø	1	1	ø	1	1	Ø	OR memory with A
CMP M	1	Ø	i	i	1	1	1	Ø	Compare memory with A
ANI	1	1	1	ø	ø	1	i	Ø	And immediate with A
XRI	i	1	1	Ø	1	1	1	Ø	Exclusive OR immediate with A
ORI	1	1	1	1	ø	1	1	Ø	OR immediate with A
CPI	1	1	1	1	1	1	1	Ø	Compare immediate with A
							•		compare ininiculate with A
ROTATE			_	_	_				
RLC	Ø	Ø	Ø	Ø	Ø	1	1	1	Rotate A left
RRC	Ø	Ø	Ø	Ø	1	1	1	1	Rotate A right
RAL	Ø	Ø	Ø	1	Ø	1	1	1	Rotate A left throught carry
RAR	0	Ø	Ø	1	1	1	1	1	Rotate A right through carry
SPECIALS									
CMA	Ø	Ø	1	Ø	1	1	1	1	Complement A
STC	Ø	Ø	1	1	Ø	1	1	1	Set carry
CMC	Ø	Ø	1	1	1	1	1	1	Complement carry
DAA	Ø	Ø	1	Ø	Ø	1	1	1	Decimal adjust A
CONTROL									
EI	1	1	1	1	1	Ø	1	1	Enable interrupt
DI	1	1	1	1	Ø	Ø	1	1	Disable interrupt
NOP	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	No operation
HLT	Ø	1	1	1	Ø	1	1	Ø	Halt
NEW SAB 8085A	INST	RUC	TIONS	S					
RIM I	Ø	Ø	1	Ø	Ø	Ø	Ø	Ø	Read Interrupt Mask
SIM	Ø	Ø	i	1	ø	Ø	ø	Ø	Set Interrupt Mask

NOTES

^{1.} DDS or SSS: B 000, C 001, D 010, E 011, H 100, L 101, Memory 110, A 111.

^{2.} Two possible cycle times (6/12) indicate instruction cycles dependent on condition flags.

^{*} All mnemonic copyrighted © Intel Corporation 1976.

SAB 8085A

Absolute maximum ratings *)

Ambient Temperature Under Bias

0 to 70°C

Storage Temperature

 $-65~to~\pm125^{\circ}C$

Voltage on any Pin with Respect to Ground Power Dissipation

-0.5 to +7 V 1.5 Watt

D.C. Characteristics

 $T_{A}=0$ to 70°C; $V_{CC}=5\,V\,\pm5\%$; $V_{SS}=0\,V$; (unless otherwise specified)

Symbol	Parameter	Limi	t Values	Units	Test Conditions	
		Min.	Max.	1		
V _{IL}	Input Low Voltage	-0.5	+0.8			
V _{IH}	Input High Voltage	2.0	V _{CC} +0.5] _v		
V _{OL}	Output Low Voltage	_	0.45] *	$I_{OL} = 2 \text{ mA}$	
V _{OH}	Output High Voltage	2.4	-		$I_{OH} = -400 \mu A$	
$I_{\rm CC}$	Power Supply Current		170	mA	_	
I _{IL}	Input Leakage	-	± 10	цA	$V_{\text{IN}} = V_{\text{CC}}$	
I _{LO}	Output Leakage		_ 10	"	$0.45\mathrm{V} \leqslant V_{\mathrm{OUT}} \leqslant V_{\mathrm{CC}}$	
V _{ILR}	Input Low Level, RESET	-0.5	+0.8			
V _{IHR}	Input High Level, RESET	2.4	V _{CC} +0.5	v	_	
V _{HY}	Hysteresis, RESET	0.25				

^{*)} Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

A.C. Characteristics

 $T_{\rm A} = 0 \text{ to } 70^{\circ} \text{C}; V_{\rm CC} = 5 \text{V} \pm 5\%; V_{\rm SS} = 0 \text{V}$

Symbol	Parameter		Units			
		SAE	3 8085A ²⁾	SAB	8085A-2 ²⁾	1
		Min.	Max.	Min.	Max.	1
$t_{\rm CYC}$	CLK Cycle Period	320	2000	200	2000	
t_1	CLK Low Time (Standard CLK Loading)	80		40		1
t_2	CLK High Time Standard CLK Loading)	120	_	70	_	
$t_{\rm r}$, $t_{\rm t}$	CLK Rise and Fall Time		30	-	30	1
t_{XKR}	X ₁ Rising to CLK Rising	30	120	30	100	1
t _{XKF}	X ₁ Rising to CLK Falling	30	150	30	110	1
t _{AC}	A ₈ -A ₁₅ Valid to Leading Edge of Control ¹⁾	270		115		1
t _{ACL}	A ₀ -A ₇ Valid to Leading Edge of Control	240	_	115	-	
t _{AD}	A ₀ – A ₁₅ Valid to Valid Data In		575		350	1
t _{AFR}	Address Float After Leading Edge of READ (INTA)	-	0	_	0	
t _{AL}	A ₈ -A ₁₅ Valid Before Trailing Edge of ALE ¹⁾	115		50		1
t _{ALL}	A ₀ -A ₇ Valid Before Trailing Edge of ALE	90	_	50	_	
t _{ARY}	READY Valid from Address Valid	_	220		100	ns
t _{CA}	Address (A ₈ -A ₁₅) Valid After Control	120		60		
t _{CC}	Width of Control Low (RD, WR, INTA)	400		230		
t _{CL}	Trailing Edge of Control to Leading Edge of ALE	50	_	25	_	
t _{DW}	Data Valid to Trailing Edge of WRITE	420		230		
t _{habe}	HLDA to Bus Enable		210		150	1
t _{HABF}	Bus Float After HLDA		210	-	150	
t _{HACK}	HLDA Valid to Trailing Edge of CLK	110		40		
t_{HDH}	HOLD Hold Time	0		0		
t _{HDS}	HOLD Setup Time to Trailing Edge of CLK	170		120		
t _{INH}	INTR Hold Time	0		0		
t _{INS}	INTR, RST, and TRAP Setup Time to Falling Edge of CLK		_	150]-	
t _{LA}	Address Hold Time After ALE	100		50		
$t_{\rm LC}$	Trailing Edge of ALE to Leading Edge of Control	130		60		
t_{LCK}	ALE Low During CLK High	100	7	50	7	

Notes see next page.

A.C. Characteristics (Continued)

Symbol	Parameter	Limit Values						
		SAE	3 8085A ²⁾	SAB	8085A-2 ²⁾	7		
		Min.	Max.	Min.	Max.			
t _{LDR}	ALE to Valid Data During Read		460		270			
t_{LDW}	ALE to Valid Data During Write		200		120			
t_{LL}	ALE Width	140	_	80	-			
t _{LRY}	ALE to READY Stable	_	110	-	30			
t _{RAE}	Trailing Edge of READ to Re-Enabling of Address	150	_	90	-			
t _{RD}	READ (or INTA) to Valid Data	-	300	_	150			
t _{RV}	Control Trailing Edge to Leading Edge of Next Control	400		220		ns		
t_{RDH}	Data Hold Time After READ INTA ⁷⁾	0		0				
t _{RYH}	READY Hold Time]	_		-			
t _{RYS}	READY Setup Time to Leading Edge of CLK	110		100				
t _{wD}	Data Valid After Trailing Edge of WRITE	100		60				
t _{WDL}	LEADING Edge of WRITE to Data Valid	-	40	_	20			

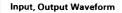
NOTES

- 1. A_8-A_{15} address Specs apply to IO/\overline{M} , S_0 , and S_1 except A_8-A_{15} are undefined during T_4-T_6 of OF cycle, whereas IO/\overline{M} , S_0 , and S_1 are stable.
- 2. **Test conditions**: $t_{CYC} = 320 \text{ ns}$ (SAB 8085A)/200 ns (SAB 8085A-2); $C_L = 150 \text{ pF}$.
- 3. For all output timings where $C_L = 150 \, \text{pF}$ use the following correction factors:

```
25 pF \leq C_L < 150 pF: -0.10 \text{ ns/pF}
150 pF < C_L \leq 300 pF: +0.30 \text{ ns/pF}
```

- 4. Output timings are measured with purely capacitive load.
- 5. All timings are measured at output votage $V_L = 0.8V$, $V_H = 2.0V$, and 1.5V with 20 ns rise and fall time on inputs.
- 6. To calculate timing specifications at other values of t_{CYC} the following table should be used.
- 7. Data hold time is guaranteed under all loading conditions.

A.C. Testing

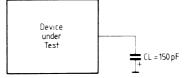




A.C. Testing: Input are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0".

Timing Measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

Load Circuit



 $C_L = 150 pF$

C_L = includes JIG Capacitance

Bus Timing Specification as a $t_{\rm CYC}$ Dependent SAB 8085A

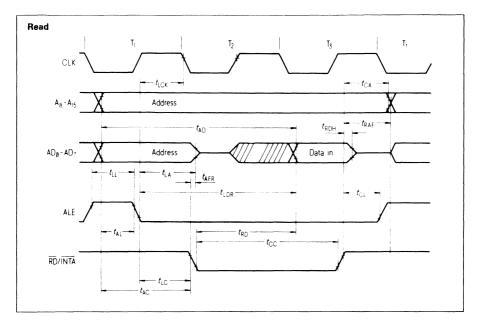
Symb.	Min.	Max.
t _{AL}	(1/2) T - 45	
t _{LA}	(1/2) T - 60	
t _{LL}	(1/2) T - 20	_
t_{LCK}	(1/2) T - 60	
t _{LC}	(1/2) T - 30	
t _{AD}		(5/2 + N) T - 225
t_{RD}		(3/2 + N) T - 180
t _{RAE}	(1/2) T - 10	
t_{CA}	(1/2) T - 40	
$t_{\sf DW}$	(3/2 + N) T - 60	
t _{WD}	(1/2) T - 60	_
t _{CC}	(3/2 + N) T - 80	
t _{CL}	(1/2) T - 110	
t _{ARY}	-	(3/2) T - 260
t _{HACK}	(1/2) T - 50	10.00
t_{HABF}		(1/2) T + 50
t_{HABE}		(1/2) T + 50
t _{AC}	(2/2) T - 50	
t ₁	(1/2) T - 80	_
$\overline{t_2}$	(1/2) T - 40	
t _{RV}	(3/2) T - 80	
t _{LDR}	_	(4/2) T - 180

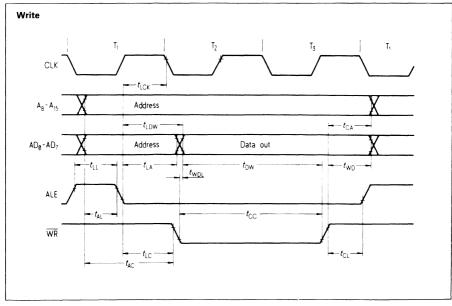
N is equal to the total WAIT states. $T = t_{CYC}$

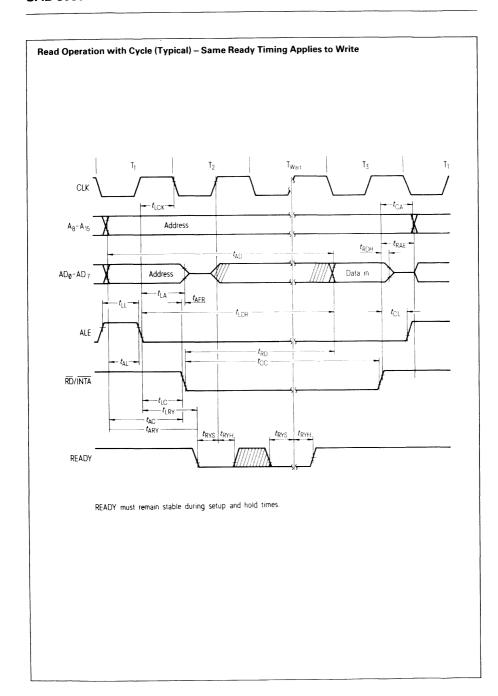
SAB 8085A-2

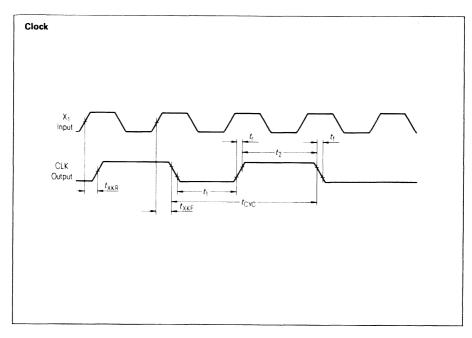
Symb.	Min.	Max.
t _{AL}	(1/2) T - 50	
t _{LA}	(1/2) T - 50	
t _{LL}	(1/2) T - 20	
t _{LCK}	(1/2) T - 50	
t_{LC}	(1/2) T - 40	
t_{AD}		(5/2 + N) T - 150
t_{RD}		(3/2 + N) T - 150
t_{RAE}	(1/2) T - 10	
t_{CA}	(1/2) T - 40	
t_{DW}	(3/2 + N) T - 70	_
t _{WD}	(1/2) T - 40	
t_{CC}	(3/2 + N) T - 70	
t_{CL}	(1/2) T - 75	
t _{ARY}	_	(3/2) T - 200
t _{HACK}	(1/2) T - 60	_
t _{HABF}		(1/2) T + 50
t _{HABE}		(1/2) T + 50
t _{AC}	(2/2) T - 85	
t ₁	(1/2) T - 60	_
$\overline{t_2}$	(1/2) T - 30	
t _{RV}	(3/2) T - 80	
t_{LDR}	_	(4/2) T - 130

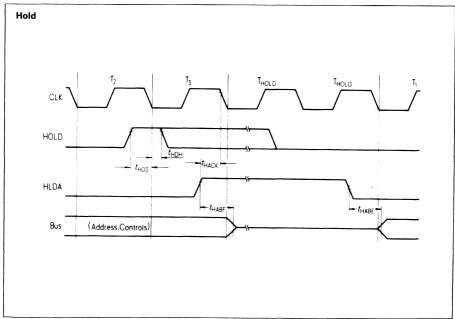
Waveforms

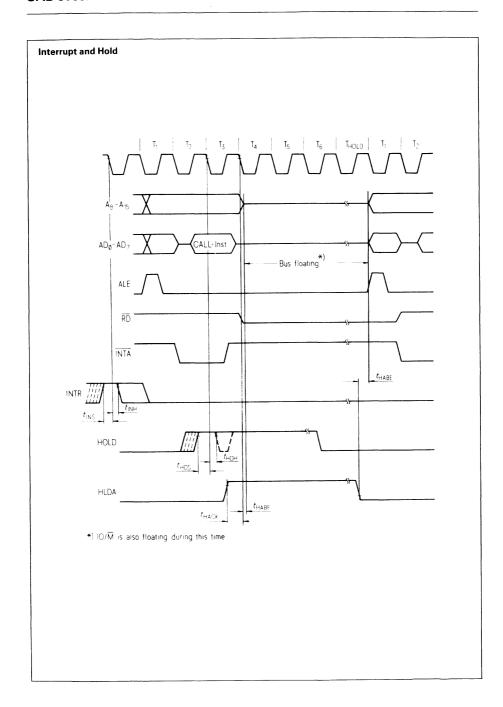




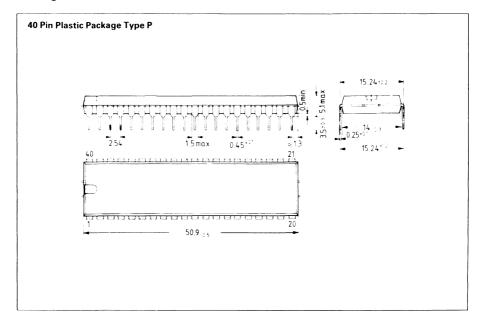








Package Outline



SAB 8085A

Ordering Information

Component	Description	Ordering Number		
	8-Bit Microprocessor			
SAB 8085A-P	–3 MHz, 1.3 μs, (plastic)	Q 67120-C34		
SAB 8085A-2-P	–5 MHz, 0.8 μs, (plastic)	Q 67120-C41		

SAB 8085AH 8-Bit Microprocessor

SAB 8085AH (3 MHz)

- Single +5V Power Supply with ±10% Voltage Margins
- 30% Less Icc than SAB 8085A
- 100% Software Compatible with SAB 8080A
- 1.3 μs Instruction Cycle (SAB 8085AH);
 0.8 μs (SAB 8085AH-2)
- On-Chip Clock Generator (with External Crystal, LC or RC Network)
- On-Chip System Controller; Advanced Cycle Status Information Available for Large System Control

SAB 8085AH-2 (5 MHz)

- Four Vectored Interrupt Inputs (one is Non-Maskable) Plus an SAB 8080A Compatible Interrupt
- Serial In/Serial Out Port
- Decimal, Binary and Double Precision Arithmetic
- Direct Addressing Capability to 64K Bytes of Memory

Pin Configurat	ion	Pin Name:	Pin Names							
X	40 Hrc 39 HOLD 38 HLDA 37 CLK(Out) 36 RESTIN 36 READY 54 IO/M 33 S; 52 RD 31 WR 30 ALE 29 I Se 28 Als 27 Ala 26 I Ala 26 I Ala 27 Ala 28 Ala 29 I Ala 20 I Ala 21 I Ala 22 I Ala 23 I Ala 24 I Ala 25 I Ala 26 I Ala 27 I Ala 28 I Ala 29 I Ala	A_8-A_{15} AD_0-AD_7 ALE $S_0, S_1, IO/\overline{M}$ \overline{RD} \overline{WR} \overline{READY} \overline{HOLD} \overline{HLDA} \overline{INTR}	Address Bus Mux. Address/ Data Bus Address Latch Enable Machine Cycle Status Read Control Write Control Ready Hold Hold Acknowledge Interrupt Request	INTA RST 5.5, 6.5, 7.5 TRAP RESET IN RESET OUT X ₁ , X ₂ CLK SID SOD V _{CC} V _{SS}	Interrupt Acknowledge Restart Interrupts Trap Reset in Reset out Crystal/Clock Input Clock Output Serial Input Data Serial Output Data +5V Ground (OV)					

SAB 8085AH is a complete 8 bit parallel Central Processing Unit (CPU). Its instruction set is 100% software compatible with the SAB 8080A microprocessor. Its high level of system integration allows a minimum of three ICs (SAB 8085AH (CPU), SAB 8156 (RAM/IO) and SAB 8355/SAB 8755A (ROM/PROM/IO)) while maintaining total system expandability. The SAB 8085AH-2 is a faster version of the SAB 8085AH.

The SAB 8085AH incorporates all of the features that the SAB 8224 (clock generator) and SAB 8228

(system controller) provided for the SAB 8080A, thereby offering a high level of system integration. The SAB 8085AH uses a multiplexed data bus. The address is split between the 8 bit address bus and the 8 bit data bus. The on-chip address latches of SAB 8155/SAB 8156/SAB 8355/SAB 8755A memory products allow a direct interface with the SAB 8085AH.

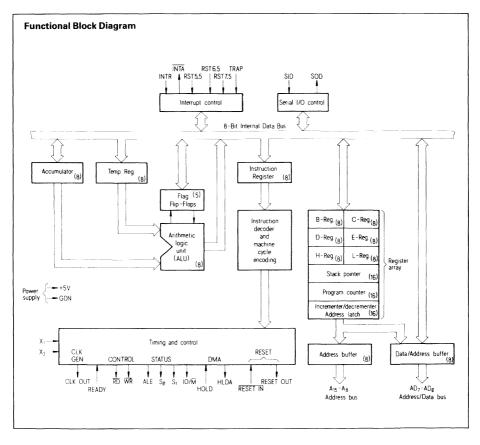
SAB 8085AH is implemented in +5V advanced N-channel, silicon gate Siemens MYMOS technology and is a selected version of the standard SAB 8085A

Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function						
X ₁ , X ₂	1, 2	1	X_1 AND X_2 – Are connected to a crystal, LC, or RC networ to drive the internal clock generator. X_1 can also be an external clock input from a logic gate. The input frequencis divided by 2 to give the processor's internal operating frequency.						
RESET OUT	3	0	RESET OUT – Reset Out indicates CPU is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.						
SOD	4	0	SERIAL OUTPUT DATA LINE – The output SOD is set or reset as specified by the SIM instruction.						
SID	5	1	SERIAL INPUT DATA LINE – The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.						
TRAP	6	I	TRAP – Trap interrupt is a nonmaskable RESTART interrupt. It is recognized at the same time as INTR or RST 5.5-7.5. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt (see following table).						
RST 5.5 RST 6.5 RST 7.5	9 8 7	1	RESTART INTERRUPTS – These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted. The priority of these interrupts is ordered as shown in the following table. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction.						
INTR	10	l	INTERRUPT REQUEST – Is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an INTA will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.						
INTA	11	0	INTERRUPT ACKNOWLEDGE – Is used instead of (and has the same timing as) RD during the instruction cycle after an INTR is accepted. It can be used to activate an SAB 8259A Interrupt chip or some other interrupt port.						
AD ₀ -AD ₇	12-19	I/O	MULTIPLEXED ADDRESS/DATA BUS – Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.						
A ₈ -A ₁₅	21-28	0	ADDRESS BUS – The most significant 8 bits of the memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.						

Symbol	Number	Input (I) Output (O)	Function						
S_{\emptyset} , S_{1} , and IO/\overline{M}	29, 33	0	MACHINE CYCLE STATUS -						
	34		IO/M S ₁ S ₀ Status						
			0						
			* = 3-state (high impedance) X = unspecified						
			S_1 can be used as an advanced R/\overline{W} status. IO/\overline{M} , S_0 and S_1 become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines.						
ALE	30	О	ADDRESS LATCH ENABLE – It occurs during the first closs state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can als be used to strobe the status information. ALE is never 3-stated.						
WR	31	0	WRITE CONTROL – A low level on WR indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of WR. 3-stated during Hold and Halt modes and during RESET.						
RD	32	0	READ CONTROL – A low level on \overline{RD} indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer, 3-stated during Hold and Halt modes and during RESET.						
READY	35	ı	READY – If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the CPU will wait an integral number of clock cycles for READY to go high before completing the read or write cycle. READY must conform to specified setup and hold times.						
RESETIN	36	I	RESET IN – Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. RESET IN is a Schmitt-triggered input, allowing connection to an RC network for power-on RESET delay. The CPU is held in the reset condition as long as RESET IN is applied.						
CLK	37	0	CLOCK – Clock output for use as a system clock. The period of CLK is twice the X_1,X_2 input period.						

Symbol	Number	Input (I) Output (O)	Function						
HLDA	38	0	HOLD ACKNOWLEDGE – Indicates that the CPU has received the HOLD request and that it will relinquish the bus in the next clock cycle. HLDA goes low after the Hold request is removed. The CPU takes the bus one half clock cycle after HLDA goes low.						
HOLD	39		HOLD – Indicates that another master is requesting the use of the address and data buses. The CPU, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data RD, WR, and IO/M lines are 3-stated.						
V _{CC}	40		POWER SUPPLY (+5V)						
V _{SS}	20		GROUND (OV)						



Name	Priority	Address Branched To ¹⁾ When Interrupt Occurs	Type Trigger					
TRAP	1	24H	Rising edge AND high level until sampled					
RST 7.5	2	3СН	Rising edge (latched)					
RST 6.5	3	34H	High level until sampled					
RST 5.5	4	2CH	High level until sampled					
INTR	5	see Note 2	High level until sampled					

NOTES

- 1. The processor pushes the PC on the stack before branching to the indicated address.
- The address branched to depends on the instruction provided to the CPU when the interrupt is acknowledged.

Functional Description

The SAB 8085AH is a complete 8-bit parallel central processor. It is designed with N-channel depletion loads and requires a single +5 volt supply. Its basic clock speed is 3 MHz (SAB 8085AH) or 5 MHz (SAB 8085AH-2), thus improving on SAB 8080A's performance with higher system speed. Also it is designed to fit into a minimum system of three ICs: The CPU (SAB 8085AH), a RAM/IO (SAB 8156), and a ROM or EPROM/IO chip (SAB 8355 or SAB 8755A).

The SAB 8085AH has twelve addressable 8-bit registers. Four of them can function only as two 16-bit register pairs. Six others can be used interchangeably as 8-bit registers or as 16-bit register pairs. The SAB 8085AH register set is as follows:

Mnemonic	Register	Contents
ACC or A	Accumulator	8 bits
PC	Program Counter	16-bit address
BC, DE, HL	General-Purpose Registers; data pointer (HL)	8 bits × 6 or 16 bits × 3
SP	Stack Pointer	16-bit address
Flags or F	Flag Register	5 flags (8-bit space)

The SAB 8085AH uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first T state (clock cycle) of a machine cycle the low order address is sent out on the Address/Data bus. These lower 8 bits may be latched externally by the Address Latch Enable signal (ALE). During the rest of the machine cycle the data bus is used for memory or I/O data.

The SAB 8085AH provides \overline{RD} , \overline{WR} , S_0 , S_1 , and IO/\overline{M} signals for bus control. An Interrupt Acknowledge signal (\overline{INTA}) is also provided. HOLD and all Interrupts are synchronized with the processor's internal clock. The SAB 8085AH also provides Serial Input Data (SID) and Serial Output Data (SOD) lines for simple serial interface.

In addition to these features, the SAB 8085AH has three maskable, vector interrupt pins and one nonmaskable TRAP interrupt.

Interrupt and Serial I/O

The SAB 8085AH has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP. INTR is identical in function to the SAB 8080A INT. Each of the three RESTART inputs, 5.5, 6.5, and 7.5, has a programmable mask. TRAP is also a RESTART interrupt but it is nonmaskable.

The three maskable interrupts cause the internal execution of RESTART (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The non-maskable TRAP causes the internal execution of a RESTART vector independent of the state of the interrupt enable or masks (see table above).

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are **high level-sensitive** like INTR (and INT on the SAB 8080) and are recognized with the same timing as INTR. RST 7.5 is **rising edge-sensitive**.

For RST 7.5, only a pulse is required to set an internal flip-flop which generates the internal interrupt request. The RST 7.5 request flip-flop remains set until the request is serviced. Then it is reset automatically. This flip-flop may also be reset

by using the SIM instruction or by issuing a RESETIN to the SAB 8085AH. The RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

The status of the three RST interrupt masks can only be affected by the SIM instruction and RESET IN.

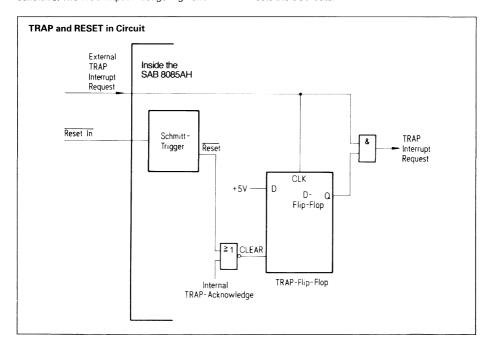
The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending as follows: TRAP – highest priority, RST 7.5, RST 6.5, RST 5.5, INTR – lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt an RST 7.5 routine if the interrupts are re-enabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic events such as power failure or bus error. The TRAP input is recognized just as any other interrupt but has the highest priority. It is not affected by any flag or mask. The TRAP input is both edge and level sensitive. The TRAP input must go high and

remain high until it is acknowledged. It will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches. The following figure illustrates the TRAP interrupt request circuitry within the SAB 8085AH. Note that the servicing of any interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5, INTR) disables all future interrupts (except TRAPs) until an El instruction is executed.

The TRAP interrupt is special in that it disables interrupts, but preserves the previous interrupt enable status. Performing the first RIM instruction following a TRAP interrupt allows you to determine whether interrupts were enabled or disabled prior to the TRAP. All subsequent RIM instructions provide current interrupt enable status. Performing a RIM instruction following INTR or RST 5.5 – 7.5 will provide current Interrupt Enable status, revealing that Interrupts are disabled.

The serial I/O system is also controlled by the RIM and SIM instructions. SID is read by RIM, and SIM sets the SOD data.



Driving the X₁ and X₂ Inputs

You may drive the clock inputs of the SAB 8085AH or SAB 8085AH-2 with a crystal, an LC tuned circuit, an RC network, or an external clock source. The driv-

ing frequency must be at least 1 MHz, and must be twice the desired internal clock frequency; hence, the SAB 8085AH is operated with a 6 MHz crystal (for 3 MHz clock), and the SAB 8085AH-2 can be operated with a 10 MHz crystal (for 5 MHz clock).

If a crystal is used, it must have the following characteristics:

Parallel resonance at twice the clock frequency desired

 C_1 (load capacitance) $\leq 30 \text{ pF}$

 C_s (shunt capacitance) $\leq 7 \text{ pF}$

R_s (equivalent shunt resistance) ≤ 75 Ohms

Drive level: 10 mW

Frequency tolerance: ±.005% (suggested)

Note the use of the 20 pF capacitor between X_2 and ground. This capacitor is required with crystal frequencies below 4 MHz to assure oscillator startup at the correct frequency. A parallel-resonant LC circuit may be used as the frequency-determining network for the SAB 8085AH, providing that its frequency tolerance of approximately $\pm 10\%$ is acceptable. The components are from the formula:

$$f = \frac{1}{2 \pi \sqrt{L \left(C_{ext} + C_{int}\right)}}$$

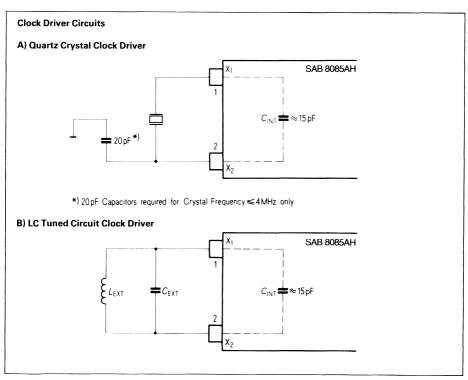
To minimize variations in frequency, it is recommended that you choose a value for C_{ext} that is at least twice that of C_{int} , or 30 pF. The use of an LC

circuit is not recommended for frequencies higher than approximately 5 MHz.

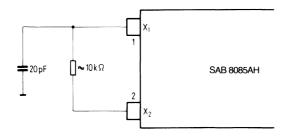
An RC circuit may be used as the frequency-determining network for the SAB 8085AH if maintaining a precise clock frequency is of no importance. Variations in the on-chip timing generation can cause a wide variation in frequency when using the RC mode. Its advantage is its low component costs. The driving frequency generated by the circuit shown is approximately 3 MHz. It is not recommended that frequencies greatly higher or lower than this be attempted.

The following figures show the recommended clock driver circuits. Note in D and E that pullup resistors are required to assure that the high level voltage of the input is at least 4V.

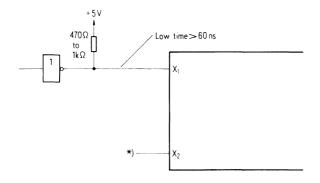
For driving frequencies up to and including 6 MHz you may supply the driving signal to X_1 and leave X_2 opencircuited (Figure D). If the driving frequency is from 6 MHz to 10 MHz, stability of the clock generator will be improved by driving both X_1 and X_2 with a pushpull source (Figure E). To prevent self-oscillation of the SAB 8085AH, be sure that X_2 is not coupled back to X_1 through the driving circuit.



C) RC Circuit Clock Driver

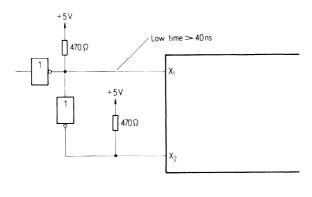


D) 1 - 6 MHz Input Frequency External Clock Driver Circuit



*) X₂ left floating

E) 1 – 10 MHz Input Frequency External Clock Driver Circuit



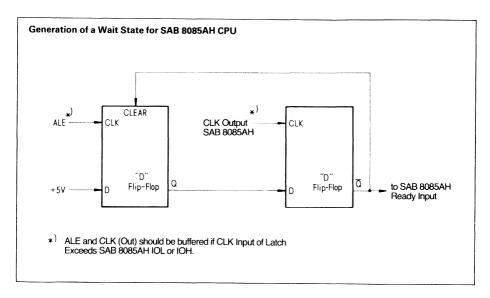
Generating Wait State

If your system requirements are such that slow memories or peripheral devices are being used, the circuit shown in the following figure may be used to insert one WAIT state in each SAB 8085AH machine cycle.

The D flip-flops should be chosen so that

- CLK is rising edge-triggered
- CLEAR is low-level active.

As in the SAB 8080, the READY line is used to extend the read and write pulse lengths so that the SAB 8085AH can be used with slow memory. HOLD causes the CPU to relinquish the bus when it is through with it by floating the Address and Data Buses.



System Interface

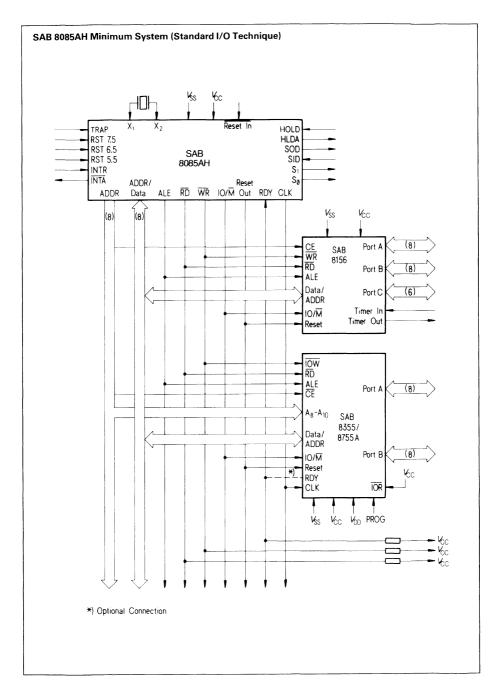
The SAB 8085A family includes memory components, which are directly compatible to the SAB 8085AH CPU. For example, a system consisting of the three chips, SAB 8085AH, SAB 8156, and SAB 8355 will have the following features:

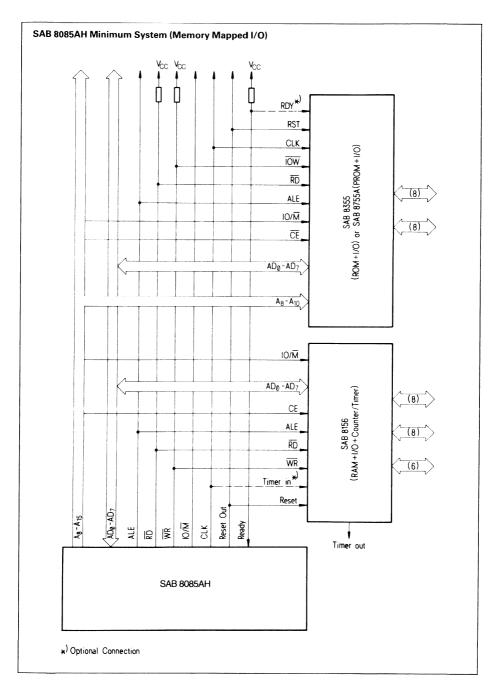
- 2K Bytes ROM
- 256 Bytes RAM
- 1 Timer/Counter
- 4 8-bit I/O Ports
- 1 6-bit I/O Port
- 4 Interrupt Levels
- Serial In/Serial Out Ports

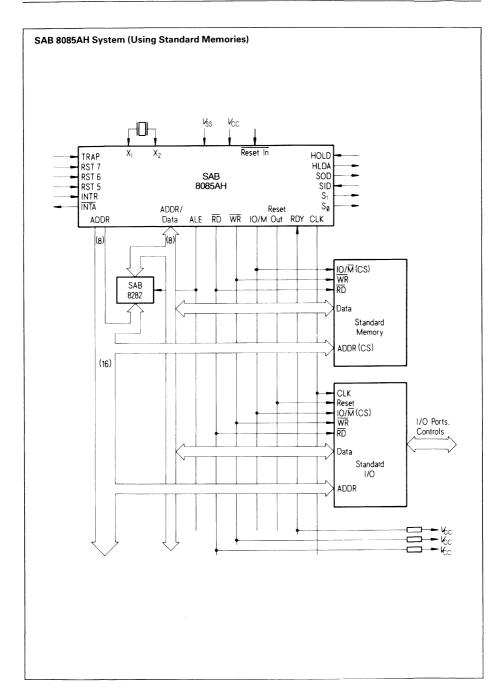
This minimum system, using the standard I/O technique is as shown in the following figure.

In addition to standard I/O, the memory mapped I/O offers an efficient I/O addressing technique. With this technique, an area of memory address space is assigned for I/O address, thereby, using the memory address for I/O manipulation. The figure on page 11 shows the system configuration of Memory Mapped I/O using SAB 8085AH.

The SAB 8085AH CPU can also interface with the standard memory that does **not** have the multiplexed address/data bus. It will require a simple SAB 8282 (8-bit latch) as shown in the figure on page 12.



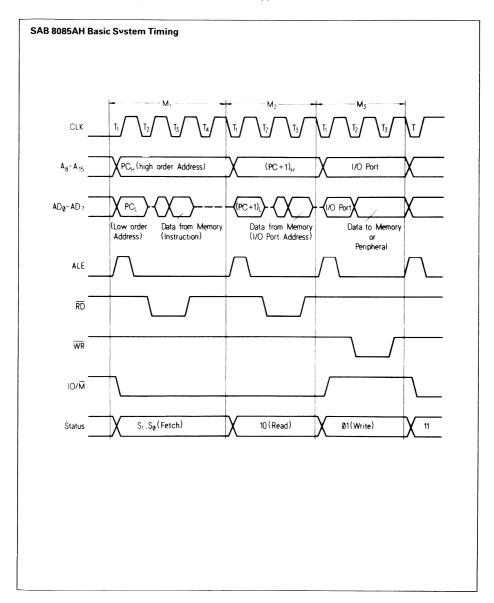




Basic System Timing

The SAB 8085AH has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8-bits of address on the Data Bus. The following figure shows an instruction fetch, memory read and I/O write

cycle (as would occur during processing of the OUT instruction). Note that during the I/O write and read cycle the I/O port address is copied on both, the upper and lower half of the address.



There are seven possible types of machine cycles. Which of these seven takes place is defined by the status of the three status lines (IO/ \overline{M} , S_1 , S_0) and the three control signals (\overline{RD} , \overline{WR} , and \overline{INTA}); (see following table). The status lines can be used as advanced controls (for device selection, for example),

since they become active at the T_1 state, at the outset of each maching cycle. Control lines $R\bar{D}$ and $W\bar{R}$ become active later, at the time when the transfer of data is to take place, so are used as command lines.

SAB 8085AH Machine Cycle Chart

		Status			Contro	Control			
Machine Cycle		IO/M	S1	SØ	RD	WR	ĪNTA		
Opcode Fetch	(OF)	Ø	1	1	Ø	1	1		
Memory Read		Ø	1	Ø	Ø	1	1		
Memory Write		Ø	Ø	1	1	Ø	1		
I/O Read	(IOR)	1	1	Ø	Ø	1	1		
I/O Write	(IOW)	1	Ø	1	1	Ø	1		
Acknowledge for INTR	(INA)	1	1	1	1	1	Ø		
Bus Idle	(BI): DAD ACK of	Ø	1	Ø	1	1	1		
	RST, TRAP	1	1	1	1	1	1		
	HALT	TS	Ø	Ø	TS	TS	1		

Ø = Logic "Ø"; 1 = Logic "1"; TS = High Impedance

A machine cycle normally consists of three T states, with the exception of OPCODE FETCH, which normally has either four or six T states (unless WAIT

or HOLD states are forced by the receipt of READY or HOLD inputs). Any T state must be one of ten possible states, as summarized in the following table.

SAB 8085AH Machine State Chart

Machine	Status ar	d Buses	Control	Control			
State	S1, SØ	IO/M	A ₈ -A ₁₅	AD _Ø -AD ₇	RD, WR	ĪŅTA	ALE
T ₁	X	X	Х	Х	1	1	1 1)
T ₂	x	l x	×	×	×	×	Ø
T _{WAIT}	×	l x	×	×	×	×	Ø
T ₃	x	×	×	×	x	×	Ø
T ₄	1	Ø ²)	×	TS	1	1	Ø
T ₅	1	Ø 2)	×	TS	1	1	Ø
T ₆	1	Ø 2)	l x	TS	1	1	Ø
T _{RESET}	×	TS	TS	TS	TS	1	Ø
THALT	Ø	TS	TS	TS	TS	1	Ø
T _{HOLD}	×	TS	TS	TS	TS	1	Ø

Ø = Logic "Ø"; 1 = Logic "1"; TS = High Impedance; X = Unspecified.

¹⁾ ALE not generated during 2nd and 3nd machine cycles of DAD instruction.

²) $IO/\overline{M} = 1$ during T_4-T_6 of INA machine cycle.

Instruction Set Summary

Instruction Code									Operations			
Mnemonic	D ₇	D_6	D_5	D_4	D_3	D_2	D_1	D_{\emptyset}	Description			
MOVE, LOAD, A	ND S	TOR	Ē									
MOVr1 r2	Ø	1	D	D	D	S	S	S	Move register to register			
MOV M.r	Ø	1	1	1	Ø	S	S	S	Move register to memory			
MOV r.M	Ø	1	D	D	D	1	1	Ø	Move memory to register			
MVI r	Ø	Ø	D	D	D	1	1	Ø	Move immediate register			
MVIM	Ø	Ø	1	1	Ø	1	1	Ø	Move immediate memory			
LXI B	Ø	Ø	Ø	Ø	Ø	Ø	Ø	1	Load immediate register Pair B & C			
LXI D	Ø	Ø	Ø	1	Ø	Ø	Ø	1	Load immediate register Pair D & E			
LXIH	Ø	Ø	1	Ø	Ø	Ø	Ø	1	Load immediate register Pair H & L			
STAX B	Ø	Ø	Ø	Ø	Ø	Ø	1	Ø	Store A indirect			
STAX D	Ø	Ø	Ø	1	Ø	Ø	1	Ø	Store A indirect			
LDAX B	Ø	Ø	Ø	Ø	1	Ø	1	Ø	Load A indirect			
LDAX D	Ø	Ø	Ø	1	1	Ø	1	Ø	Load A indirect			
STA	Ø	Ø	1	1	Ø	Ø	1	Ø	Store A direct			
LDA	Ø	Ø	1	1	1	Ø	1	Ø	Load A direct			
SHLD	Ø	Ø	1	Ø	Ø	Ø	1	Ø	Store H & L direct			
LHLD	Ø	Ø	1	Ø	1	Ø	1	Ø	Load H & L direct			
XCHG	1	1	1	Ø	1	Ø	1	1	Exchange D & E, H & L Registers			
STACK OPS												
PUSH B	1	1	Ø	Ø	Ø	1	Ø	1	Push register Pair B & C on stack			
PUSH D	1	1	ø	1	ő	1	ő	1	Push register Pair D & E on stack			
PUSH H	1	1	1	ø	ø	1	ø	1	Push register Pair H & L on stack			
PUSH PSW	1	1	1	1	ő	1	ø	1	Push A and Flags on stack			
POP B	1	1	ø	ø	ø	Ø	ø	1	Pop register Pair B & C off stack			
POP D	1	1	ø	1	ø	Ø	ø	1	Pop register Pair D & E off stack			
POP H	1	1	1	ø	ø	ø	ø	1	Pop register Pair H & L off stack			
POP PSW	1	1	1	1	ø	ø	ø	1	Pop A and Flags off stack			
XTHL	1	1	1	ø	ø	ø	1	1	Exchange top of stack, H & L			
SPHL	1	1	1	1	1	ø	ø	1	H & L to stack pointer			
LXISP	Ø	ø	1	1	ø	ø	ø	1	Load immediate stack pointer			
INX SP	ő	ø	1	1	ø	ø	1	1	Increment stack pointer			
DCX SP	Ø	ø	1	1	1	ø	1	1	Decrement stack pointer			
JUMP												
JMP	1	1	Ø	Ø	Ø	Ø	1	1	Jump unconditional			
JC	1	1	ø	1	1	ø	1	Ø	Jump on carry			
JNC	1	1	ø	1	Ø	Ø	1	Ø	Jump on no carry			
JZ	1	1	ø	Ø	1	Ø	1	Ø	Jump on zero			
JNZ	1	1	ø	ø	Ø	ø	1	Ø	Jump on no zero			
JP	1	1	1	1	ø	ø	1	Ø	Jump on positive			
JM	1	1	1	1	1	ø	1	ø	Jump on minus			
JPE	1	1	1	ø	1	ø	1	ø	Jump on parity even			
JPO	1	1	1	ø	ø	ø	1	Ø	Jump on perity odd			
PCHL	1	1	1	ø	1	ø	ø	1	Jump on perity odd H & L to program counter			

Instruction Set Summary (Cont'd)

			ln	struc	tion (Code			Operations		
Mnemonic	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_{\emptyset}	Description		
CALL											
CALL	1	1	Ø	Ø	1	1	Ø	1	Call unconditional		
CC	1	1	ø	1	1	1	ø	Ø	Call on carry		
CNC	1	1	ø	1	Ø	1	ø	ø	Call on no carry		
cz	1	1	ø	Ø	1	1	Ø	ø	Call on zero		
CNZ	1	1	ø	ø	ø	1	Ø	ø	Call on no zero		
CP I	1	1	1	1	Ø	1	Ø	ø	Call on positive		
CM	1	1	1	1	1	1	ø	ø	Call on minus		
CPE	1	1	1	Ø	1	1	Ø	ø	Call on parity even		
CPO	1	1	1	Ø	Ø	1	Ø	Ø	Call on parity odd		
RETURN								,			
RET	1	1	Ø	Ø	1	Ø	Ø	1	Return		
RC	1	1	Ø	1	1	Ø	Ø	Ø	Return on carry		
RNC	1	1	Ø	1	Ø	Ø	Ø	Ø	Return on no carry		
RZ	1	1	Ø	Ø	1	Ø	Ø	Ø	Return on zero		
RNZ	1	1	Ø	Ø	Ø	Ø	Ø	Ø	Return on no zero		
RP	1	1	1	1	Ø	Ø	Ø	Ø	Return on positive		
RM	1	1	1	1	1	Ø	Ø	Ø	Return on minus		
RPE	1	1	1	Ø	1	Ø	Ø	Ø	Return on parity even		
RPO	1	1	1	Ø	Ø	Ø	Ø	Ø	Return on parity odd		
RESTART											
RST	1	1	Α	Α	Α	1	1	1	Restart		
INPUT/OUTPUT											
IN	1	1	Ø	1	1	Ø	1	1	Input		
OUT	1	1	Ø	1	Ø	Ø	1	1	Output		
INCREMENT AND) DE	CREN	1ENT								
INR r	Ø	Ø	D	D	D	1	Ø	Ø	Increment register		
DCR r	Ø	Ø	D	D	D	1	Ø	1	Decrement register		
INR M	Ø	Ø	1	1	Ø	1	Ø	Ø	Increment memory		
DCR M	Ø	Ø	1	1	Ø	1	Ø	1	Decrement memory		
INX B	Ø	Ø	Ø	Ø	Ø	Ø	1	1	Increment B & C registers		
INX D	Ø	Ø	Ø	1	Ø	Ø	1	1	Increment D & E registers		
INX H	Ø	Ø	1	Ø	Ø	Ø	1	1	Increment H & L registers		
DCX B	Ø	Ø	Ø	Ø	1	Ø	1	1	Decrement B & C		
DCX D	Ø	Ø	Ø	1	1	Ø	1	1	Decrement D & E		
DCX H	Ø	Ø	1	Ø	1	Ø	1	1	Decrement H & L		
ADD											
ADD r	1	Ø	Ø	Ø	Ø	S	S	S	Add register to A		
ADC r	1	Ø	Ø	Ø	1	S	S	S	Add register to A with carry		
ADD M	1	Ø	C	Ø	Ø	1	1	Ø	Add memory to A		
ADC M	1	Ø	Ø	Ø	1	1	1	Ø	Add memory to A with carry		
ADI	1	1	Ø	Ø	Ø	1	1	Ø	Add immediate to A		
ACI	1	1	Ø	Ø	1	1	1	Ø	Add immediate to A with carry		
	Α.	Ø	Ø	Ø	1	Ø	Ø	1	Add B & C to H & L		
DAD B	Ø	v	v	ν.					1		
DAD B DAD D	Ø	ø	ø	1	1	Ø	Ø	1	Add D & E to H & L		
									1		

Instruction Set Summary (Cont'd)

			ı	nstru	ction	Code	:	Operations	
Mnemonic	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	Dø	Description
SUBTRACT									
SUB r	1	Ø	Ø	1	Ø	S	S	S	Subtract register from A
SBB r	1	Ø	Ø	1	1	S	S	S	Subtract register from A with borrow
SUB M	1	Ø	Ø	1	Ø	1	1	Ø	Subtract memory from A
SBB M	1	Ø	Ø	1	1	1	1	Ø	Subtract memory from A with borrow
SUI	1	1	Ø	1	Ø	1	1	Ø	Subtract immediate from A
SBI	1	1	Ø	1	1	1	1	Ø	Subtract immediate from A with borrow
LOGICAL									
ANA r	1	Ø	1	Ø	Ø	S	s	S	And register with A
XRA r	1	Ø	1	Ø	1	S	S	S	Exclusive OR register with A
ORA r	1	Ø	1	1	Ø	S	S	S	OR register with A
CMP r	1	ø	1	1	1	S	S	S	Compare register with A
ANA M	1	Ø	1	Ø	Ø	1	1	Ø	And memory with A
XRA M	1	ø	1	ø	1	1	1	ø	Exclusive OR memory with A
ORA M	1	ø	1	1	Ø	1	1	ø	OR memory with A
CMP M	1	ő	1	1	1	1	1	ø	Compare memory with A
ANI	1	1	1	ø	ø	1	1	ø	And immediate with A
XRI	1	1	1	ø	1	1	1	ø	Exclusive OR immediate with A
ORI	1	1	1	1	ø	1	1	ø	OR immediate with A
CPI	1	i	1	1	1	1	1	ø	Compare immediate with A
ROTATE									
RLC	Ø	Ø	Ø	Ø	Ø	1	1	1	Rotate A left
RRC	Ø	Ø	Ø	Ø	1	1	1	1	Rotate A right
RAL	Ø	Ø	Ø	1	Ø	1	1	1	Rotate A left throught carry
RAR	Ø	Ø	Ø	1	1	1	1	1	Rotate A right through carry
SPECIALS									
СМА	Ø	Ø	1	Ø	1	1	1	1	Complement A
STC	Ø	Ø	1	1	Ø	1	1	1	Set carry
CMC	Ø	ø	1	1	1	1	1	1	Complement carry
DAA	Ø	Ø	1	Ø	Ø	1	1	1	Decimal adjust A
CONTROL									
EI	1	1	1	1	1	Ø	1	1	Enable interrupts
DI	1	1	1	1	Ø	Ø	1	1	Disable Interrupt
NOP	Ø	Ø	Ø	Ø	Ø	ø	Ø	Ø	No-operation
HLT	ø	1	1	1	Ø	1	1	Ø	Halt
NEW SAB 8085	AH IN	STRU	CTIO	NS					
RIM	ΙØ	Ø	1	Ø	Ø	Ø	Ø	Ø	Read Interrupt Mask
SIM	Ιō	ø	1	1	ø	Ø	Ø	Ø	Set Interrupt Mask

NOTES

- 1. DDS or SSS: B 000, C 001, D 010, E 011, H 100, L 101, Memory 110, A 111.
- 2. Two possible cycle times (6/12) indicate instruction cycles dependent on condition flags.

^{*} All mnemonic copyrighted © Intel Corporation 1976.

SAB 8085AH

Absolute maximum ratings *)

 $\begin{array}{lll} \mbox{Ambient Temperature Under Bias} & 0 \ \mbox{to } 70^{\circ}\mbox{C} \\ \mbox{Storage Temperature} & -65 \ \mbox{to } +150^{\circ}\mbox{C} \\ \mbox{Voltage on any Pin with Respect to Ground} & -0.5 \ \mbox{to } +7 \ \mbox{V} \\ \end{array}$

Power Dissipation 1.5 Watt

D.C. Characteristics

 $T_{A}=0$ to 70°C; $V_{CC}=5\,V\,\pm10\%$; $V_{SS}=0\,V$; (unless otherwise specified)

Symbol	Parameter	Limi	t Values	Units	Test Conditions
		Min.	Max.		
V _{IL}	Input Low Voltage	-0.5	+0.8		
V _{IH}	Input High Voltage	2.0	V _{CC} +0.5	$]_{v}$	
V _{OL}	Output Low Voltage	-	0.45]	$I_{OL} = 2 \text{ mA}$
V _{OH}	Output High Voltage	2.4	-		$I_{OH} = -400\ \muA$
I _{cc}	Power Supply Current		120	mA	_
I_{IL}	Input Leakage		± 10	μА	$0 \leqslant V_{\text{IN}} \leqslant V_{\text{CC}}$
I_{LO}	Output Leakage				$0.45\mathrm{V} \leqslant V_{\mathrm{OUT}} \leqslant V_{\mathrm{CC}}$
V _{ILR}	Input Low Level, RESET	-0.5	+0.8		
V _{IHR}	Input High Level, RESET	2.4	V _{CC} +0.5	v	_
V _{HY}	Hysteresis, RESET	0.25			

^{*)} Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

A.C. Characteristics

 $T_{A}=0$ to 70°C; $V_{CC}=5\,V\,\pm\,10\%$; $V_{SS}=0\,V$

Symbol	Parameter	Limit Values				Units
		SAB 8085AH ²⁾		SAB 8085AH-2 ²⁾		
		Min.	Max.	Min.	Max.	1
t_{CYC}	CLK Cycle Period	320	2000	200	2000	
t ₁	CLK Low Time (Standard CLK Loading)	80		40		
$\overline{t_2}$	CLK High Time Standard CLK Loading)	120		70		
t_r , t_t	CLK Rise and Fall Time		30	-	30	
t_{XKR}	X ₁ Rising to CLK Rising	30	120	30	100	
t _{XKF}	X₁ Rising to CLK Falling	30	150	30	110	
t _{AC}	A ₈ -A ₁₅ Valid to Leading Edge of Control ¹⁾	270		115	-	
t _{ACL}	A ₀ -A ₇ Valid to Leading Edge of Control	240				
t _{AD}	A ₀ -A ₁₅ Valid to Valid Data In		575	_	350	
t _{AFR}	Address Float After Leading Edge of READ (INTA)	-	0		0	
t _{AL}	A ₈ -A ₁₅ Valid Before Trailing Edge of ALE ¹⁾	115	_	50	-	
t _{ALL}	A ₀ -A ₇ Valid Before Trailing Edge of ALE	90				
t _{ARY}	READY Valid from Address Valid	-	220	-	100	ns
t _{CA}	Address (A ₈ -A ₁₅) Valid After Control	120		60		
$t_{\rm CC}$	Width of Control Low (RD, WR, INTA)	400		230		
t_{CL}	Trailing Edge of Control to Leading Edge of ALE	50		25		
t_{DW}	Data Valid to Trailing Edge of WRITE	420		230		
t _{HABE}	HLDA to Bus Enable	_ 210	210	_	150	
t _{HABF}	Bus Float After HLDA			_ 100		
t _{HACK}	HLDA Valid to Trailing Edge of CLK	110		40		
t_{HDH}	HOLD Hold Time	0		0		
t _{HDS}	HOLD Setup Time to Trailing Edge of CLK	170		120	7	
t _{INH}	INTR Hold Time	0		0		
t _{INS}	INTR, RST, and TRAP Setup Time to Falling Edge of CLK	160	_	150	_	
t _{LA}	Address Hold Time After ALE	100		50		
t_{LC}	Trailing Edge of ALE to Leading Edge of Control	130	60			
t _{LCK}	ALE Low During CLK High	100	7	50		

Notes see next page.

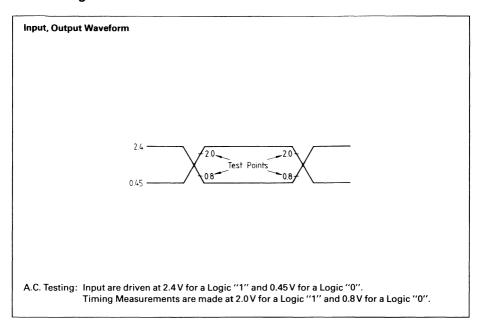
A.C. Characteristics (continued)

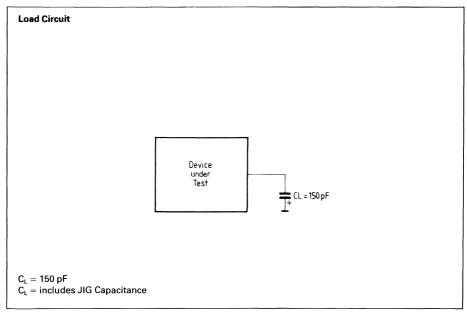
Symbol	Parameter	Limit Values				Units
		SAB 8085AH ²⁾		SAB 8085AH-2 ²⁾		1
		Min.	Max.	Min.	Max.	1
t_{LDR}	ALE to Valid Data During Read		460		270	
t_{LDW}	ALE to Valid Data During Write		200	7	120	
t _{LL}	ALE Width	140	-	80	-	
t _{LRY}	ALE to READY Stable	_	110	-	30	1
t _{RAE}	Trailing Edge of READ to Re-Enabling of Address	150	-	90	-	
t_{RD}	READ (or INTA) to Valid Data	-	300	-	150	
t _{RV}	Control Trailing Edge to Leading Edge of Next Control	400		220		ns
t _{RDH}	Data Hold Time After READ INTA ⁷⁾	0	-	0	_	ns
t _{RYH}	READY Hold Time					
t _{RYS}	READY Setup Time to Leading Edge of CLK	110		100	7	
t _{wD}	Data Valid After Trailing Edge of WRITE	100		60		
t_{WDL}	LEADING Edge of WRITE to Data Valid	_	40	_	20	1

NOTES

- 1. $A_8 A_{15}$ address Specs apply to IO/\overline{M} , S_0 , and S_1 except $A_8 A_{15}$ are undefined during $T_4 T_6$ of OF cycle, whereas IO/\overline{M} , S_0 , and S_1 are stable.
- 2. **Test conditions**: $t_{CYC} = 320 \text{ ns}$ (SAB 8085AH)/200 ns (SAB 8085AH-2); $C_L = 150 \text{ pF}$.
- 3. For all output timings where $C_L=150$ pF use the following correction factors: 25 pF $\le C_L < 150$ pF: -0.10 ns/pF 150 pF $< C_L \le 300$ pF: +0.30 ns/pF
- 4. Output timings are measured with purely capacitive load.
- 5. All timings are measured at output votage $V_L = 0.8V$, $V_H = 2.0V$, and 1.5V with 20 ns rise and fall time on inputs.
- 6. To calculate timing specifications at other values of $t_{\mathtt{CYC}}$ the following table should be used.
- 7. Data hold time is guaranteed under all loading conditions.

A.C. Testing





Bus Timing Specification as a $t_{\rm CYC}$ Dependent SAB 8085AH

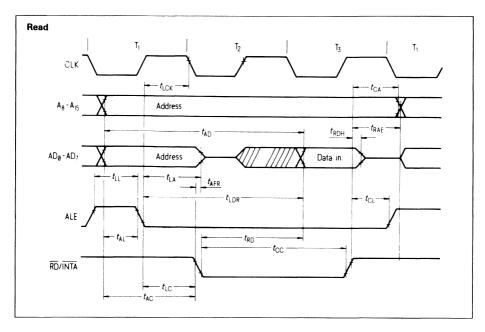
Symb. Min. Max. (1/2) T - 45 t_{AL} (1/2) T - 60 t_{LA} $t_{\rm LL}$ (1/2) T - 20(1/2) T - 60 t_{LCK} (1/2) T - 30 t_{LC} (5/2 + N) T - 225 t_{AD} (3/2 + N) T - 180 t_{RD} (1/2) T - 10 t_{RAE} (1/2) T - 40 t_{CA} (3/2 + N) T - 60 t_{DW} $t_{\rm WD}$ (1/2) T - 60(3/2 + N) T - 80 t_{CC} (1/2) T - 110 t_{CL} (3/2) T - 260 t_{ARY} (1/2) T - 50 t_{HACK} t_{HABF} (1/2) T + 50(1/2) T + 50 t_{HABE} (2/2) T - 50 t_{AC} t₁ (1/2) T - 80(1/2) T - 40 t_2 (3/2) T - 80 $t_{\sf RV}$ (4/2) T - 180 t_{LDR}

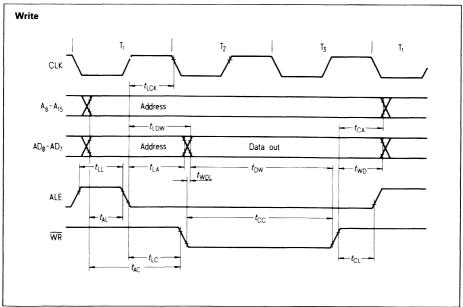
SAB 8085AH-2

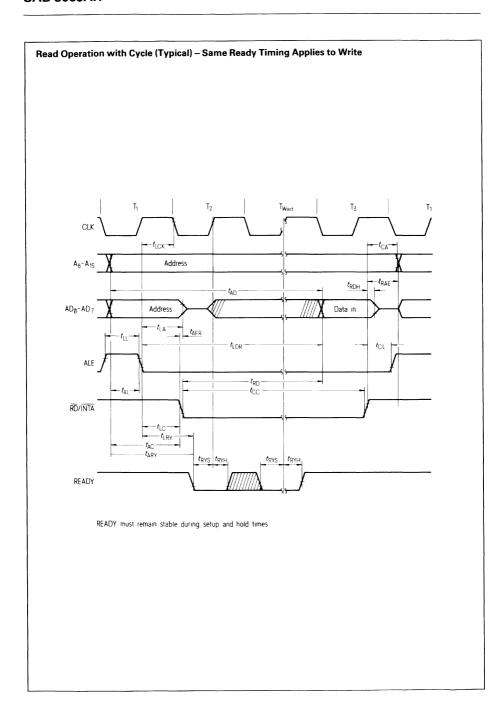
Symb.	Min.	Max.
t_{AL}	(1/2) T - 50	
t _{LA}	(1/2) T - 50	
t _{LL}	(1/2) T - 20	_
t _{LCK}	(1/2) T - 50	
t _{LC}	(1/2) T — 40	
t _{AD}		(5/2 + N) T - 150
t _{RD}		(3/2 + N) T - 150
t _{RAE}	(1/2) T — 10	
t _{CA}	(1/2) T - 40	
t _{DW}	(3/2 + N) T - 70	_
t _{WD}	(1/2) T - 40	
t _{CC}	(3/2 + N) T - 70	
t _{CL}	(1/2) T - 75	
t _{ARY}	_	(3/2) T - 200
t _{HACK}	(1/2) T - 60	_
t _{HABF}		(1/2) T + 50
t _{HABE}		(1/2) T + 50
t _{AC}	(2/2) T — 85	
t ₁	(1/2) T - 60	_
t ₂	(1/2) T - 30	
t _{RV}	(3/2) T - 80	
t _{LDR}	-	(4/2) T - 130

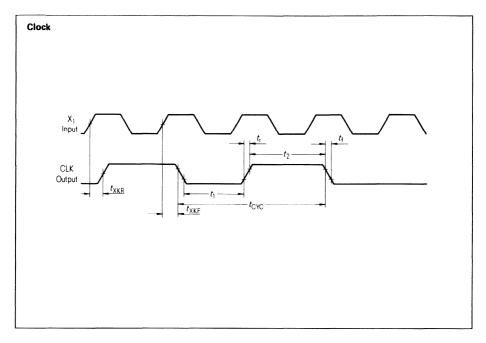
N is equal to the total WAIT states. T = t_{CYC}

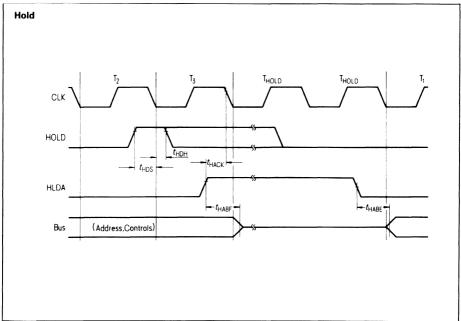
Waveforms

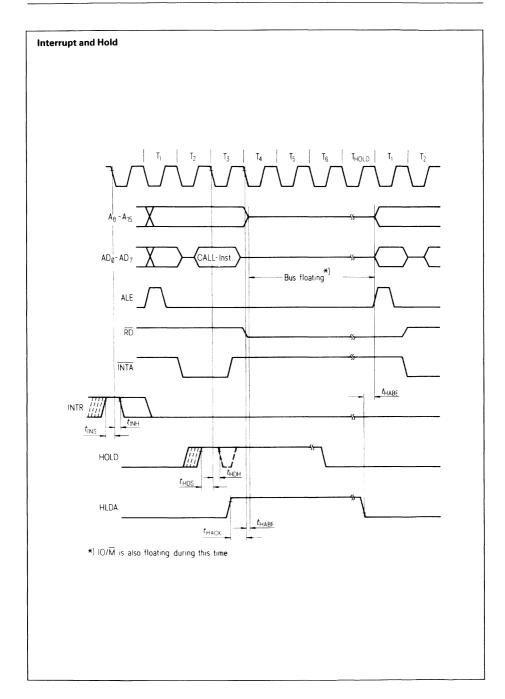




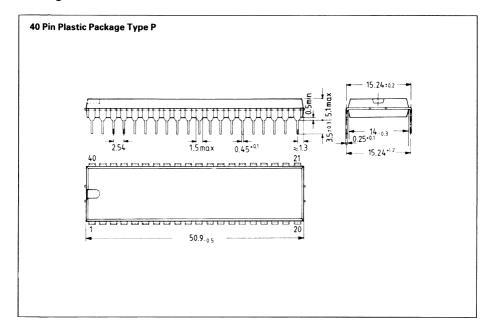








Package Outline



SAB 8085AH

Ordering Information

Component	Description	Ordering code
	8-Bit Microprocessor	
SAB 8085AH-P	3 MHz, 1.3 μs, (plastic)	Q 67120-C122
SAB 8085AH-2-P	5 MHz, 0.8 μs, (plastic)	Q 67120-C124

SAB 8086 16-Bit Microprocessor

SAB 8086-2 8 MHz **SAB 8086-1** 10 MHz

- Direct Addressing Capability to 1 MByte of Memory
- Assembly Language Compatible with SAB 8080 / SAB 8085
- 14 Word, By 16-Bit Register Set with Symmetrical Operations
- 8- and 16-Bit Signed and Unsigned Arithmetic in Binary or Decimal Including Multiply and Divide

SAB 8086 5 MHz

- Bit, Byte, Word, and Block Operations
- 24 Operand Addressing Modes
- Clock Rate upto10 MHz (SAB 8086-1)
- Compatible with Industry Standard 8086
- In plastic and ceramic package

Figure 1.	Pin Diagram	Figure 2.	Pin Names		
GND (40 D V _{CC}	AD _{Ø-15}	Address/Data	A ₁₆₋₁₉	Address
AD ₁₄ 2	39 🗀 AD ₁₅	Š₀-2	Status	S ₃₋₇	Status
AD ₁₃ 3	38 A ₁₆ /S ₃	INTR	Interrupt Request	BHE	Bus High Enable
AD ₁₇ 4	37 A ₁₇ /S ₄	CLK	Clock	HOLD	Hold
AD ₁₀ 5 AD ₁₀ 6	36 A ₁₈ /S ₅ 35 A ₇₆ /S ₆	QS ₀₋₁	Queue Status	HLDA	Hold Acknowledge
AD ₀ 7	34 T BHE/S-	TEST	Test for Busy	WR	Write
AD ₈ B	33 MN/MX	READY	Ready	DT/R	Bus Driver Transmit/
AD, 3	32 🗆 🗺	RESET	Chip Reset		Receive
AD ₆ 10 SAB	31 🗆 RO /GT _e (HOLD)	MN/\overline{MX}	Minimum/Maximum	DEN	Bus Driver Enable
AD ₅ □ 11 8086	JOE KONSTITUTION		Mode	ALE	Address Latch Enable
AD ₄ 🖂 12	29 DOCK (WR)	RD	Read	INTA	Interrupt Acknowledg
AD ₃ 🔲 13	28 3 ₇ (M/iÖ)	$\overline{RQ}/\overline{GT}_{0-1}$		NMI	Non-maskable
AD ₂ 14	27 S, (DT/R)	LOCK	Bus Lock		Interrupt
AD ₁	26 3 (OEN) 25 0 05¢ (ALE)	M/ IO	Memory/IO	GND	Ground
NMI 17	24 QS, (INTA)			V _{cc}	+5 Volts
NTR 18	23 TEST		l	1.00	1.0.00
CLK 19	22 READY				
GND 20	21 RESET				

SAB 8086 is a new generation, high performance 16-bit Microprocessor implemented in +5 Volts, depletion load, N channel, silicon gate Siemens MYMOS technology packaged in a 40 pin package. It is 100 percent compatible with the industry

standard 8086. With features like string handling, 16-bit arithmetic with multiply and divide it significantly increases system performance. It is highly suited for multiprocessor applications in various configurations.

Functional Pin Definition

The following pin function descriptions are for SAB 8086 systems in either minimum or maximum mode. The "Local Bus" in these descriptions is

the direct multiplexed bus interface connection to the SAB 8086 (without regard to additional bus buffers).

Number	Symbol	Input (I) Output (O)	Function		
2-16 39	AD ₀ -AD ₁₅	1/0	These lines constitute the time multiplexed memory I/O address (T_1) and data (T_2, T_3, T_4) bus. A_0 is analogous to BHE for the lower byte of the data bus, pins $D_7 - D_0$. It is LOW during T_1 when a byte is to be transferred on the lower portion of the bus in memory or I/O operations. Eight-bit oriented devices tied to the lower half would normally use A_0 to condition chip select functions. These lines are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus "hold acknowledge"		
35–38	A ₁₆ /S ₃ A ₁₇ /S ₄ A ₁₈ /S ₅ A ₁₉ /S ₆	0	During T_1 these are the four most significant address liftor memory operations. During I/O operations these liare LOW. During memory and I/O operations, status information is available on these lines during T_2 , T_3 , T_w , T_4 . The status of the interrupt enable FLAG bit (S_5) is updated at the beginning of each CLK cycle. A_{17}/S_4 and A_{16}/S_3 are encoded as follows:		tions. During I/O operations these lines nemory and I/O operations, status ilable on these lines during T ₂ , T ₃ , T _w and ne interrupt enable FLAG bit (S ₅) is ginning of each CLK cycle.
			A ₁₇ /S ₄	A_{16}/S_3	Characteristics
			0 (LOW) 0 1 (HIGH) 1 S ₆ is 0 (LOW)	0 1 0 1	Alternate Data Stack Code or None Data
			presently	being us	ndicates which relocation register is sed for data accessing. o 3-state OFF during local bus "hold
34	BHE/S,	0	During T ₁ the bus high enable signal (\overline{BHE}) should be used to enable data onto the most significant half of the data bus, pins D ₁₅ —D ₈ . Eight-bit oriented devices tied to the upper half of the bus would normally use \overline{BHE} to condition chip select functions. \overline{BHE} is LOW during T ₁ for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the high portion of the bus. The S ₇ status information is available during T ₂ , T ₃ , and T ₄ . The signal is active LOW, and floats to 3-state OFF in "hold". It is LOW during T ₁ for the first interrupt acknowledge cycle.		
32	RD	0			

Number	Symbol	Input (I) Output (O)	Function
22	READY	l	READY is the acknowledgement from the addressed memory or I/O device that it will complete the data transfer. The RDY signal from memory I/O is synchronized by the SAB 8284A Clock Generator to form READY. This signal is active HIGH. The SAB 8086 READY input is not synchronized. Correct operation is not guaranteed if the setup and hold times are not met.
18	INTR	I	Interrupt request is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software reseting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH.
23	TEST	I	The TEST input is examined by the "Wait" instruction. If the TEST input is LOW execution continues, otherwise the processor waits in an "Idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.
17	NMI	I	Non-maskable interrupt is an edge triggered input which causes a type 2 interrupt. A subroutine is vectored to via interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from a LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.
21	RESET	ı	RESET causes the processor to immediately terminate its present activity. The signal must be active HIGH for at least four clock cycles. It restarts execution, as described in the Instruction Set description, when RESET returns LOW. RESET is internally synchronized.
19	CLK	I	The clock provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.
33	MN/MX	ı	Minimum/Maximum: indicates what mode the processor is to operate in. The two modes are discussed in the following sections.
40	V _{cc}		+5V (power supply)
1, 20	GND		GND (ground)

The following pin function descriptions are for the SAB 8086/8288 system in **maximum mode** (i. e. $MN/\overline{MX} = GND$). Only the pin functions which are

unique to maximum mode are described; all other pin functions are as already described.

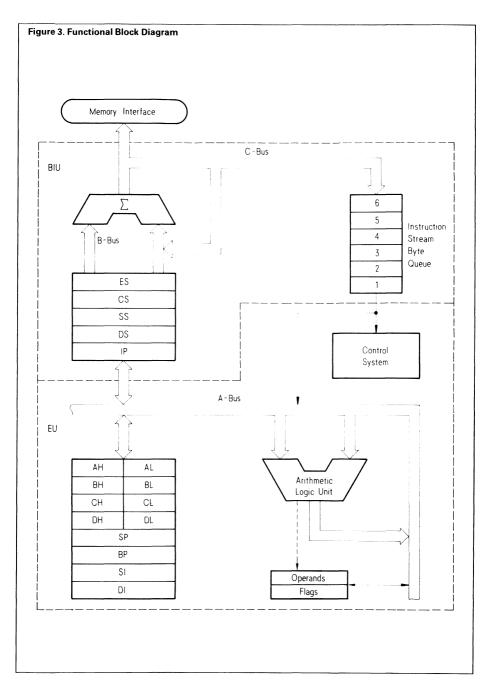
Number	Symbol	Input (I) Output (O)	Function	Function			
26-28	$\overline{S}_2, \overline{S}_1, \overline{S}_0$	0	These status lines are encoded as follows:				
			S ₂	S ₁	Sø	Characteristics	
			0 (LOW) 0 0 1 (HIGH) 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0	Interrupt Acknowledge Read I/O Port Write I/O Port Halt Code Access Read Memory Write Memory Passive	
			Status is active during T ₄ , T ₁ , and T ₂ and is returned to the passive state (1,1,1) during T ₃ or during T _w when READY is HIGH. This status is used by the SAB 8288 Bus Controller to generate all memory and I/O access control signals. Any change by S ₂ , S ₁ , or S ₀ during T ₄ is used to indicate the beginning of a bus cycle, and the return to the passive state in T ₃ or T _w is used to indicate the end of a bus cycle. These signals float to 3-state OFF in "hold acknowledge".				
30-31	RQ/GT₀, RQ/GT₁	1/0	The request/grant pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bidirectional with RO/GT_0 having higher priority than RO/GT_1 . RO/GT has an internal pull-up resistor so may be left unconnected. The request/grant sequence is as follows (see Figure 14):				
						another local bus master t (''hold'') to the SAB 8086	
			the SAB 808 indicates the to float and state at the	36 to the r at the SA that it wil next CLK. ed logical	equest B 8086 I enter The Cl	T_1 a pulse 1 CLK wide from ing master (pulse 2) has allowed the local bus the 'hold acknowledge'' PU's bus interface unit is the local bus during 'hold	
			3. A pulse 1 CLK wide from the requesting master indicates to the SAB 8086 (pulse 3) that the "hold" request is about to end and that the SAB 8086 can reclaim the local bus at the next CLK.				
			Each master-master exchange of the local bus is a sequence of 3 pulses. There must be one dead CLK cycle after each bus exchange. Pulses are active LOW.				
			If the request is made while the CPU is performing a memory cycle, it will release the local bus during T_4 of the cycle when all the following conditions are met:				
			address). 3. Current cycl acknowledg	le is not th le is not th je sequen	ne low ie first a ice.	. T ₂ . byte of a word (on an odd acknowledge of an interrupt urrently executing.	

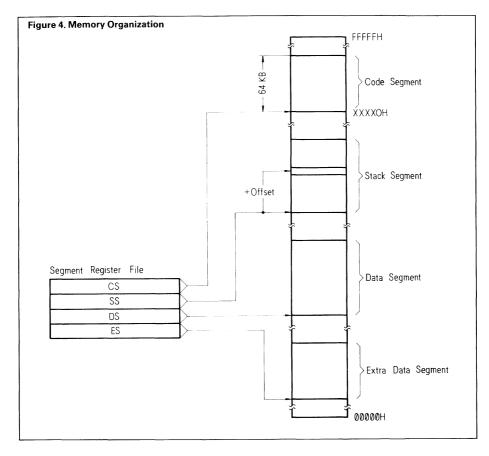
Number	Symbol	Input (I) Output (O)	Function			
29	LOCK	0	The LOCK output indicates that other system bus masters are not to gain control of the system bus while LOCK is active LOW. The LOCK signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and floats to 3-state OFF in "hold acknowledge".			
24-25	QS₁, QS∅	0	QS_1 and QS_0 provide status to allow external tracking of the internal SAB 8086 instruction queue.			
			QS ₁	QS ₀	Characteristics	
			0 (LOW) 0 1 (HIGH)	0 1 0 1	No Operation First Byte of Op Code from Queue Empty the Queue Subsequent Byte from Queue	
			The queue statu which the queue		during the CLK cycle after on is performed.	

The following pin function descriptions are for the SAB 8086 **minimum mode** (i. e. $MN/\overline{MX} = V_{CC}$). Only the pin functions which are unique to

minimum mode are described; all other pin functions are as described before.

Number	Symbol	Input (I) Output (O)	Function
28	M/ĪŌ	0	This status line is logically equivalent to S $_2$ in the maximum mode. It is used to distinguish a memory access from an I/O access. M/\overline{D} becomes valid in the T $_4$ preceding a bus cycle and remains valid until the final T $_4$ of the cycle (M = HIGH, IO = LOW). M/\overline{D} floats to 3-state OFF in local bus "hold acknowledge".
29	WR	0	Write strobe indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the M/\overline{IO} signal. \overline{WR} is active for T_2 , T_3 and T_w of any write cycle. It is active LOW, and floats to 3-state OFF in local bus "hold acknowledge".
24	ĪNTĀ	0	$\overline{\text{INTA}}$ is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T_2 , T_3 and T_w of each interrupt acknowledge cycle.
25	ALE	0	Address latch enable is provided by the processor to latch the address into the SAB 8282/SAB 8283 address latch. It is a HIGH pulse active during T ₁ of any bus cycle. Note that ALE is never floated.
27	DT/R	0	Data transmit/receive is needed in minimum system that desires to use a SAB 8286/SAB 8287 data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically DT/\overline{R} is equivalent to S_1 in the maximum mode, and its timing is the same as for M/\overline{IO} . (T=HIGH, R=LOW). This signal floats to 3-state OFF in local bus "hold acknowledge".
26	DEN	0	Data enable is provided as an output enable for the SAB 8286/SAB 8287 in a minimum system which uses the transceiver. \overline{DEN} is active LOW during each memory and I/O access and for INTA cycles. For a read or INTA cycle it is active from the middle of T_2 until the middle of T_4 , while for a write cycle it is active from the beginning of T_2 until the middle of T_4 . \overline{DEN} floats to 3-state OFF in local bus "hold acknowledge".
30-31	HOLD HLDA	lo	HOLD indicates that another master is requesting a local bus "hold". To be acknowledged, HOLD must be active HIGH. The processor receiving the "hold" request will issue HLDA (HIGH) as an acknowledgement in the middle of T_a or T_i . Simultaneous with the issuance of HLDA the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor will lower HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. HOLD is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the setup time. The same rules as for $\overline{RQ}/\overline{GT}$ apply regarding when the local bus will be released.





Functional Description

The internal functions of the SAB 8086 processor are partitioned logically into two processing units. The first is the Bus Interface Unit (BIU) and the second is the Execution Unit (EU) as shown in the block diagram of Figure 3.

The bus interface unit provides the functions related to instruction fetching and queuing, operand fetch and store, and address relocation. The overlap of instruction pre-fetching provided by this unit serves to increase processor performance through improved bus bandwidth utilization. Up to 6 bytes of the instruction stream can be queued while waiting for decoding and execution.

The instruction stream queuing mechanism allows the BIU to keep the memory utilized very efficiently. Whenever there is space for at least 2 bytes in the queue, the BIU will attempt a word fetch memory cycle. This greatly reduces "dead time" on the memory bus.

The execution unit receives pre-fetched instructions from the BIU queue and provides un-relocated operand addresses to the BIU. Memory operands are passed through the BIU for processing by the EU, which passes results to the BIU for storage.

The processor provides a 20-bit address to memory which locates the byte being referenced. The memory is logically organized as a linear array of 1 million bytes, addressed as 00000(H) to FFFF(H). The memory can be further logically divided into code, data, alternate data, and stack segments of up to 64 Kbytes each, with each segment falling on 16-byte boundaries. (See Figure 4)

Minimum and Maximum Modes

The requirements for supporting minimum and maximum SAB 8086 systems are sufficiently different that they cannot be done efficiently with 40 uniquely defined pins. Consequently, the SAB 8086 is equipped with a strap pin (MN/\overline{MX}) which defines the system configuration.

The definition of a certain subset of the pins changes dependent on the condition of the strap pin.

When MN/ \overline{MX} pin is strapped to GND, the SAB 8086 treats pins 24 through 31 in maximum mode. An SAB 8288 bus controller interprets status information coded into \overline{S}_{θ} , \overline{S}_{1} , \overline{S}_{2} to generate bus timing and control signals.

When the MN/\overline{MX} pin is strapped to V_{CC} , the SAB 8086 generates bus control signals itself on pins 24 through 31, as shown in parentheses in Figure 1.

Bus Operation

The SAB 8086 has a combined address and data bus commonly referred to as a time multiplexed bus.

Each processor bus cycle consists of at least four CLK cycles. These are referred to as T_1 , T_2 , T_3 and T_4 (see Figure 5). The address is emitted from the processor during T_1 and data transfer occurs on the bus during T_3 and T_4 . T_2 is used primarily for changing the direction of the bus during read operations. In the event that a "NOT READY" indication is given by the addressed device, "Wait" states (T_w) are inserted between T_3 and T_4 . Each inserted "Wait" state is of the same duration as a CLK cycle. Periods can occur between SAB 8086 bus cycles. These are referred to as "Idle" states (T_i) or inactive CLK cycles. The processor uses these cycles for internal housekeeping.

During T_1 of any bus cycle the ALE (Address Latch Enable) signal is emitted (by either the processor or the SAB 8288 bus controller, depending on the MN/ \overline{MX} strap). At the trailing edge of this pulse, a valid address and certain status information for the cycle may be latched.

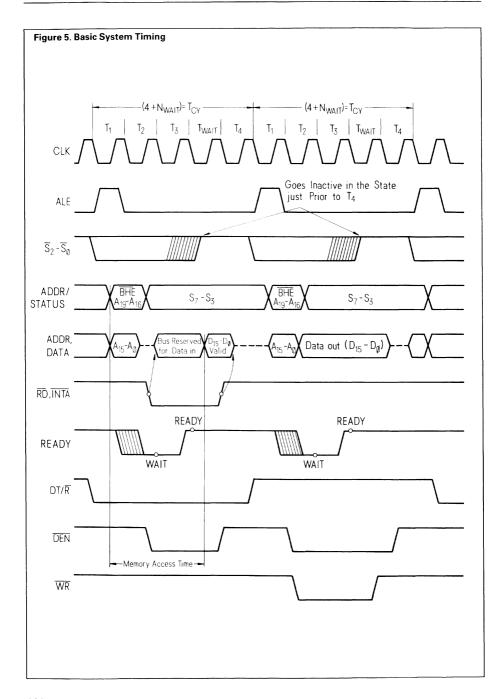
Status bits $\overline{S_0}$, $\overline{S_1}$, and $\overline{S_2}$ are used, in maximum mode, by the bus controller to identify the type of bus transaction according to the following table:

\overline{S}_2	ĪS ₁	Ŝ₀	Characteristics
0 (LOW)	0	0	Interrupt Acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1 (HIGH)	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

Status bits S_3 through S_7 are multiplexed with highorder address bits and the \overline{BHE} signal, and are therefore valid during T_2 through T_4 . S_3 and S_4 indicate which segment register (see Instruction Set description) was used for this bus cycle in forming the address, according to the following table:

S ₄	S₃	Characteristics
0 (LOW)	0	Alternate Data (extra segment)
0	1	Stack
1 (HIGH)	0	Code or None
1	1	Data

 S_5 is a reflection of the PSW interrupt enable bit. $S_6 = 0$ and S_7 is a spare status bit.



I/O Addressing

In the SAB 8086, I/O operations can address up to a maximum of 64 K I/O byte registers or 32 K I/O word registers.

The I/O address appears in the same format as the memory address on bus lines A_{15} – A_{0} . The address lines A_{19} – A_{16} are zero in I/O operations.

The variable I/O instructions which use register DX as a pointer have full address capability while the direct I/O instructions directly address one or two of the 256 I/O byte locations in page 0 of the I/O address space.

System Components

Processors

SAB 8088 - 100% Compatible CPU with SAB 8086

with 8-bit bus

SAB 8087 - Numeric Data Processor. Coprocessor

to SAB 8086 and SAB 8088.

SAB 8089 - Input / Output Processor.

Support Circuits

SAB 8282 Octal Latch

SAB 8283 Octal Latch (Inverting)

SAB 8284A Clock Generator and Driver

SAB 8286 Octal Bus Transceiver

SAB 8287 Octal Bus Transceiver (Inverting)

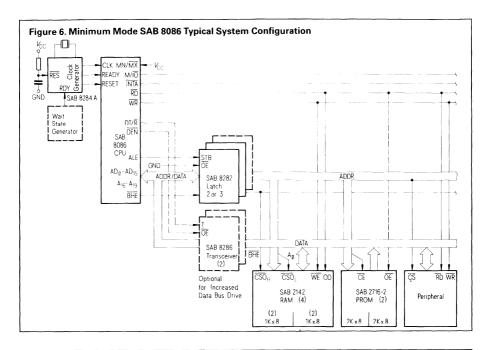
SAB 8288 Bus Controller

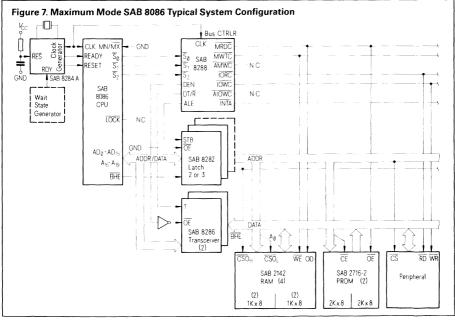
SAB 8289 Bus Arbiter

SAB 8259A Programmable Interrupt Controller

Typical Applications

SAB 8086 is a general purpose 16-bit microprocessor which can be used for applications ranging from process control to data processing. Figures 6 and 7 show typical system configurations for SAB 8086 familiy components.





Instruction Set Summary

DATA TRANSFER MOV = Move

76543210 76543210 76543210 76543210

Register / memory to / from register

Immediate to register/memory

Immediate to register

Memory to accumulator

Accumulator to memory

Register/memory to segment register

Segment register to register/memory

100010dw	mod reg r/m		
1100011w	mod 0 0 0 r/m	data	data if w=1
1011w reg	data	data if w=1	
1010000w	addr-low	addr-high	
1010001w	addr-low	addr-high	
10001110	mod 0 reg r/m		

PUSH = Push:

Register/memory

11111111 mod 110 r/m

mod 0 reg r/m

Register

01010 reg

10001100

Segment register

000 reg 110

POP = Pop:

Register/memory

1000**1**111 mod 000 r/m

Register

01011 reg

Segment register

000 reg 111

XCHG = Exchange:

Register/memory with register

1000011w mod reg r/m

Register with accumulator

10010 reg

IN = Input from:

Fixed port

1110010w port

Variable port

1110110w

OUT = Output to:

76543210 76543210 76543210 76543210

Fixed port 1110011w port

Variable port 1110111w

XLAT = Translate byte to AL 11010111

 LDS = Load pointer to DS
 11000101 mod reg r/m

 LES = Load pointer to ES
 11000100 mod reg r/m

LAHF = Load AH with flags

SAHF = Store AH into flags 10011110

PUSHF = Push flags 10011100

POPF = Pop flags 10011101

ARITHMETIC ADD = Add:

Reg./memory with register to either

Immediate to register/memory

Immediate to accumulator

00000dw	mod reg r/m		
100000sw	mod 0 0 0 r/m	data	data if s: w=01
0000010w	data	data if w=1	

ADC = Add with carry:

Reg./memory with register to either

Immediate to register/memory

Immediate to accumulator

000100dw	mod reg r/m		
100000sw	mod 0 1 0 r/m	data	data if s:w=01
0001010w	data	data if w=1	

INC = Increment:

Register/memory 1111111 w mod 0 0 0 r/m

Register 0 1 0 0 0 reg

AAA = ASCII adjust for add 0 0 1 1 0 1 1 1

DAA = Decimal adjust for add 0 0 1 0 0 1 1 1

SUB = Subtract:

Reg./memory and register to either Immediate from register/memory Immediate from accumulator

76543210 76543210 76543210 76543210

001010dw	mod reg r/m		
100000sw	mod 1 0 1 r/m	data	data if s:w=01
0010110w	data	data if w=1	

SBB = Subtract with borrow

Reg./memory and register to either Immediate from register/memory Immediate from accumulator

000110dw	mod reg r/m		
100000sw	mod 0 1 1 r/m	data	data if s:w=01
0001110w	data	data if w=1	

DEC = Decrement:

Register/memory
Register

NEG = Change sign

76543210 76543210 76543210 76543210

1111111 w mod 0 0 1 r/m
0 1 0 0 1 reg

1111011 w mod 0 1 1 r/m

10011001

CMP = Compare:

Register/memory and register

Immediate with register/memory

Immediate with accumulator

AAS = ASCII adjust for subtract

DAS = Decimal adjust for subtract

MUL = Multiply (unsigned)

IMUL = Integer multiply (signed)

AAM = ASCII adjust for multiply

DIV = Divide (unsigned)

IDIV = Integer divide (signed)

AAD = ASCII adjust for divide

CBW = Convert byte to word

CWD = Convert word to double word

		mod reg r/m	001110dw
data if s:w=0	data	mod 1 1 1 r/m	100000sw
	data if w=1	data	0011110w
-			00111111
			00101111
		mod 1 0 0 r/m	1111011w
		mod 1 0 1 r/m	1111011w
		00001010	11010100
		mod 1 1 0 r/m	1111011w
		mod 1 1 1 r/m	1111011w
		00001010	11010101
			10011000

NOT = Invert SHL/SAL = Shift logical/arithmetic left SHR = Shift logical right I10100vw mod 101r/m SAR = Shift arithmetic right ROL = Rotate left I10100vw mod 101r/m ROR = Rotate right I10100vw mod 000r/m RCR = Rotate through carry flag left RCR = Rotate through carry right I10100vw mod 010r/m RCR = Rotate through carry right I10100vw mod 010r/m RCR = Rotate through carry right I10100vw mod 010r/m AND = And: Reg/memory and register to either Immediate to register/memory Immediate to accumulator Immediate data and register memory Immediate data and register memory Immediate data and accumulator Interest = And function to flags, no result: Register/memory and register Immediate data and accumulator Interest = And function to flags, no result: Regimemory and register Immediate data and accumulator Interest = And function to flags, no result: Regimemory and register o either Immediate data and accumulator Interest = And function to flags, no result: Regimemory and register memory Immediate data and accumulator Interest = And function to flags, no result: Regimemory and register memory Immediate data and register memory Immediate data and accumulator Interest = And function to flags, no result: Regimemory and register to either Immediate to register/memory Immediate to register/memory Immediate to register memory Immediate to register	LOGIC	76543210	76543210	76543210	76543210
SHR = Shift logical right SAR = Shift arithmetic right ROL = Rotate left 110100vw mod 101r/m ROL = Rotate right ROL = Rotate through carry flag left RCL = Rotate through carry right 110100vw mod 010r/m RCL = Rotate through carry right 110100vw mod 011r/m AND = And: Reg/memory and register to either Immediate to register/memory Immediate to accumulator TEST = And function to flags, no result: Register/memory and register Immediate data and register/memory Immediate data and register/memory Immediate data and register/memory Immediate data and register to either OR = Or: Reg/memory and register to either Immediate to register/memory Immediate to register to either O000110 dw mod reg r/m Immediate to register/memory Immediate to register to either O000110 dw mod reg r/m Immediate to register/memory Immediate to register to either O01100 dw mod reg r/m Immediate to register/memory Immediate to register to either O01100 dw mod reg r/m Immediate to register/memory Immediate to register/memory Immediate to register/memory Immediate to register to either O01100 dw mod reg r/m Immediate to register/memory	NOT = Invert	1111011w	mod 0 1 0 r/m		
SAR = Shift arithmetic right ROL = Rotate left 110100vw mod 111r/m ROR = Rotate right 110100vw mod 000r/m RCR = Rotate through carry flag left RCR = Rotate through carry right 110100vw mod 010r/m RCR = Rotate through carry right 110100vw mod 011r/m AND = And: Reg/memory and register to either Immediate to accumulator 100000w mod 100r/m data data if w=1 TEST = And function to flags, no result: Register/memory and register Immediate data and accumulator 101010w mod reg r/m Immediate data and accumulator 101010w mod reg r/m Immediate data and accumulator 101010w mod reg r/m Immediate data and accumulator OR = Or: Reg/memory and register to either Immediate to register/memory Immediate to accumulator 000010dw mod reg r/m Immediate to register/memory Immediate to accumulator 000010dw mod reg r/m Immediate to accumulator 0000110w data data if w=1 XOR = Exclusive or: Reg./memory and register to either Immediate to register/memory 1000000w mod reg r/m 1000000w mod reg r/m 10000010w data data if w=1 XOR = Exclusive or: Reg./memory and register to either Immediate to register/memory 1000000w mod reg r/m	SHL/SAL = Shift logical/arithmetic left	110100vw	mod 1 0 0 r/m		
ROL = Rotate left ROR = Rotate right RICL = Rotate through carry flag left RCR = Rotate through carry right RICL = Rotate through carry mod 0 11 r/m AND = Ricl is reference of the result	SHR = Shift logical right	110100vw	mod 1 0 1 r/m		
ROR = Rotate right RCL = Rotate through carry flag left RCR = Rotate through carry right 110100vw mod 010r/m RCR = Rotate through carry right 110100vw mod 011r/m AND = And: Reg/memory and register to either Immediate to register/memory Immediate to accumulator 1001000w mod 100r/m data data if w=1 Immediate data and register/memory Immediate data and register/memory Immediate data and accumulator Reg/memory and register Immediate data and accumulator OR = Or: Reg/memory and register to either Immediate to register/memory I	SAR = Shift arithmetic right	110100vw	mod 1 1 1 r/m		
RCL = Rotate through carry flag left RCR = Rotate through carry right 110100 v w mod 010 r/m RCR = Rotate through carry right 110100 v w mod 011 r/m AND = And: Reg/memory and register to either Immediate to register/memory Immediate to accumulator TEST = And function to flags, no result: Register/memory and register Immediate data and register/memory Immediate data and accumulator Reg/memory and register Induor 100000 w mod 100 r/m data data if w=1 Immediate data and accumulator TEST = And function to flags, no result: Register/memory and register Induor 100000 w mod reg r/m Immediate data and accumulator Reg/memory and register to either Immediate to register/memory Immediate to register/memory Immediate to accumulator Reg./memory and register to either Reg./memory and register to either Immediate to register/memory Immediate to accumulator Reg./memory and register to either Immediate to register/memory Immediate to regis	ROL = Rotate left	110100vw	mod 0 0 0 r/m		
AND = And: Reg/memory and register to either	ROR = Rotate right	110100vw	mod 0 0 1 r/m		
AND = And: Reg/memory and register to either Immediate to register/memory Immediate to accumulator TEST = And function to flags, no result: Register/memory and register Immediate data and register/memory Immediate data and register/memory Immediate data and accumulator TEST = And function to flags, no result: Register/memory and register Inmediate data and register/memory Immediate data and accumulator TEST = And function to flags, no result: Register/memory and register Inmediate data and register/memory Inmediate data and accumulator TEST = And function to flags, no result: Inmediate data and register/memory Inmediate data and register/memory Inmediate data and register/memory Inmediate to register/memory Inmediate to register/memory Inmediate to register to either Inmediate to register to either Inmediate to register/memory Inmediate to register to either Inmediate to register/memory Inmediate to register to either Inmediate to register/memory Inmediate to register/memory Inmediate to register to either Inmediate to register/memory Inmediate to register to either Inmediate to register/memory Inmediate to register/memory Inmediate to register to either Inmediate to r	RCL = Rotate through carry flag left	110100vw	mod 0 1 0 r/m		
Reg/memory and register to either Immediate to register/memory Immediate to accumulator TEST = And function to flags, no result: Register/memory and register Immediate data and register/memory Immediate data and accumulator OR = Or: Reg/memory and register to either Immediate to register/memory Immediate to register/memory Immediate to register/memory Immediate to register/memory Immediate to register to either Immediate to accumulator OR = Exclusive or: Reg./memory and register to either Immediate to register/memory Immediate to register to either Immediate to register to either Immediate to accumulator OR = Exclusive or: Reg./memory and register to either Immediate to register/memory Immediate to register to either	RCR = Rotate through carry right	110100vw	mod 0 1 1 r/m		
Reg/memory and register to either Immediate to register/memory Immediate to accumulator TEST = And function to flags, no result: Register/memory and register Immediate data and register/memory Immediate data and accumulator OR = Or: Reg/memory and register to either Immediate to register/memory Immediate to register/memory Immediate to register/memory Immediate to register/memory Immediate to register to either Immediate to accumulator OR = Exclusive or: Reg./memory and register to either Immediate to register/memory Immediate to register to either Immediate to register to either Immediate to accumulator OR = Exclusive or: Reg./memory and register to either Immediate to register/memory Immediate to register to either					
Immediate to register/memory Immediate to accumulator TEST = And function to flags, no result: Register/memory and register Immediate data and register/memory Immediate data and accumulator TEST = And function to flags, no result: Register/memory and register Immediate data and register/memory Immediate data and accumulator TEST = And function to flags, no result: Register/memory and register Immediate data and register/memory Immediate data and accumulator TEST = And function to flags, no result: Immediate data and register Immediate data and register/memory Immediate data and register/memory Immediate to register/memory Immediate to register/memory Immediate to accumulator TEST = And function to flags, no result: Immediate data if w=1 Immediate data and register for either Immediate to register/memory Immediate data and register for either Immediate to register/memory Immediate data and register for either Immediate to register/memory Immediate data and register for either Immediate for register for either Immediate for register/memory Immediate for register for either	AND = And:				
TEST = And function to flags, no result: Register/memory and register Immediate data and accumulator OR = Or: Reg/memory and register to either Immediate to register/memory TO 00010 w mod reg r/m Indicate data and accumulator OR = Or: Reg/memory and register to either Immediate to register/memory Immediate to accumulator OR = Cr: Reg/memory and register to either Immediate to register/memory Immediate to accumulator OR = Cr: Reg/memory and register to either Immediate to register/memory Immediate to accumulator OR = Cr: Immediate to register/memory Immediate to register/memory Immediate to accumulator OR = Cr: Immediate to register/memory Immediate to accumulator OR = Cr: Immediate to register/memory Immediate to register to either Immediate to register/memory	Reg/memory and register to either	001000dw	mod reg r/m		
TEST = And function to flags, no result: Register/memory and register Immediate data and register/memory Immediate data and accumulator OR = Or: Reg/memory and register to either Immediate to register/memory Immediate to accumulator OO 0010 dw mod reg r/m Immediate to register/memory Immediate to accumulator TO 00000 w mod 001 r/m data data if w=1 Immediate to accumulator OO 00110 w data data if w=1 XOR = Exclusive or: Reg./memory and register to either Immediate to register/memory In 00000 w mod reg r/m Immediate to register to either Immediate to register / memory Immediate / memory I	Immediate to register/memory	1000000w	mod 1 0 0 r/m	data	data if w=1
Register/memory and register Immediate data and register/memory Immediate data and accumulator OR = Or: Reg/memory and register to either Immediate to register/memory Immediate to accumulator NOR = Exclusive or: Reg./memory and register to either Immediate to register/memory Immediate to register to either Immediate to accumulator OO00110 w mod reg r/m Indicate to accumulator OO00110 w mod 001 r/m data data if w=1 OO00110 w mod reg r/m Immediate to accumulator OO01110 w data data if w=1 Immediate to register to either Immediate to register/memory Indicate to register to either Immediate to register/memory	Immediate to accumulator	0010010w	data	data if w=1	
Register/memory and register Immediate data and register/memory Immediate data and accumulator OR = Or: Reg/memory and register to either Immediate to register/memory Immediate to accumulator NOR = Exclusive or: Reg./memory and register to either Immediate to register/memory Immediate to register to either Immediate to accumulator OO00110 w mod reg r/m Indicate to accumulator OO00110 w mod 001 r/m data data if w=1 OO00110 w mod reg r/m Immediate to accumulator OO01110 w data data if w=1 Immediate to register to either Immediate to register/memory Indicate to register to either Immediate to register/memory					
Immediate data and register/memory Immediate data and accumulator OR = Or: Reg/memory and register to either Immediate to register/memory Immediate to accumulator Immed	$TEST = And \ function \ to \ flags, \ no \ result:$				
Immediate data and accumulator 1010100w data data if w=1 OR = Or: Reg/memory and register to either Immediate to register/memory Immediate to accumulator XOR = Exclusive or: Reg./memory and register to either Immediate to register/memory 1000000w mod 001r/m data data if w=1 XOR = Exclusive or: Reg./memory and register to either Immediate to register/memory 1000000w mod 110r/m data data if w=1	Register/memory and register	1000010w	mod reg r/m		
OR = Or: Reg/memory and register to either Immediate to register/memory Immediate to accumulator XOR = Exclusive or: Reg./memory and register to either Immediate to register/memory In 0 0 0 0 0 1 0 d w mod reg r/m Immediate to accumulator O 0 0 1 1 0 w data data if w=1 XOR = Exclusive or: Reg./memory and register to either Immediate to register/memory In 0 0 0 0 0 0 w mod 1 1 0 r/m data data if w=1	Immediate data and register/memory	1111011w	mod 0 0 0 r/m	data	data if w=1
Reg/memory and register to either Immediate to register/memory Immediate to accumulator XOR = Exclusive or: Reg./memory and register to either Immediate to register/memory Immediate to register to either Immediate to register/memory	Immediate data and accumulator	1010100w	data	data if w=1	
Reg/memory and register to either Immediate to register/memory Immediate to accumulator XOR = Exclusive or: Reg./memory and register to either Immediate to register/memory Immediate to register to either Immediate to register/memory					
Immediate to register/memory Inmediate to accumulator Inmediate to a	OR = Or:		_	i	
Immediate to accumulator 0000110 w data data if w=1 XOR = Exclusive or: Reg./memory and register to either Immediate to register/memory 001100 d w mod reg r/m 1000000 w mod 110 r/m data data if w=1	Reg/memory and register to either	000010dw	mod reg r/m		
XOR = Exclusive or: Reg./memory and register to either Immediate to register/memory 001100dw mod reg r/m 1000000w mod 110r/m data data if w=1	Immediate to register/memory	1000000w	mod 0 0 1 r/m	data	data if w=1
Reg./memory and register to either 0 0 1 1 0 0 d w mod reg r/m Immediate to register/memory 1 0 0 0 0 0 w mod 1 1 0 r/m data data if w=1	Immediate to accumulator	0000110w	data	data if w=1	
Reg./memory and register to either 0 0 1 1 0 0 d w mod reg r/m Immediate to register/memory 1 0 0 0 0 0 w mod 1 1 0 r/m data data if w=1					
Immediate to register/memory 100000 w mod 110 r/m data data if w=1	XOR = Exclusive or:				
	Reg./memory and register to either	001100dw	mod reg r/m		
Immediate to accumulator	Immediate to register/memory	1000000w	mod 1 1 0 r/m	data	data if w=1
infinediate to accumulator	Immediate to accumulator	0011010w	data	data if w=1	

STRING MANIPULATION

76543210 76543210 76543210

REP =	Repeat
-------	--------

1111001z

MOVS = Move byte/word

1010010w

CMPS = Compare byte/word

1010011w

SCAS = Scan byte/word

1010111w

LODS = Load byte/word to AL/AX

1010110w

STDS = Store byte/word from AL/A

1010101w

CONTROL TRANSFER

CALL = Call:

Direct within segment

11101000 disp-low disp-high

Indirect within segment

11111111 mod 0 1 0 r/m

Direct intersegment

10011010 offset-low offset-high seg-low seg-high

Indirect intersegment

11111111 mod 0 1 1 r/m

JMP = Unconditional Jump:

Direct within segment

11101001 disp-low disp-high disp

Direct within segment short

11111111 mod 100 r/m

11101011

Indirect within segment

11101010 offset-low offset-high seg-low

seg-high

Direct intersegment

11111111 mod 101 r/m

Indirect intersegment

RET = Return from CALL:	76543210	76543210	76543210
Within segment	11000011		
Within seg. adding immed to SP	11000010	data-low	data-high
Intersegment	11001011		
Intersegment adding immediable to SP	11001010	data-low	data-high
JE/JZ = Jump on equal/zero	01110100	disp	
JL/JNGE = Jump on less/not greater or equal	01111100	disp]
JLE/JNG = Jump on less or equal/not greater	01111110	disp	
JB/JNAE = Jump on below/not above or equal	01110010	disp	
JBE/JNA = Jump on below or equal/ not above	01110110	disp]
JP/JPE = Jump on parity/parity even	01111010	disp	
JO = Jump on overflow	01110000	disp]
JS = Jump on sign	01111000	disp]
JNE/JNZ = Jump on not equal/not zero	01110101	disp	
JNL/JGE = Jump on not less/greater or equal	01111101	disp]
JNLE/JG = Jump on not less or equal/ greater	01111111	disp	
JNB/JAE = Jump on not below/above or equal	01110011	disp	
JNBE/JA = Jump on not below or equal/above	01110111	disp	
JNP/JPO = Jump on not par/par odd	01111011	disp	
JNO = Jump on not overflow	01110001	disp	
JNS = Jump on not sign	01111001	disp	
LOOP = Loop CX times	11100010	disp	
LOOPZ/LOOPE = Loop while zero/equal	11100001	disp	
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000	disp	
JCXZ = Jump on CX zero	11100011	disp	

INT = Interrupt	76543210	76543210
Type specified	11001101	type
Туре 3	11001100	
INTO = Interrupt on overflow	11001110	ĺ
IRET = Interrupt return	11001111	
PROCESSOR CONTROL		
CLC = Clear carry	11111000	
CMC = Complement carry	11110101	
STC = Set Carry	11111001	
CLD = Clear direction	11111100	
STD = Set direction	11111101	
CLI = Clear interrupt	11111010	
STI = Set interrupt	11111011	
HLT = Halt	11110100	
WAIT = Wait	10011011	
ESC = Escape (to external device)	11011xxx	mod x x x r/m
LOCK = Bus lock prefix	11110000	

Footnotes:

AL = 8-bit accumulator

AX = 16-bit accumulator

CX = Count register

DS = Data segment

ES = Extra segment

Above/below refers to unsigned value.

Greater = more positive;

Less = less positive (more negative) signed values

if d = 1 then "to" reg; if d = 0 then "from" reg

if w = 1 then word instruction; if w = 0 then byte

instruction

if mod = 11 then r/m is treated as a REG field if mod = 00 then DISP = 0*, disp-low and disp-high are absent

if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp high is absent

if mod = 10 then DISP = disp-high: disp low

if r/m = 000 then EA = (BX) + (SI) + DISP

if r/m = 001 then EA = (BX) + (DI) + DISP

if r/m = 0.10 then EA = (BP) + (SI) + DISP

if r/m = 010 then EA = (BP) + (DI) + DISP

if r/m = 100 then EA = (SI) + DISP

if r/m = 100 then EA = (DI) + DISP

if r/m = 110 then EA = (BP) + DISP*

if r/m = 111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (before data if required)

if s:w = 01 then 16-bits of immediate data from the operand

it s:w = 11 then an immediate data byte is sign extended to form the 16-bit operand

if v = 0 then "count" = 1; if v = 1 then "count" in (CL)

x = don't care

z is used for string primitives for comparsion with ZF FLAG

SEGMENT OVERRIDE PREFIX

0 0 1 reg 1 1 0

REG is assigned according to the following table

16-Bit (w=1)	8-Bit (w=0)	Segment
000 AX	000 AL	00 ES
001 CX	001 CL	01 CS
010 DX	010 DL	10 SS
011 BX	011 BL	11 DS
100 SP	100 AH	
101 BP	101 CH	
110 SI	110 DH	
111 DI	111 BH	

Instruction which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:

 $\begin{aligned} &\mathsf{FLAGS} = \mathsf{X} : \mathsf{X} : \mathsf{X} : \mathsf{X} : (\mathsf{OF}) : (\mathsf{DF}) : (\mathsf{IF}) : (\mathsf{FF}) : (\mathsf{SF}) : (\mathsf{ZF}) : \\ &\mathsf{X} : (\mathsf{AF}) : \mathsf{X} : (\mathsf{PF}) : \mathsf{X} : (\mathsf{CF}) \end{aligned}$

^{*}except if mod = 00 and r/m = 110 then EA = disp-high:disp-low.

Absolute maximum ratings *)

Ambient Temperature Under Bias $0 \text{ to } 70^{\circ}\text{C}$ Storage Temperature $-65 \text{ to } +150^{\circ}\text{C}$ Voltage on any Pin with Respect to Ground Power Dissipation -1.0 to +7V

D.C. Characteristics

SAB 8086: $T_A=0$ to 70°C, $V_{CC}=5$ V $\pm 10\%$ SAB 8086-1/8086-2: $T_A=0$ to 70°C, $V_{CC}=5$ V $\pm 5\%$

	ļ	Limit	Values			
Symbol	Parameter	Min.	Max.	Units	Test Conditions	
V _{IL}	Input Low Voltage	-0.5	+0.8			
V _{IH}	Input High Voltage	2.0	V _{CC} +0.5	V	_	
V _{OL}	Output Low Voltage	-	0.45	*	$I_{OL} = 2.0 \text{ mA}$	
V _{OH}	Output High Voltage	2.4	_		$I_{OH} = -400 \mu A$	
I _{cc}	Power Supply Current SAB 8086 SAB 8086-2 SAB 8086-1		340 350 360	mA	T _A = 25°C	
I _{LI}	Input Leakage Current		± 10	μΑ	$OV \le V_{IN} \le V_{CC}$	
I _{LO}	Output Leakage Current		- 10	μΔ	$0.45\mathrm{V} \leq V_{\mathrm{OUT}} \leq V_{\mathrm{CC}}$	
V _{CL}	Clock Input Low Voltage	-0.5	+0.6	v	_	
V _{CH}	Clock Input High Voltage	3.9	V _{cc} +1.0		_	
C _{IN}	Capacitance of Input Buffer (All input except AD ₀ – AD ₁₅ , RQ/GT)	_	15	pF	fc = 1 MHz	
C _{IO}	Capacitance of I/O Buffer (AD ₀ – AD ₁₅ , RQ/GT)			,		

^{*)} Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

A.C. Characteristics for SAB 8086/8086-2

SAB 8086: $T_A = 0$ to 70°C, $V_{CC} = 5 \text{ V} \pm 10\%$ SAB 8086-2: $T_A = 0$ to 70°C, $V_{CC} = 5 \text{ V} \pm 5\%$

Minimum Complexity System (Figures 8, 9, 12, 15) Timing Requirements

		Limit Values					
Symbol	Parameter	SAB 8086		SAB 8086-2		Units	Test Conditions
		Min.	Max.	Min.	Max.		
TCLCL	CLK Cycle Period SAB 8086	200	500	125	500		_
TCLCH	CLK Low Time	118		68			
TCHCL	CLK High Time	69]	44]		
TCH1CH2	CLK Rise Time		10		10		From 1.0 to 3.5 V
TCL2CL1	CLK Fall Time]_	10		'0		From 3.5 to 1.0 V
TDVCL	Data in Setup Time	30		20			
TCLDX	Data in Hold Time	10		10]	ns	
TR1VCL	RDY Setup Time into SAB 8284A 1) 2)	35		35			
TCLR1X	RDY Hold Time into SAB 8284A 1) 2)	0]_	0]_		_
TRYHCH	READY Setup Time into SAB 8086	118		68			
TCHRYX	READY Hold Time into SAB 8086	30	1	20			
TRYLCL	READY Inactive to CLK 3)	-8		-8]		
THVCH	HOLD Setup Time	35		20]		
TINVCH	INTR, NMI, TEST Setup Time ²)	30		15			
TILIH	Input Rise Time (Except CLK)		20		20		From 0.8 to 2.0 V
TIHIL	Input Fall Time (Except CLK)		12		12		From 2.0 to 0.8V

¹⁾ Signal at SAB 8284A shown for reference only.

²) Setup requirement for asynchronous signal only to guarantee recognition at next CLK.

³⁾ Applies only to T₂ state. (8 ns into T₃)

Timing Responses

		Limit Values					
Symbol	Parameter	SAB 8086		SAB 8086-2		Units	Test Conditions
		Min.	Max.	Min.	Max.	1	
TCLAV	Address Valid Delay	10	110	10	60		
TCLAX	Address Hold Time	110	_		-		
TCLAZ	Address Float Delay	TCLAX	80	TCLAX	50		
TLHLL	ALE Width	TCLCH-20	-	TCLCH-10	-		
TCLLH	ALE Active Delay		80		50		
TCHLL	ALE Inactive Delay		85	1	55		
TLLAX	Address Hold Time to ALE Inactive	TCHCL-10	-	TCHCL-10	-		
TCLDV	Data Valid Delay	10	110	10	60		C _L = 20 – 100 pF for all SAB 8086
TCHDX	Data Hold Time			10		ns	Outputs
TWHDX	Data Hold Time After WR	TCLCH-30	1	TCLCH-30	1	113	(In addition to SAB 8086
TCVCTV	Control Active Delay 1				70		self-load)
TCHCTV	Control Active Delay 2	10	110	10	60		
TCVCTX	Control Inactive Delay				70		
TAZRL	Address Float to READ Active	0	-	0	-		
TCLRL	RD Active Delay	10	165	10	100		
TCLRH	RD Inactive Delay		150	1	80		
TRHAV	RD Inactive to Next Address Active	TCLCL-45	-	TCLCL-40	-		
TCLHAV	HLDA Valid Delay	10	160	10	100		
TRLRH	RD Width	2TCLCL-75		2TCLCL-50			
TWLWH	WR Width	2TCLCL-60	_	2TCLCL-40]-		
TAVAL	Address Valid to ALE Low	TCLCH-60		TCLCH-40			
TOLOH	Output Rise Time		20		20		From 0.8 to 2.0V
TOHOL	Output Fall Time		12		12		From 2.0 to 0.8V

Max Mode System (Using SAB 8288 Bus Controller) (Figures 10-14) Timing Requirements

		Limit Values					
Symbol	Parameter	SAB 8086		SAB	8086-2	Units	Test Conditions
		Min.	Max.	Min.	Max.		
TCLCL	CLK Cycle Period SAB 8086	200	500	125	500		
TCLCH	CLK Low Time	118		68			_
TCHCL	CLK High Time	69		44			
TCH1CH2	CLK Rise Time	_	10	_	10		From 1.0 to 3.5 V
TCL2CL1	CLK Fall Time						From 3.5 to 1.0 V
TDVCL	Data In Setup Time	30		20		}	•
TCLDX	Data In Hold Time	10		10		ns	
TR1VCL	RDY Setup Time into SAB 8284A 1) 2)	35		35			
TCLR1X	RDY Hold Time into SAB 8284A ¹) ²)	0	_	0]_		_
TRYHCH	READY Setup Time into SAB 8086	118		68			
TCHRYX	READY Hold Time into SAB 8086	30		20			
TRYLCL	READY Inactive to CLK 4)	-8		-8			
TINVCH	Setup Time for Recognition (INTR, NMI, TEST) 2)	30		15			
TGVCH	RQ/GT Setup Time	1]		
TCHGX	RQ Hold Time into SAB 8086	40		30			
TILIH	Input Rise Time (Except CLK)		20		20		From 0.8 to 2.0 V
TIHIL	Input Fall Time (Except CLK)		12		12		From 2.0 to 0.8V

¹⁾ Signal at SAB 8284A or SAB 8288 shown for reference only.

²) Setup requirement for asynchronous signal only to guarantee recognition at next CLK.

³⁾ Applies only to T₃ and wait states.

⁴) Applies only to T_2 state (8 ns into T_3).

Timing Responses

	Parameter	Limit Values					
Symbol		SAB 8086		SAB 8086-2		Units	Test Conditions
		Min.	Max.	Min.	Max.	1	
TCLML	Command Active Delay 1)	10	35	10	35		
TCLMH	Command Inactive Delay 1)		33	10	35		
TRYHSH	READY Active to Status Passive ³)	_	110	_	65		
TCHSV	Status Active Delay			10	60	ns	$C_L=20-100~pF$ for all SAB 8086 Outputs (In addition to SAB 8086 self-load)
TCLSH	Status Inactive Delay	10	130		70		
TCLAV	Address Valid Delay	10	110	10	60		
TCLAX	Address Hold Time		_	1	-		
TCLAZ	Address Float Delay	TCLAX	80	TCLAX	50		
TSVLH	Status Valid to ALE High 1)			- 20	20		
TSVMCH	Status Valid to MCE High ¹)	_	20				
TCLLH	CLK Low to ALE Valid 1)						
TCLMCH	CLK Low to MCE High 1)						
TCHLL	ALE Inactive Delay 1)	4	15	4	15		
TCLDV	Data Valid Delay	10	110	10	60		
TCHDX	Data Hold Time	10	_	10	_		
TCVNV	Control Active Delay 1)	5	45	5	45		
TCVNX	Control Inactive Delay 1)	10	40		40		

 $^{^1)}$ Signal at SAB 8284A or SAB 8288 shown for reference only. $^2)$ Setup requirement for asynchronous signal only to guarantee recognition at next CLK. $^3)$ Applies only to T_3 and wait states. $^4)$ Applies only to T_2 state (8 ns into $\mathsf{T}_3)$.

SAB 8086

			Limit	Values			
Symbol	Parameter	SAB 8086		SAB 8086-2		Units	Test Conditions
		Min.	Max.	Min.	Max.	1	
TAZRL	Address Float to READ Active	0	_	0	_		
TCLRL	RD Active Delay	10	165	10	100		C _L = 20-100 pF for all SAB 8086
TCLRH	RD Inactive Delay		150] "	80		
TRHAV	RD Inactive to Next Address Active	TCLCL-45	-	TCLCL-40	-		
TCHDTL	Direction Control Active Delay 1)		50		50	ns	Outputs (In addition to SAB 8086
TCHDTH	Direction Control Inactive Delay 1)	1-	30	_	30		self-load)
TCLGL	GT Active Delay	0	85	0	50		
TCLGH	GT Inactive Delay	1	03		30		
TRLRH	RD Width	2TCLCL-75	_	2TCLCL-50	-		
TOLOH	Output Rise Time		20		20		From 0.8 to 2.0 V
TOHOL	Output Fall Time	1	12		12		From 2.0 to 0.8V

 $^{^1)}$ Signal at SAB 8284A or SAB 8288 shown for reference only. $^2)$ Setup requirement for asynchronous signal only to guarantee recognition at next CLK. $^3)$ Applies only to T_3 and wait states. $^4)$ Applies only to T_2 state (8 ns into T_3).

A.C. Characteristics for SAB 8086-1

 $T_A=0$ to 70°C, $V_{CC}=5V\pm5\%$

Minimum Complexity System (Figures 8, 9, 12, 15) Timing Requirements (Preliminary)

Cumbal	D	Limit Values			Test	
Symbol	Parameter	Min.	Max.	Units	Conditions	
TCLCL	CLK Cycle Period	100	500			
TCLCH	CLK Low Time	53			_	
TCHCL	CLK High Time	39				
TCH1CH2	CLK Rise Time		10		From 1.0 to 3.5V	
TCL1CL2	CLK Fall Time	7	10		From 3.5 to 1.0V	
TDVCL	Data in Setup Time	5		7		
TCLDX	Data in Hold Time	10			_	
TR1VCL	RDY Setup Time into SAB 8284A ¹) ²)	35		ns		
TCLR1X	RDY Hold Time into SAB 8284A ¹) ²)	0				
TRYHCH	READY Setup Time into SAB 8086	53	_			
TCHRYX	READY Hold Time into SAB 8086	20				
TRYLCL	READY Inactive to CLK ³)	-10				
THVCH	HOLD Setup Time	20				
TINVCH	INTR, NMI, TEST Setup Time 2)	15				
TILIH	Input Rise Time (Except CLK)		20		From 0.8 to 2.0V	
TILHIL	Input Fall Time (Except CLK)		12		From 2.0 to 0.8V	

¹) Signal at SAB 8284A shown for reference only.

²) Setup requirement for asynchronous signal only to guarantee recognition at next CLK.

³) Applies only to T_2 state. (8 ns into T_3)

SAB 8086

Timing Responses SAB 8086-1 (Preliminary)

Symbol	Parameter	Limit V	alues	11-1-1-1	Test Conditions
		Min.	Max.	Units	
TCLAV	Address Valid Delay		50		C _L = 20 – 100 pF for all SAB 8086 Outputs (In addition to SAB 8086 self-load)
TCLAX	Address Hold Time	10	_		
TCLAZ	Address Float Delay		40		
TLHLL	ALE Width	TCLCH-10	-		
TCLLH	ALE Active Delay		40	1	
TCHLL	ALE Inactive Delay		45		
TLLAX	Address Hold Time to ALE Inactive	TCHCL-10	_		
TCLDV	Data Valid Delay	10	50		
TCHDX	Data Hold Time				
TWHDX	Data Hold Time After WR	TCLCH-25			
TCVCTX	Control Active Delay 1	10	50	ns	
TCHCTV	Control Active Delay 2		45		
TCVCTX	Control Inactive Delay		50		
TAZRL	Address Float to READ Active	0	-		
TCLRL	RD Active Delay	10	70		
TCLRH	RD Inactive Delay		60		
TRHAV	RD Inactive to Next Address Active	TCLCL-35	-		
TCLHAV	HLDA Valid Delay	10	60		
TRLRH	RD Width	2TCLCL-40	40		
TWLWH	WR Width	2TCLCL-35	_		
TAVAL	Address Valid to ALE Low	TCLCH-35			
TOLOH	Output Rise Time		20		From 0.8 to 2.0V
TOHOL	Output Fall Time		12		From 2.0 to 0.8V

Max Mode System (Using SAB 8288 Bus Controller) (Figures 10-14) Timing Requirements SAB 8086-1 (Preliminary)

Symbol	Parameter	Lin	nit Values	Units	Test
Symbol	Parameter	Min.	Max.	Units	Conditions
TCLCL	CLK Cycle Period	100	500		
TCLCH	CLK Low Time	53			_
TCHCL	CLK High Time	39			
TCH1CH2	CLK Rise Time		10		From 1.0 to 3.5V
TCL2CL1	CLK Fall Time		10		From 3.5 to 1.0V
TDVCL	Data In Setup Time	5			
TCLDX	Data In Hold Time	10			
TR1VCL	RDY Setup Time into SAB 8284A ¹) ²)	35		7	
TCLR1X	RDY Hold Time into SAB 8284A ¹) ²)	0		ns	
TRYHCH	READY Setup Time into SAB 8086	53			
TCHRYX	READY Hold Time into SAB 8086	20			
TRYLCL	READY Inactive to CLK ³)	-10			
TINVCH	Setup Time for Recognition (INTR, NMI, TEST) ²)	15			
TGVCH	RQ/GT Setup Time	12			
TCHGX	RQ Hold Time into SAB 8086	20			
TILIH	Input Rise Time (Except CLK)		20		From 0.8 to 2.0V
TIHIL	Input Fall Time (Except CLK)	1	12		From 2.0 to 0.8V

¹⁾ Signal at SAB 8284A or SAB 8288 shown for reference only.

²) Setup requirement for asynchronous signal only to guarantee recognition at next CLK.

³) Applies only to T_2 state (8 ns into T_3).

SAB 8086

Timing Responses SAB 8086-1 (Preliminary)

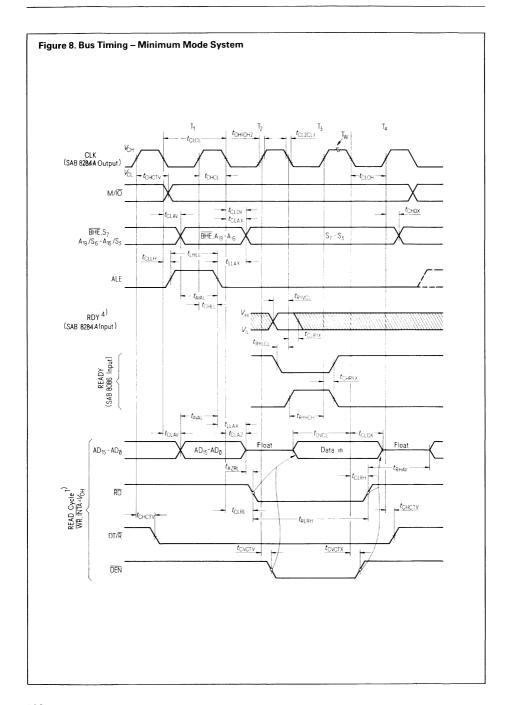
	8	Lir	nit Values	Units	Test
Symbol	Parameter	Min.	Max.	Units	Conditions
TCLML	Command Active Delay ¹)	10	35		
TCLMH	Command Inactive Delay ¹)	10			
TRYHSH	READY Active to Status Passive ²)	-	45		
TCHSV	Status Active Delay		,,,		
TCLSH	Status Inactive Delay		55		
TCLAV	Address Valid Delay	10	50		
TCLAX	Address Hold Time		-		$\begin{array}{c} C_L = 20-100 \text{ pF} \\ \text{for all SAB 8086} \\ \text{Outputs} \\ \text{(In addition to SAB 8086} \\ \text{self-load)} \end{array}$
TCLAZ	Address Float Delay		40		
TSVLH	Status Valid to ALE High ¹)			ns	
TSVMCH	Status Valid to MCE High ¹)				
TCLLH	CLK Low to ALE Valid ¹)	_	20		
TCLMCH	CLK Low to MCE High ¹)				
TCHLL	ALE Inactive Delay ¹)	4	15		
TCLDV	Data Valid Delay	10	50		
TCHDX	Data Hold Time		-		
TCVNV	Control Active Delay ¹)	5	45		
TCVNX	Control Inactive Delay ¹)	10	73		

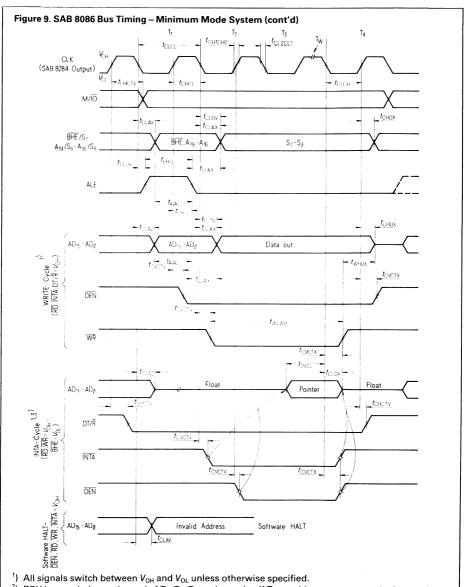
 $^{^{1})}$ Signal at SAB 8284A or SAB8288 shown for reference only. $^{2})$ Applies only to T_{2} and wait states.

Timing Responses SAB 8086-1 (continued) (Preliminary)

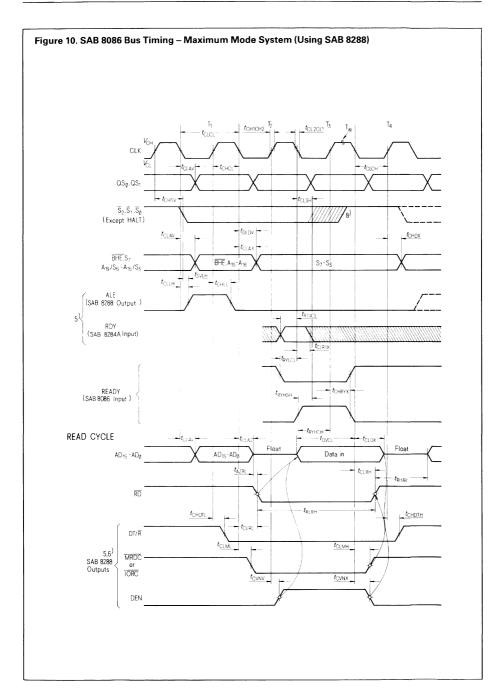
Symbol	Parameter	Limit Va	lues	Units	Test	
Symbol	rarameter	Min.	in. Max.		Conditions	
TAZRL	Address Float to READ Active	0	-			
TCLRL	RD Active Delay	10	70			
TCLRH	RD Inactive Delay		60			
TRHAV	RD Inactive to Next Address Active	TCLCL-35	-			
TCHDTL	Direction Control Active Delay ¹)		50		$C_L = 20 - 100 \text{ pF}$	
TCHDTH	Direction Control Inactive Delay ¹)		30	ns	for all SAB 8086 Outputs	
TCLGL	GT Active Delay	0	45		(In addition to SAB 8086	
TCLGH	GT Inactive Delay	7	43		self-load)	
TRLRH	RD Width	2TCLCL-40	-			
TOLOH	Output Rise Time		20		From 0.8 to 2.0V	
TOHOL	Output Fall Time		12		From 2.0 to 0.8V	

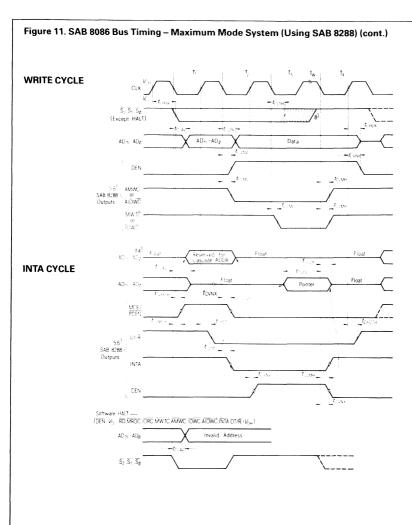
 $^{^{\}rm 1})$ Signal at SAB 8284A or SAB 8288 shown for reference only. $^{\rm 2})$ Applies only to T_3 and wait states.





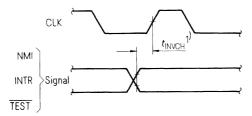
- 2) RDY is sampled near the end of T₂, T₃, T_w to determine if T_w machines states are to be inserted.
- 3) Two INTA cycles run back to back. The SAB 8086 local ADDR/DATA Bus is floating during both INTA cycles. Control signals shown for second INTA cycle.
- ⁴) Signals at SAB 8284A are shown for reference only.
- 5) All timing measurements are made at 1.5 V unless otherwise noted.





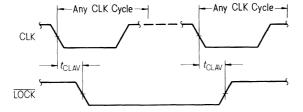
- All Signals switch between V_{OH} and V_{OL} unless otherwise specified.
- 2) RDY is sampled near the end of T₂, T₃, T_w to determine if T_w machines states are to be inserted.
- 3) Cascade address is valid between first and second INTA cycle.
- 4) Two INTA cycles run back-to-back. The SAB 8086 local ADDR/DATA Bus is floating during both INTA cycles. Control for pointer address is shown for second INTA cycle.
- 5) Signals at SAB 8284A or SAB 8288 are shown for reference only.
- The issuance of the SAB 8288 command and control signals (MRDC, MWTC, AMWC, IORC, IOWC, AIOWC, INTA and DEN) lags the active HIGH SAB 8288 DEN.
- 7) All timing measurements are made at 1.5 V unless otherwise noted.
- 8) Status inactive in state just prior to T₄.

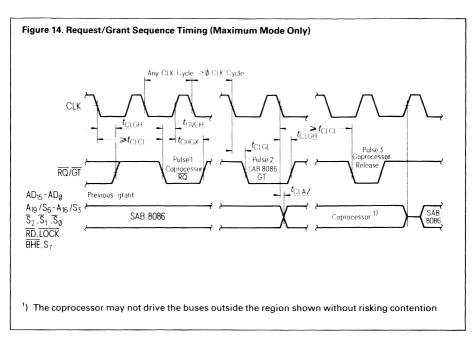


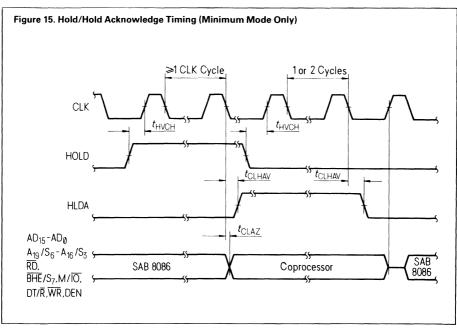


1) Setup requirements for asynchronous signals only to guarantee recognition at next CLK

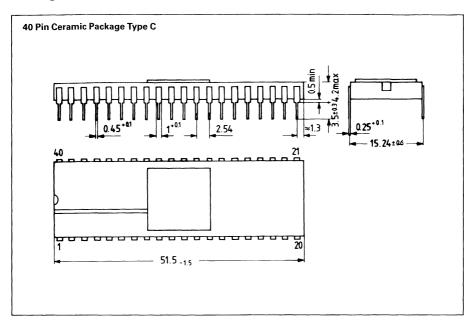


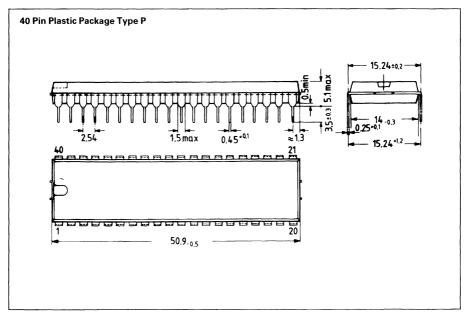






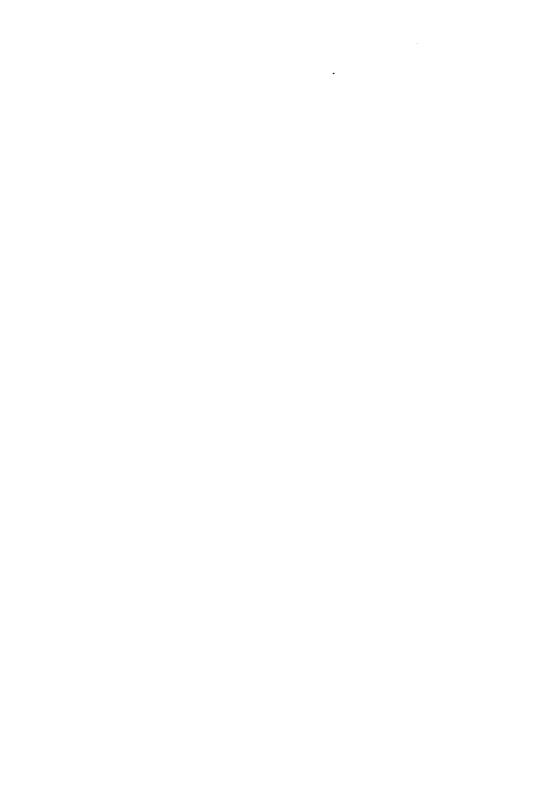
Package Outline





Ordering Information

	The state of the s	
Component	Description	Ordering code
SAB 8086-C	16 Bit Microprocessor – 5 MHz Ceramic	Q 67120-C 45
SAB 8086-2-C	16 Bit Microprocessor – 8 MHz Ceramic	Q 67120-C 60
SAB 8086-1-C	16 Bit Microprocessor – 10 MHz Ceramic	Q 67120-C 104
SAB 8086-P	16 Bit Microprocessor – 5 MHz Plastic	Q 67120-C 116
SAB 8086-2-P	16 Bit Microprocessor – 8 MHz Plastic	Q 67120-C 142
SAB 8086-1-P	16 Bit Microprocessor – 10 MHz Plastic	Q 67120-C 141



Preliminary

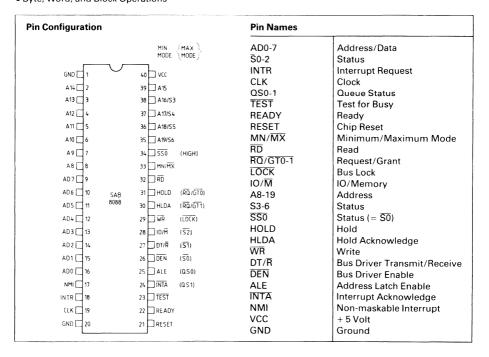
SAB 8088 8-Bit Microprocessor

SAB 8088 5 MHz

- 8 Bit Data Bus Interface
- 16 Bit Internal Architecture
- Direct Addressing Capability to 1 MByte of Memory
- Software Compatible with SAB 8086
- 14-Word by 16-Bit Register Set with Symetrical Operations
- Byte, Word, and Block Operations

SAB 8088-2 8 MHz

- 24 Operand Addressing Modes
- 8-Bit and 16-Bit Signed and Unsigned Arithmetic in Binary or Decimal, Including Multiply and Divide
- Two Clock Rates:5 MHz for SAB 80888 MHz for SAB 8088-2
- Compatible with Industry Standard 8088



SAB 8088 is a high-performance 8-bit microprocessor implemented in \pm 5 volts, advanced Siemens MYMOS technology, packaged in a 40-pin package. It is 100 percent compatible with the industry standard 8088. With features like string

handling, 16-bit arithmetic with multiply and divide it significantly increases system performance. It is highly suited for multiprocessor applications in various configurations.

^{*)} SAB 8088-1 (10 MHz) on request

Pin Definitions and Functions

The following pin function descriptions are for SAB 8088 systems in either minimum or maximum mode. The "local bus" in these descriptions is

the direct multiplexed bus interface connection to the SAB 8088 (without regard to additional bus buffers).

Symbol	Number	Input (I) Output (O)	Function					
AD7-AD0	9-16	1/0	ADDRESS DATA BUS: These lines constitute the time multiplexed memory I/O address (T1) and data (T2, T3, Tw, and T4) bus. These lines are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus "hold acknowledge".					
A15-A8	39, 2-8	0	ADDRESS BUS: These lines provide address bits 8 through 15 for the entire bus cycle (T1–T4). These lines do not have to be latched by ALE to remain valid. A15–A8 are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus "hold acknowledge".					
A17/S4, A16/S3 ficant a operati operati during interru				DRESS/STATUS: During T1, these are the four most signisant address lines for memory operations. During I/O perations, these lines are LOW. During memory and I/O perations, status information is available on these lines uring T2, T3, Tw and T4. S6 is always low. The status of the terrupt enable flag bit (S5) is updated at the beginning of ich clock cycle. S4 and S3 are encoded as shown.				
			S4	S3	Characteristics			
			0 0 1 1 1	0 1 0 1	Alternate Data Stack Code or None Data			
			being us	ed for da nes float	indicates which segment register is presently ita accessing. to 3-state OFF during local bus "hold			
RD	32	О	READ: Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the IO/M pin or S2. This signal is used to read devices which reside on the SAB 8088 local bus. RD is active LOW during T2, T3 and Tw of any read cycle, and is guaranteed to remain HIGH in T2 until the SAB 8088 local bus has floated. This signal floats to 3-state OFF in "hold acknowledge".					
READY	22	I	READY: is the acknowledgement from the addressed memory or I/O device that it will complete the data transfer. The RDY signal from memory or I/O is synchronized by the SAB 8284A/8284B clock generator to form READY. This signal is active HIGH. The SAB 8088 READY input is not synchronized. Correct operation is not guaranteed if the set up and hold times are not met.					
INTR	18	I						

Symbol	Number	Input (I) Output (O)	Function
TEST	23	I	TEST: input is examined by the "wait for test" instruction. If the TEST input is LOW, execution continues, otherwise the processor waits in an "idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.
NMI	17	į	NON-MASKABLE INTERRUPT: is an edge triggered input which causes a type 2 interrupt. A subroutine is vectored to via interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from a LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.
RESET	21	l	RESET: causes the processor to immediately terminate its present activity. The signal must be active HIGH for at least four clock cycles. It restarts execution, as described in the instruction set description, when RESET returns LOW. RESET is internally synchronized.
CLK	19	ı	CLOCK: provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.
VCC	40	_	POWER SUPPLY (+5V)
GND	1, 20	-	GROUND (OV)
MN/MX	33	I	MINIMUM/MAXIMUM: indicates what mode the processor is to operate in. The two modes are discussed in the following sections.

The following pin function descriptions are for the SAB 8088 minimum mode (i.e. $MN/\overline{MX} = VCC$). Only the pin functions which are unique to

minimum mode are described; all other pin functions are as described above.

IO/M	28	О	STATUS LINE: is an inverted maximum mode $\overline{S2}$. It is used to distinguish a memory access from an I/O access. IO/ \overline{M} becomes valid in the T4 preceding a bus cycle and remains valid until the final T4 of the cycle (I/O = HIGH, M = LOW). IO/ \overline{M} floats to 3-state OFF in local bus "hold acknowledge".
WR	29	0	WRITE: strobe indicates that the processor is performing a write memory or write I/O cycle depending on the state of the IO/M̄ signal. WR is active for T2, T3, and Tw of any write cycle. It is active LOW, and floats to 3-state OFF in local bus "hold acknowledge".
INTA	24	0	INTA: is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T2, T3, and Tw of each interrupt acknowledge cycle.

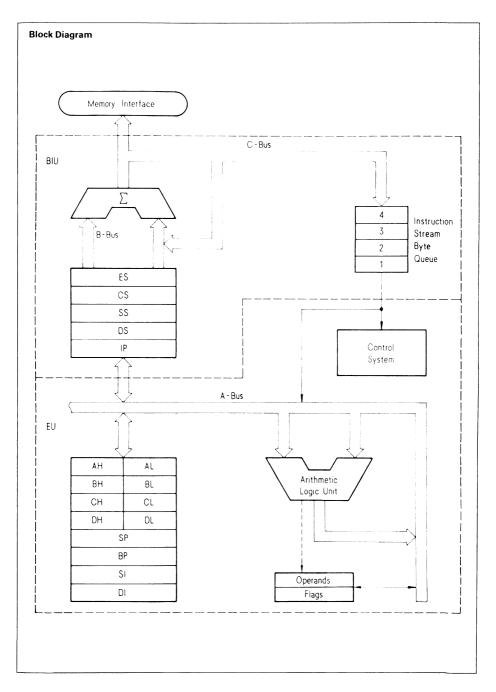
Symbol	Number	Input (I) Output (O)	Function				
ALE	25	0	ADDRESS LATCH ENABLE: is provided by the processor to latch the address into the SAB 8282 /8282A/8283/8283A address latch. It is a HIGH pulse active during clock low of T1 of any bus cycle. Note that ALE is never floated.				
DT/R	27	0	DATA TRANSMIT/RECEIVE: is needed in a minimum system that desires to use an SAB 8286/8286A/8287/8287A data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically, DT/\overline{R} is equivalent to $\overline{S1}$ in the maximum mode, and its timing is the same as for IO/M (T = HIGH, R = LOW). This signal floats to 3-state OFF in local "hold acknowledge".				
DEN	26	0	DATA ENABLE: is provided as an output enable for the SAB 8286/8286A/ 8287/8287A in a minimum system which uses the transceiver. DEN is active LOW during each memory and I/O access, and for INTA cycles. For a read or INTA cycle, it is active from the middle of T2 until the middle of T4, while for a write cycle, it is active from the beginning of T2 until the middle of T4. DEN floats to 3-state OFF during local bus "hold acknowledge".				
HOLD, HLDA	31, 30	I/O	HOLD: indicates that another master is requesting a local bus "hold". To be acknowledged, HOLD must be active HIGH. The processor receiving the "hold" request will issue HLDA (HIGH) as an acknowledgement, in the middle of a T4 or T1 clock cycle. Simultaneous with the issuance of HLDA the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor lowers HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. Hold is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the set up time.				
SSO	34	0	STATUS LINE: is logically equivalent to \overline{SO} in the maximum mode. The combination of \overline{SSO} , $\overline{IO/M}$ and $\overline{DT/R}$ allows the system to completely decode the current bus cycle status.				
			IO/M	DT/R	SSO	Characteristics	
			1 1 1 1 0 0 0	0 0 1 1 0 0	0 1 0 1 0 1 0	Interrupt Acknowledge Read I/O Port Write I/O Port Halt Code access Read memory Write memory Passive	

The following pin function descriptions are for the SAB 8088/8288 system in maximum mode (i.e. $MN/\overline{MX} = GND$). Only the pin functions which

are unique to maximum mode are described. All other pin functions are as described above.

Symbol	Number	Input (I) Output (O)	Functio	n					
\$2, \$1, \$0	28-26	28-26 O			STATUS: is active during clock high of T4, T1, and T2, and is returned to the passive state (1,1,1) during T3 or during Tw when READY is HIGH. This status is used by the SAB 8288/8288A bus controller to generate all memory and I/O access control signals. Any change by \$\frac{32}{51}\$, or \$\frac{50}{61}\$ during T4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T3 or Tw is used to indicate the end of a bus cycle. These signals float to 3-state OFF during "hold acknowledge". During the first clock cycle after RESET becomes active, these signals are active HIGH. After this first clock, they float to 3-state OFF.				
			<u>S2</u>	S1	<u>50</u>	Characteristics			
		0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0	Interrupt Acknowledge Read I/O Port Write I/O Port Halt Code access Read memory Write memory Passive				
RO/GTO RO/GT1	31 30	I/O I/O	to force the processor to release processor's current bus cycle. ERQ/GTO having higher priority to internal pull-up resistor so may request/grant sequence is as fol 1. A pulse of one CLK wide from indicates a local bus request (pulse 1). 2. During a T4 or T1 clock cycle, the SAB 8088 to the requesting that the SAB 8088 has allowed it will enter the "hold acknowl The CPU's bus interface unit in the local bus during "hold ack as for HOLD/HOLDA apply as			is as follows (See page 28): de from another local bus master equest ("hold") to the SAB 8088 (cycle, a pulse one clock wide from questing master (pulse 2), indicates allowed the local bus to float and that icknowledge" state at the next CLK. ise unit is disconnected logically from hold acknowledge". The same rules pply as for when the bus is released. from the requesting master indicates			
			to the SAB 8088 (pulse 3) that the "hold" request is about to end and that the SAB 8088 can reclaim the local bus at the next CLK. The CPU then enters T4. Each master-master exchange of the local bus is a sequence of three pulses. There must be one idle CLK cycle after each bus exchange. Pulses are active LOW.						

Symbol	Number	Input (I) Output (O)	Functi	Function				
			cycle,	it will rele	made while the CPU is performing a memory base the local bus during T4 of the cycle when all onditions are met:			
			2. Cur 3. Cur ackı	rent cycle rent cycle nowledge	urs on or before T2. e is not the low byte of a word. e is not the first acknowledge of an interrupt e sequence. ruction is not currently executing.			
			If the local bus is idle when the request is made the two possible events will follow:					
			Local bus will be released during the next clock. A memory cycle will start within 3 clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied.					
LOCK	29	0	LOCK: indicates that other system bus masters are not to gain control of the system bus while LOCK is active (LOW). The LOCK signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and floats to 3-state off in "hold acknowledge".					
QS1, QS0	24, 25	0	the int	ernal SA ueue stat	S: provide status to allow external tracking of B 8088 instruction queue. us is valid during the CLK cycle after which the n is performed.			
			QS1	QS0	Characteristics			
			0 0 1 1	0 1 0 1	No operation First Byte of opcode from queue Empty the queue Subsequent byte from queue			
_	34	0	Pin 34 is always high in the maximum mode.					



Functional Description

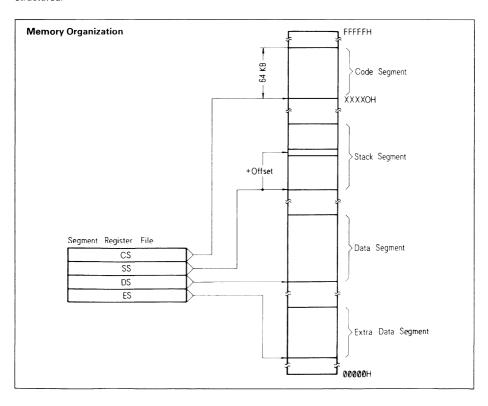
Memory Organization

The processor provides a 20-bit address to memory which locates the byte being referenced. The memory is organized as a linear array of up to 1 million bytes, addressed as 00000(H) to FFFFF(H). The memory is logically divided into code, data, extra data, and stack segments of up to 64 Kbytes each, with each segment falling on 16-byte boundaries.

All memory references are made relative to base addresses contained in high speed segment registers. The segment types were chosen based on the addressing needs of programs. The segment register to be selected is automatically chosen according to the rules of the following table. All information in one segment type share the same logical attributes (e.g. code or data). By structuring memory into relocatable areas of similar characteristics and by automatically selecting segment registers, programs are shorter, faster, and more structured.

Word (16-bit) operands can be located on even or odd address boundaries. For address and data operands, the least significant byte of the word is stored in the lower valued address location and the most significant byte in the next higher address location. The BIU will automatically execute two fetch or write cycles for 16-bit operands.

Certain locations in memory are reserved for specific CPU operations. Locations from addresses FFFF0H trough FFFFFH are reserved for operations including a jump to the initial system initialization routine. Following RESET, the CPU will always begin execution at location FFFF0H where the jump must be located. Locations 00000H through 003FFH are reserved for interrupt operations. Fourbyte pointers consisting of a 16-bit segment address and a 16-bit offset address direct program flow to one of the 256 possible interrupt service routines. The pointer elements are assumed to have been stored at their respective places in reserved memory prior to the occurrence of interrupts.



Minimum and Maximum Modes

The requirements for supporting minimum and maximum SAB 8088 systems are sufficiently different that they cannot be done efficiently with 40 uniquely defined pins. Consequently, the SAB 8088 is equipped with a strap pin (MN/MX) which defines the system configuration. The definition of a certain subset of the pins changes, dependent on the condition of the strap pin. When the MN/MX pin is strapped to GND, the SAB 8088 defines pins 24 through 31 and 34 in maximum mode. When the MN/MX pin is strapped to VCC, the SAB 8088 generates bus control signals itself on pins 24 through 31 and 34.

The minimum mode SAB 8088 can be used with either a multiplexed or demultiplexed bus. The multiplexed bus configuration is compatible with the SAB 8085A multiplexed bus peripherals (e.g. SAB 8155) and provides the user with a minimum chip count system. This architecture provides the 8088 processing power in a highly integrated form.

The demultiplexed mode requires one latch (for 64K addressability) or two latches (for a full megabyte of addressing). A third latch can be used for buffering if the address bus loading requires it. An SAB 8286/8286A or SAB 8287/8287A transceiver can also be used if data bus buffering is required. The SAB 8088 provides DEN and DT/R to control the transceiver, and ALE to latch the addresses. This configuration of the minimum mode provides the standard demultiplexed bus structure with heavy bus buffering and relaxed bus timing requirements.

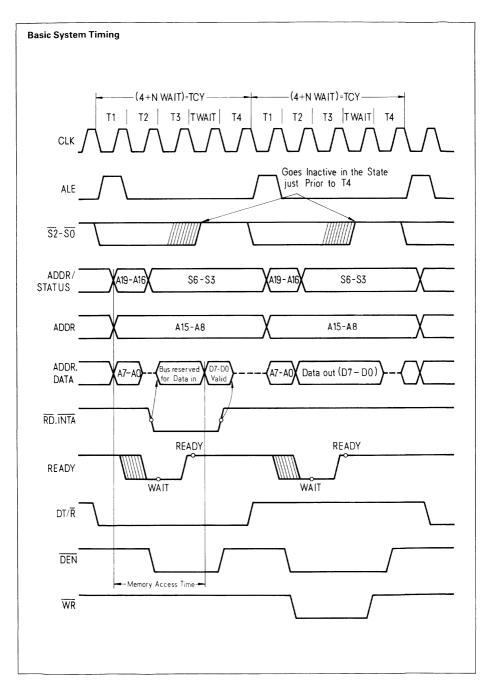
The maximum mode employs the SAB 8288/8288A bus controller. The SAB 8288/8288A decodes status lines $\overline{50}$, $\overline{51}$, and $\overline{52}$, and provides the system with all bus control signals. Moving the bus control to the SAB 8288/8288A provides better source and sink current capability to the control lines, and frees the SAB 8088 pins for extended large system features. Hardware lock, queue status, and two request/grant interfaces are provided by the SAB 8088 in maximum mode. These features allow co-processors in local bus and remote bus configurations.

Bus Operation

The SAB 8088 address/data bus is broken into three parts – the lower eight address/data bits (ADO–AD7), the midle eight address bits (A8–A15), and the upper four address bits (A16–A19). The address/data bits and the highest four address bits are time multiplexed. This technique provides the most efficient use of pins on the processor, permitting the use of a standard 40 lead package. The middle eight address bits are not multiplexed, i.e. they remain valid throughout each bus cycle. In addition, the bus can be demultiplexed at the processor with a single address latch if a standard, non-multiplexed bus is desired for the system.

Each processor bus cycle consists of at least four CLK cycles. These are referred to as T1, T2, T3 and T4. The address is emitted from the processor during T1 and data transfer occurs on the bus during T3 and T4. T2 is used primarily for changing the direction of the bus during read operations. In the event that a "NOT READY" indication is given by the addressed device, "wait" states (Tw) are inserted between T3 and T4. Each inserted "wait" state is of the same duration as a CLK cycle. Periods can occur between SAB 8088 driven bus cycles. These are referred to as "idle" states (Ti), or inactive CLK cycles. The processor uses these cycles for internal housekeeping.

During T1 of any bus cycle, the ALE (address latch enable) signal is emitted (by either the processor or the SAB 8288/8288A bus controller, depending on the MN/MX strap). At the trailing edge of this pulse, a valid address and certain status information for the cycle may be latched.



Status bits $\overline{S0}$, $\overline{S1}$, and $\overline{S2}$ are used by the bus controller, in maximum mode, to identify the type of bus transaction according to the following table:

	Š1	Ī0	Characteristics
0 (LOW) 0	0	0	Interrupt Acknowledge Read I/O
0	1	0	Write I/O
0	1	1	Halt
1 (HIGH)	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

Status bits S3 through S6 are multiplexed with highorder address bits and are therefore valid during T2 through T4. S3 and S4 indicate which segment register was used for this bus cycle in forming the address according to the following table:

S4	S3	Characteristics
0 (LOW)	0	Alternate Data (extra segment)
0 1 (HIGH)	1 0	Stack Code or None
1	1	Data

S5 is a reflection of the PSW interrupt enable bit. S6 is always equal to 0.

I/O Addressing

In the SAB 8088, I/O operations can address up to a maximum of 64 K I/O registers. The I/O address appears in the same format as the memory address on bus lines A15 – A0. The address lines A19 – A16 are zero in I/O operations. The variable I/O instructions, which use register DX as a pointer have full address capability, while the direct I/O instructions directly address one or two of the 256 I/O byte locations in page 0 of the I/O address space. I/O ports are addressed in the same manner as memory locations.

Designers familiar with the SAB 8085 or upgrading an SAB 8085 design should note that the SAB 8085 addresses I/O with an 8-bit address on both halves of the 16-bit address bus. The SAB 8088 uses a full 16-bit address on its lower 16 address lines.

System Components

Support Circuits

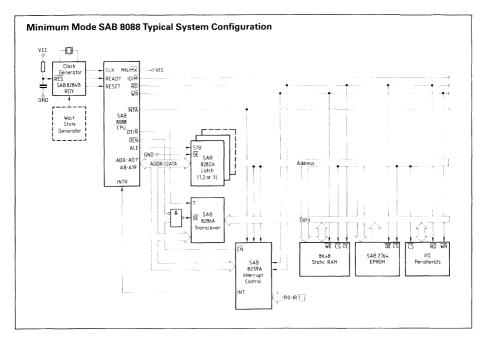
SAB 8282/8282A Octal Latch
SAB 8283/8283A Octal Latch (Inverting)
SAB 8284A/8284B Clock Generator and Driver
SAB 8286/8286A Octal Bus Transceiver
SAB 8287/8287A Octal Bus Transceiver (Inverting)
SAB 8288/8288A Bus Controller
SAB 8289
Rus Arbiter

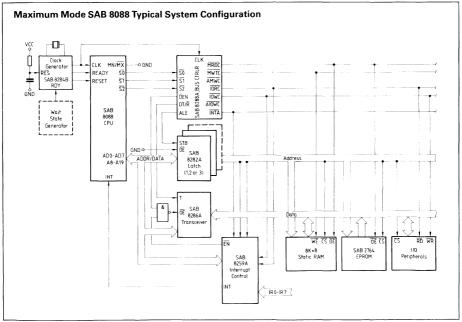
SAB 8289 Bus Arbiter SAB 8259A Programma

SAB 8259A Programmable Interrupt Controller

Typical Applications

The SAB 8088 is a general purpose 8-bit microprocessor which can be used for applications ranging from process control to data processing. On page 12 are shown typical system configurations for SAB 8088 famility components.





DATA TRANSFER MOV = Move	76543210	76543210 76543210 76543210 76543210	76543210	76543210	OUT = Output to:	76543210 76543210 76543210 76543210	43210 7654	43210 7	6543210 Instru
Register / memory to / from register	100010dw mod reg r/m	mod reg r/m			Fixed port	w1100111	port		ucti
Immediate to register/memory	1100011	1100011w mod000r/m	data	data if w=1	Variable port	W1110111			ion :
Immediate to register	1011w reg	data	data if w=1		XLAT = Translate byte to AL	111010111			Set
Memory to accumulator	1010000	addr-low	addr-high		LEA = Load EA to register	10001101 mod reg r/m	eg r/m		Sur
Accumulator to memory	1010001	addr-low	addr-high		LDS = Load pointer to DS	11000101 modregr/m	m/u ba		nma
Register/memory to segment register	10001110 mod0regr/m	mod 0 reg r/m			LES = Load pointer to ES	11000100 mod reg r/m	eg r/m		ary
Segment register to register/memory	10001100 mod0regr/m	mod 0 reg r/m			LAHF = Load AH with flags	10011111			
					SAMF = Store AH into flags	10011110			
PUSH = Push:					PUSHF = Push flags	10011100			
Register/memory	1111111 mod110r/m	mod 1 1 0 r/m			POPF = Pop flags	10011101			
Register	01010 reg								
Segment register	000 reg 110				ARITHMETIC ADD = Add:				
POP = Pop:					Reg./memory with register to either	000000dw mod reg r/m	eg r/m		
Register/memory	100C1111 mod000r/m	mod 0 0 0 r/m			Immediate to register/memory	100000sw mod000r/m		data da	data if s: w = 01
Register	01011 reg				Immediate to accumulator	0000010w	data data	data if w=1	
Segment register	000reg111				ADC = Add with carry:				
XCHG = Exchange:					Reg./memory with register to either	000100dw modregr/m	m/u Ba		
Register/memory with register	1000011w mod reg r/m	mod reg r/m			Immediate to register/memory	100000sw mod010r/m		data da	data if s:w=01
Register with accumulator	10010 reg				Immediate to accumulator	0001010w	data data	data if w=1	
IN = Input from:					INC = Increment:				
Fixed port	1110010w	port			Register/memory	1111111 mod000r/m	m/u 0 0 0		
Variable port	1110110w				Register	01000reg			
					AAA = ASCII adjust for add	11101110			
					DAA = Decimal adjust for add	00100111			

SUB = Subtract:	76543210 76543210 76543210 76543210	6543210	76543210	76543210	POGIC TOGIC	76543210	76543210 76543210 76543210 76543210	76543210	76543210
Reg./memory and register to either	001010dw mod reg r/m	nod reg r/m			NOT = Invert	1111011w	1111011w mod010r/m		
Immediate from register/memory	100000sw mod101r/m	nod 1 0 1 r/m	data	data if s:w=01	SHL/SAL = Shift logical/arithmetic left	110100vw mod100r/m	mod 1 0 0 r/m		
Immediate from accumulator	0010110w	data	data if w=1		SHR = Shift logical right	110100vw	110100vw mod101r/m		
					SAR = Shift arithmetic right	110100vw	110100vw mod111r/m		
SBB = Subtract with borrow					ROL = Rotate left	1101,00vw	1101,00 v w mod 0 0 0 r/m		
Reg./memory and register to either	000110dw mod reg r/m	m/u gar por			ROR = Rotate right	110100 v w	110100vw mod001r/m		
Immediate from register/memory	100000sw mod011r/m	nod 0 1 1 r/m	data	data if s:w=01	RCL = Rotate through carry flag left	110100 v w	110100vw mod010r/m		
Immediate from accumulator	0001110w	data	data if w=1		RCR = Rotate through carry right	110100vw	110100vw mod011r/m		
DEC = Decrement:	76543210 76543210 76543210 76543210	6543210	76543210	76543210					
Register/memory	1111111w mod001r/m	nod 0 0 1 r/m			AND = And:				
Register	01001reg				neg: memory and register to either	100000 modregrm	100000 modregr/m	1	1 1 1 1 1 1
NEG = Change sign	1111011w mod011r/m	nod 0 1 1 r/m			Immediate to accumulator	30000	mico o o o o o	udid data if w. 1	Odid II W
CMP = Compare:					TEST = And function to flags no result:				
Register/memory and register	001110dw modregr/m	nod reg r/m			Begister/memory and register	1000010w mod rear/m	mod reg r/m		
Immediate with register/memory	100000sw mod111r/m	nod 1 1 1 r/m	data	data if s:w=01	Immediate data and register/memory	w11111	1111011w mod000r/m	data	data if w = 1
Immediate with accumulator	0011110w	data	data if w=1		Immediate data and actiminator	10101	data	t = w fi etch	
AAS = ASCII adjust for subtract	00111111								
DAS = Decimal adjust for subtract	00101111				OR = Or:				
MUL = Multiply (unsigned)	1111011w mod100r/m	nod 100 r/m			Reg/memory and register to either	000010dw modregr/m	mod reg r/m		
IMUL = Integer multiply (signed)	1111011w mod101r/m	nod 1 0 1 r/m			Immediate to register/memory	1000000w	1000000w mod001r/m	data	data if w = 1
AAM = ASCII adjust for multiply	11010100 00001010	0001010			Immediate to accumulator	0000110w	data	data if w = 1	
DIV = Divide (unsigned)	1111011w mod110r/m	nod 1 1 0 r/m							
IDIV = Integer divide (signed)	1111011w mod1111r/m	nod 1 1 1 r/m			XOR = Exclusive or:				
AAD = ASCII adjust for divide	11010101 00001010	0001010			Reg./memory and register to either	001100dw modregr/m	mod reg r/m		
CBW = Convert byte to word	10011000				Immediate to register/memory	1000000w	1000000w mod110r/m	data	data if w = 1
CWD = Convert word to double word	10011001				Immediate to accumulator	0011010w	data	data if w = 1	

w disp-high ow offset-high fr/m seg-high w disp-high w seg-high ow offset-high fr/m seg-high fr/m se	RET = Return from CALL: 76543210 76543210 76543210	Within segment	Within seg. adding immed to SP 11000010 data-low data-high	Intersegment	Intersegment adding immediable to SP	JE/JZ = Jump on equal/zero 01110100 disp	JL/JNGE = Jump on less/not greater 0 1 1 1 1 1 0 0 disp	JLE/JNG = Jump on less or equal/not 01111110 disp	JB/JNAE = Jump on below/not above 011110010 disp	JBE/JNA = Jump on below or equal/	JP/JPE = Jump on parity/parity even	JO = Jump on overflow disp	JS = Jump on sign disp	JNE/JNZ = Jump on not equal/not zero 0 1 1 1 0 1 0 1 disp	JNL/JGE = Jump on not less/greater 01111101 disp	JNLE/JG = Jump on not less or equal/ greater disp	JNB/JAE = Jump on not below/above 01110011 disp	JNBE/JA = Jump on not below or 01110111 disp	JNP/JPO = Jump on not par/par odd 01111011 disp	JNO = Jump on not overflow (01110001 disp	JNS = Jump on not sign	LOOP = Loop CX times 11100010 disp	LOOPZ/LOOPE = Loop while zero/equal	LOOPNZ/LOOPNE = Loop while not removed the company of the company	JCXZ = Jump on CX zero
	7654,3210 76543210 76543210									disp-high disp-high	mod 0 1 0 r/m	offset-low offset-high	seg-low seg-high	mod 0 1 1 r/m			disp-high disp-high	disp	mod 100 r/m	offset-low offset-high	seg-low seg-high	mod 1 0 1 r/m			

JMP = Unconditional Jump:

Indirect intersegment

Direct within segment

Direct within segment short

Indirect within segment

Direct intersegment

Indirect intersegment

LODS = Load byte/word to AL/AX STOS = Store byte/word from AL/A

Indirect within segment

Direct intersegment

CONTROL TRANSFER
CALL = Call:
Direct within segment

CMPS = Compare byte/word

SCAS = Scan byte/word

MOVS = Move byte/word

REP = Repeat

STRING MANIPULATION

NT = Interrupt	76543210 76543210	Footnotes:	
Type specified	11001101 type	AL = 8-bit accumulator $AX = 16$ -bit accumulator	if $s, w = 01$ then 16-bits of immediate data from the operand
Туре 3	11001100	CX = Count register DS = Data segment	it s.w = 11 then an immediate data byte is sign extended to form the 16-bit operand
NTO = Interrupt on overflow	11001110	ES = Extra segment $Above$ /below refers to unsigned value.	<pre>if v = Uthen count = 1;If v = Ithen count in (CL) v = dou't care</pre>
RET = Interrupt return	111001111	Greater = more positive; Less = less positive (more negative) signed values	z sueed for string primitives for comparsion with ZF FLAG
PROCESSOR CONTROL		if d = 1 then "to" reg; if d = 0 then "from" reg if w = 1 then word instruction; if w = 0 then byte instruction	SEGMENT OVERRIDE PREFIX 001reg110
CLC = Clear carry	11111000		
CMC = Complement carry	11110101	if mod = 11 then r/m is treated as a REG field if mod = 00 then DISP = 0*, disp-low and disp-high	REG is assigned according to the following table
STC = Set Carry	111111001	are absent if mod = 01 then DISP = disp-low sign-extended to	16-Bit (w=1) 8-Bit (w=0) Segment
CLD = Clear direction	11111100	16-bits, disp high is absent if $mod = 10$ then DISP = disp-high; disp low	001 CL
STD = Set direction	11111101	if $r/m = 000$ then EA = (BX) + (SI) + DISP if $r/m = 001$ then EA = (BX) + (DI) + DISP	011 BL
CLI = Clear interrupt	11111010	if $r/m = 010$ then EA = (BP) + (SI) + DISP if $r/m = 011$ then EA = (BP) + (DI) + DISP	101 BP 101 CH
STI = Set interrupt	11111011	if $r/m = 100$ then EA = (SI) + DISP if $r/m = 101$ then EA = (DI) + DISP	
HLT = Halt	11110100	if r/m = 110 then EA = (BP) + DISP* if r/m = 111 then EA = (BX) + DISP	Instruction which reference the flag register file as a 16-bit object use the symbol FLAGS to
WAIT = Wait	10011011	DISP follows 2nd byte of instruction (before data if required)	represent the file:
ESC = Escape (to external device)	11011xxx modxxxr/m	*except if mod = 00 and r/m = 110 then EA = disp-high-disp-low.	FLAGS = X:X:X:(OF):(DF):(IF):(TF):(SF):(ZF): X:(AF):X:(FF):X:(CF)
LOCK = Bus lock prefix	111110000		

Absolute Maximum Ratings *)

D.C. Characteristics

SAB 8088: TA = 0 to 70° C, $VCC = 5 \text{ V} \pm 10\%$ SAB 8088-2: TA = 0 to 70° C, $VCC = 5 \text{ V} \pm 5\%$

		Limi	t Values		
Symbol	Parameter	Min.	Max.	Unit	Test Conditions
VIL	Input Low Voltage	-0.5	+0.8		
VIH	Input High Voltage	2.0	VCC+0.5	V	
<i>V</i> OL	Output Low Voltage	_	0.45		IOL = 2.0 mA
VОН	Output High Voltage	2.4	_		/OH = -400 μA
ICC	Power Supply Current SAB 8088 SAB 8088-2		340 350	mA	All outputs open TA = 25°C
/LI	Input Leakage Current		+ 10	μА	$OV \le VIN \le VCC$
/LO	Output Leakage Current		1.10	μΑ	0.45 V ≤ <i>V</i> OUT ≤ <i>V</i> CC
VCL	Clock Input Low Voltage	-0.5	+0.6	v	
<i>V</i> CH	Clock Input High Voltage	3.9	VCC+1.0	*	
CIN	Capacitance of Input Buffer (All input except AD0 – AD7, RQ/GT)	_	15	pF	fc = 1 MHz
CIO	Capacitance of I/O Buffer (ADØ – AD7, RQ/GT)				

^{*)} Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

A.C. Characteristics

SAB 8088: TA = 0 to 70° C, $VCC = 5 V \pm 10\%$ SAB 8088-2: TA = 0 to 70° C, $VCC = 5 V \pm 5\%$

Minimum Complexity System Timing Requirements

			Lim	it Values			
Symbol	Parameter	SAB 808	8	SAB 80	88-2	Unit	Test Condition
		Min.	Max.	Min.	Max.		
TCLCL	CLK Cycle Period	200	500	125	500		
TCLCH	CLK Low Time	118		68			-
TCHCL	CLK High Time	69		44			
TCH1CH2	CLK Rise Time		10		10		From 1.0 to 3.5V
TCL2CL1	CLK Fall Time						From 3.5 to 1.0V
TDVCL	Data in Setup Time	30		20			
TCLDX	Data in Hold Time	10		10		ns	
TR1VCL	RDY Setup Time into SAB 8284A/8284B 1) 2)	35		35			
TCLR1X	RDY Hold Time into SAB 8284A/8284B 1) 2)	0	_	0	-		_
TRYHCH	READY Setup Time into SAB 8088	118		68			
TCHRYX	READY Hold Time into SAB 8088	30		20			
TRYLCL	READY Inactive to CLK 3)	-8		-8			
THVCH	HOLD Setup Time	35		20			
TINVCH	INTR, NMI, TEST Setup Time ²)	30		15			
TILIH	Input Rise Time (Except CLK)		20		20		From 0.8 to 2.0 V
TIHIL	Input Fall Time (Except CLK)		12		12		From 2.0 to 0.8V

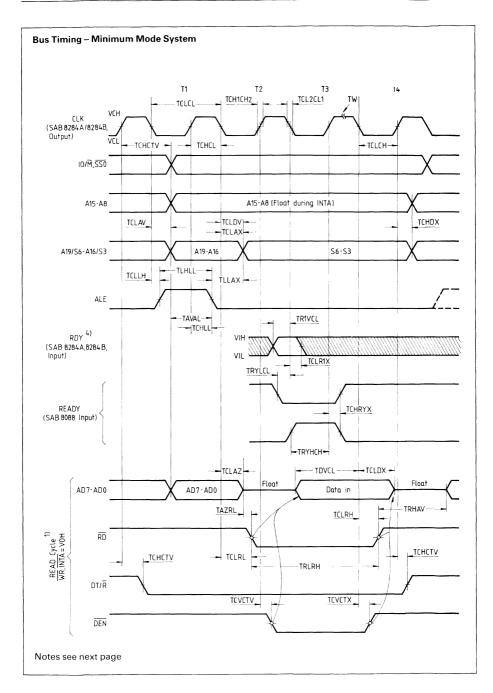
 $^{^{\}rm 1})$ Signal at SAB 8284A/8284B shown for reference only.

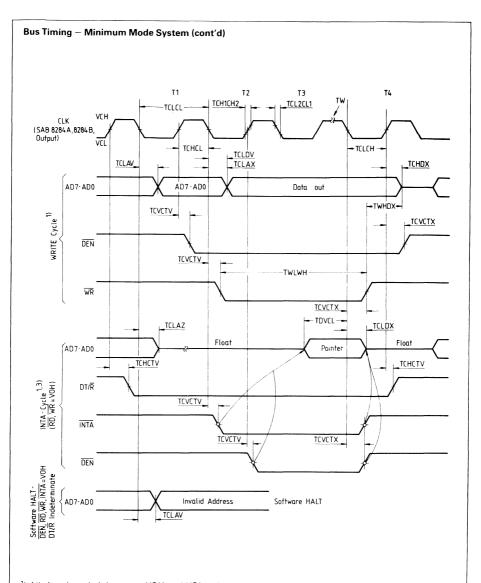
²⁾ Setup requirement for asynchronous signal only to guarantee recognition at next CLK.

³) Applies only to T2 state (8 ns into T3).

Timing Responses

			Limit	Values			
Symbol	Parameter	SAB 8088		SAB 8088-2		Unit	Test Condition
		Min.	Max.	Min.	Max.	1	
TCLAV	Address Valid Delay	10	110	10	60		
TCLAX	Address Hold Time	10	_		-		
TCLAZ	Address Float Delay	TCLAX	80	TCLAX	50		
TLHLL	ALE Width	TCLCH-20	-	TCLCH-10	-		
TCLLH	ALE Active Delay		80		50		
TCHLL	ALE Inactive Delay		85		55		
TLLAX	Address Hold Time to ALE Inactive	TCHCL-10	-	TCHCL-10	-		
TCLDV	Data Valid Delay	10	110	10	60		$C_L = 20 - 100 \text{ pF}$
TCHDX	Data Hold Time	10				ns	for all SAB 8088 Outputs in
TWHDX	Data Hold Time After WR	TCLCH-30	1	TCLCH-30	1	115	addition to the internal loads
TCVCTV	Control Active Delay 1				70		
TCHCTV	Control Active Delay 2	10	110	10	60	1	
TCVCTX	Control Inactive Delay				70		
TAZRL	Address Float to READ Active	0	-	0	-		
TCLRL	RD Active Delay	10	165	10	100		
TCLRH	RD Inactive Delay	10	150		80		
TRHAV	RD Inactive to Next Address Active	TCLCL-45	-	TCLCL-40	-		
TCLHAV	HLDA Valid Delay	10	160	10	100		
TRLRH	RD Width	2TCLCL-75		2TCLCL-50			
TWLWH	WR Width	2TCLCL-60]_	2TCLCL-40	-		
TAVAL	Address Valid to ALE Low	TCLCH-60		TCLCH-40			
тогон	Output Rise Time	_	20		20		From 0.8 to 2.0 V
TOHOL	Output Fall Time		12		12		From 2.0 to 0.8V





¹⁾ All signals switch between VOH and VOL unless otherwise specified.

²⁾ RDY is sampled near the end of T2, T3, Tw to determine if Tw machines states are to be inserted.

³) Two INTA cycles run back to back. The SAB 8088 local ADDR/DATA Bus is floating during both INTA cycles. Control signals shown for second INTA cycle.

⁴) Signals at SAB 8284A/8284B are shown for reference only.

⁵) All timing measurements are made at 1.5V unless otherwise noted.

SAB 8088

Max Mode System (Using SAB 8288/8288A Bus Controller) Timing Requirements

			Lim	nit Values			
Symbol	Parameter	SAB 8088	3	SAB 808	8-2	Unit	Test Condition
		Min.	Max.	Min.	Max.		
TCLCL	CLK Cycle Period	200	500	125	500		
TCLCH	CLK Low Time	118		68			-
TCHCL	CLK High Time	69		44			
TCH1CH2	CLK Rise Time		10		10		From 1.0 to 3.5V
TCL2CL1	CLK Fall Time						From 3.5 to 1.0 V
TDVCL	Data In Setup Time	30		20			
TCLDX	Data In Hold Time	10		10		ns	
TR1VCL	RDY Setup Time into SAB 8284A/8284B 1) 2)	35		35			
TCLR1X	RDY Hold Time into SAB 8284A/8284B 1) 2)	0	_	0	_		_
TRYHCH	READY Setup Time into SAB 8088	118		68			
TCHRYX	READY Hold Time into SAB 8088	30		20			
TRYLCL	READY Inactive to CLK 3)	-8		-8			
TINVCH	Setup Time for Recognition (INTR, NMI, TEST) 2)	30		15			
TGVCH	RQ/GT Setup Time						
TCHGX	RQ Hold Time into SAB 8088	40		30			
TILIH	Input Rise Time (Except CLK)		20		20		From 0.8 to 2.0V
TIHIL	Input Fall Time (Except CLK)	_	12		12		From 2.0 to 0.8V

 $^{^{\}rm 1})$ Signal at SAB 8284A/8284B or SAB 8288/8288A shown for reference only.

²⁾ Setup requirement for asynchronous signal only to guarantee recognition at next CLK.

³) Applies only to T2 state (8 ns into T3).

Timing Responses

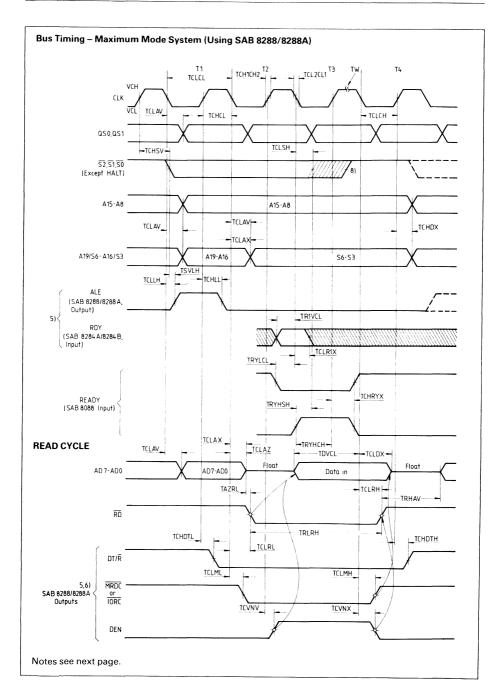
			Limit	Values			
Symbol	Parameter	SAB 8088		SAB 8088-2		Unit	Test Condition
		Min.	Max.	Min.	Max.		
TCLML	Command Active Delay 1)	10	35	10	35		
TCLMH	Command Inactive Delay ¹)	10	33	10			
TRYHSH	READY Active to Status Passive 2)	_	110	_	65		
TCHSV	Status Active Delay				60		
TCLSH	Status Inactive Delay	10	130	10	70		
TCLAV	Address Valid Delay	10	110		60	1	CL 20 100 F
TCLAX	Address Hold Time		_		-	1	CL = 20-100 pF for all SAB 8088
TCLAZ	Address Float Delay	TCLAX	80	TCLAX	50	ns	Outputs in addition to the
TSVLH	Status Valid to ALE High 1)					1	internal loads
TSVMCH	Status Valid to MCE High ¹)	_	20	_	20		
TCLLH	CLK Low to ALE Valid 1)						
TCLMCH	CLK Low to MCE High 1)					1	
TCHLL	ALE Inactive Delay 1)	4	15	4	15	1	
TCLDV	Data Valid Delay	10	110	10	60	1	
TCHDX	Data Hold Time	10	_	10	_		
TCVNV	Control Active Delay 1)	5	45	5	45	1	
TCVNX	Control Inactive Delay 1)	10] •3	10	1 +3		

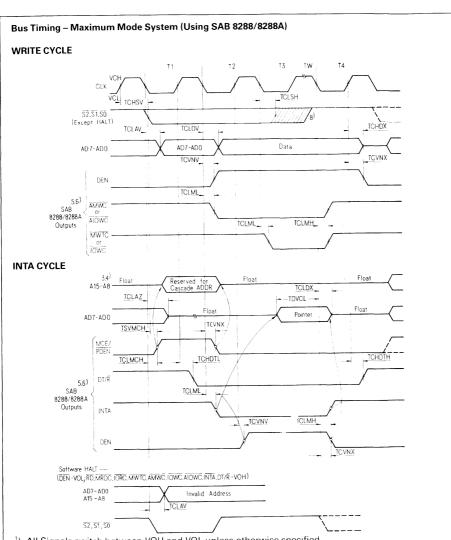
 $^{^1)}$ Signal at SAB 8284A/8284B or SAB 8288/8288A shown for reference only. $^2)$ Applies only to T2 state (8 ns into T3).

SAB 8088

			Limit	Values			
Symbol	Parameter	SAB 8088		SAB 8088-2		Unit	Test Condition
		Min.	Max.	Min.	Max.]	
TAZRL	Address Float to READ Active	0	-	0	-		
TCLRL	RD Active Delay	10	165	10	100		
TCLRH	RD Inactive Delay	7 10	150		80]	
TRHAV	RD Inactive to Next Address Active	TCLCL-45	-	TCLCL-40	-		CL = 20-100 pF for all SAB 8088
TCHDTL	Direction Control Active Delay 1)		50		50		Outputs in addition to the
TCHDTH	Direction Control Inactive Delay 1)	_	30	_	30		internal loads
TCLGL	GT Active Delay]	85		50		
TCLGH	GT Inactive Delay		03		30	ļ	
TRLRH	RD Width	2TCLCL-75	-	2TCLCL-50	-]	
TOLOH	Output Rise Time		20		20	1	From 0.8 to 2.0V
TOHOL	Output Fall Time]_	12		12		From 2.0 to 0.8V

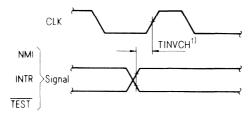
¹⁾ Signal at SAB 8284A/8284B or SAB 8288/8288A shown for reference only.





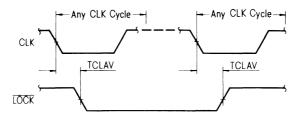
- 1) All Signals switch between VOH and VOL unless otherwise specified.
- 2) RDY is sampled near the end of T2, T3, Tw to determine if Tw machines states are to be inserted.
- 3) Cascade address is valid between first and second INTA cycle.
- 4) Two INTA cycles run back-to-back. The SAB 8088 local ADDR/DATA Bus is floating during both INTA cycles. Control for pointer address is shown for second INTA cycle.
- 5) Signals at SAB 8284A/8284B or SAB 8288/8288A are shown for reference only.
- 6) The issuance of the SAB 8288/8288A command and control signals (MRDC, MWTC, AMWC, IORC, IOWC, AIOWC, INTA and DEN) lags the active HIGH SAB 8288/8288A DEN.
- 7) All timing measurements are made at 1.5 V unless otherwise noted.
- 8) Status inactive in state just prior to T4.

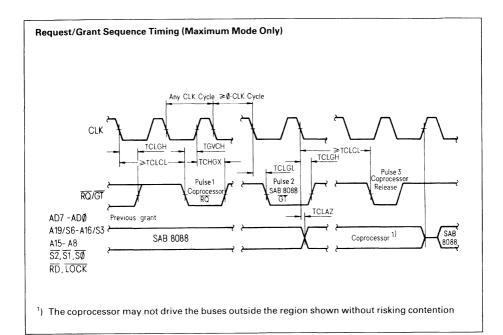
Asynchronous Signal Recognition

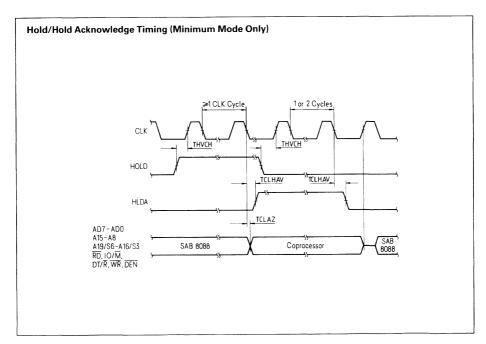


1) Setup requirements for asynchronous signals only to guarantee recognition at next CLK

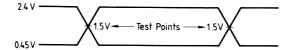
Bus Lock Signal Timing (Maximum Mode Only)





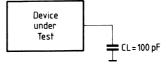


Input/Output Waveforms for A.C.-Tests



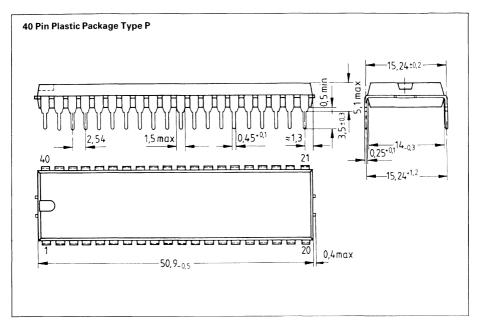
A.C. Testing: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". The clock is driven at 4.3V and 0.25V. Timing measurements are made at 1.5V for both a logic "1" and "0".

Load Circuit for A.C.-Tests



CL includes Jig Capacitance

Package Outline



Ordering Information

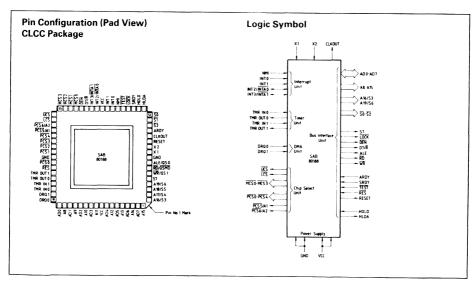
Туре	Description	Ordering code
SAB 8088-P	8-Bit Microprocessor – 5 MHz Plastic	Q 67120-C 106
SAB 8088-2-P	8-Bit Microprocessor – 8 MHz Plastic	Q 67120-C 213

Advance Information

SAB 80186 High-Integration 16-Bit Microprocessor

- Integrated feature set
 - enhanced SAB 8086-2 CPU
- clock generator
- 2 independent high-speed DMA channels
- programmable interrupt controller
- 3 programmable 16-bit timers
- programmable memory and peripheral chip-select logic
- programmable wait state generator
- local bus controller
- High-performance 8 MHz processor
 - twice the performance of the standard SAB 8086
 - 4 Mbyte/s bus bandwidth interface

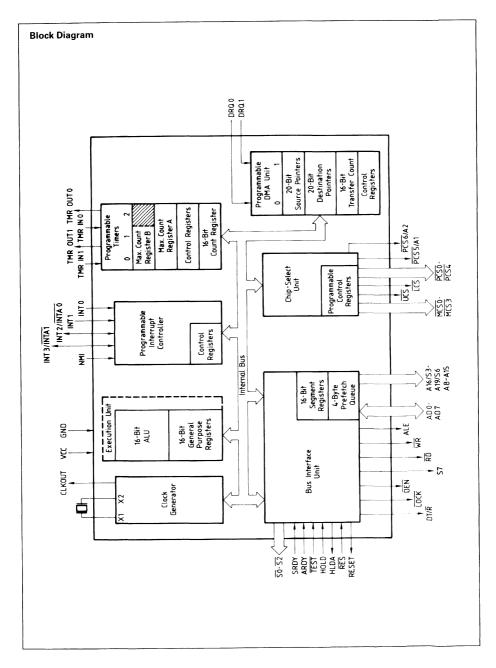
- Direct addressing capability to 1 Mbyte of memory
- Completely object-code compatible with all existing SAB 8086/8088 software
 - 10 new instruction types
- Optional numerical processor extension
- Compatible with the bus support components SAB 8282A/8283A/8286A/8287A and SAB 8288A/8289
- Compatible with industry standard 80186 processor



The SAB 80186 is a highly integrated 16-bit microprocessor implemented in +5 V advanced Siemens MYMOS technology, it effectively combines 15 to 20 of the most common SAB 8086 systems components on one chip. The SAB 80186 provides twice the throughput of the standard

5 MHz SAB 8086. The SAB 80186 is upward-compatible with SAB 8086 and SAB 8088 software, and adds 10 new instruction types to the existing set. The SAB 80186 comes in a 68-pin ceramic package and requires single +5 V power supply.

5.85



Advance Information

SAB 80188 High-Integration 8-Bit Microprocessor

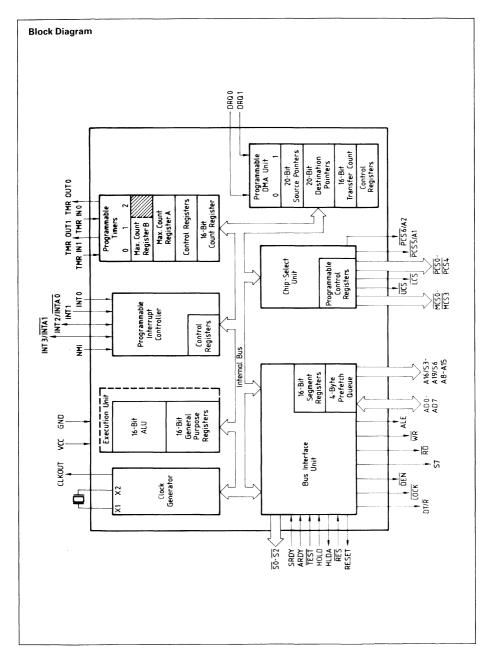
- Integrated feature set
 - enhanced SAB 8088-2 CPU
 - clock generator
 - 2 independent, high-speed DMA channels
 - programmable interrupt controller
 - 3 programmable 16-bit timers
 - programmable memory and peripheral chip-select logic
 - programmable wait state generator
 - local bus controller
- High-performance 8 MHz processor
 - 2 times the performance of the standard SAB 8088
 - 2 Mbyte/s bus bandwidth interface

- Direct addressing capability to 1 Mbyte of memory
- Completely object-code compatible with all existing SAB 8086/8088 software
 - 10 new instruction types
- Optional numeric processor extension
- Compatible with the bus support components SAB 8282A/8283A/8286A/8287A and SAB 8288A/8289
- Compatible with industry standard 80188 processor

The SAB 80188 is a highly integrated 8-bit microprocessor implemented in +5 V, advanced Siemens MYMOS technology. It effectively combines 15 to 20 of the most common SAB 8088 system components on one chip. The SAB 80188 provides twice the throughput of the standard

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5.85



Preliminary

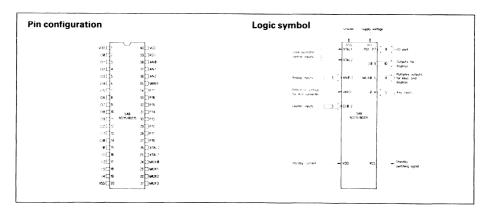
SAB 80215 SLE 43215 8-Bit Single-Chip Microcontroller

SAB 80215 with mask-programmable ROM SAB 80315 with external EPROM (piggyback version)

SLE 43215 as SAB 80215 with more closely specified electrical parameters

- 8-bit CPU
- 63 instructions
- 4 counters (4, 8, 8, 12 bits), two counters (8 and 12 bits) also as timers
- clock with American or European display
 - stop watch
 - alarm signal

- 5 V supply voltage
- 2K×8 ROM; 128×8 RAM; 30 I/O pins
- 8-bit A/D converter with 3 analog inputs
- interfaces directly to keys and 7-segment displays
- brightness control
- instruction cycle time 10μs; 1 or 2 cycles each instruction
- standby current supply for RAM, clock, stop watch, and alarm function

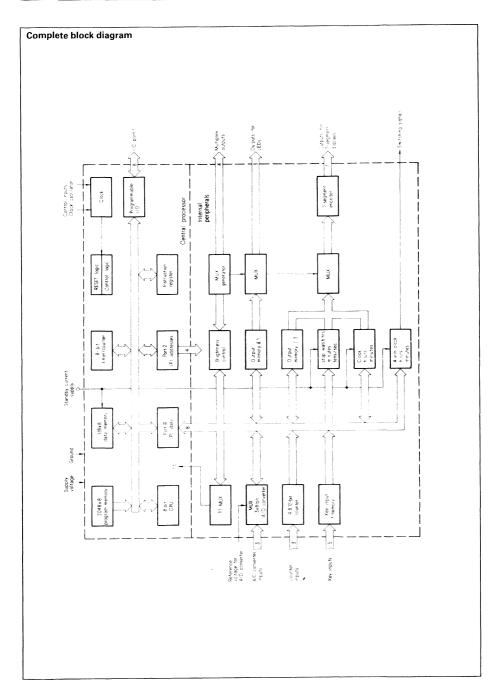


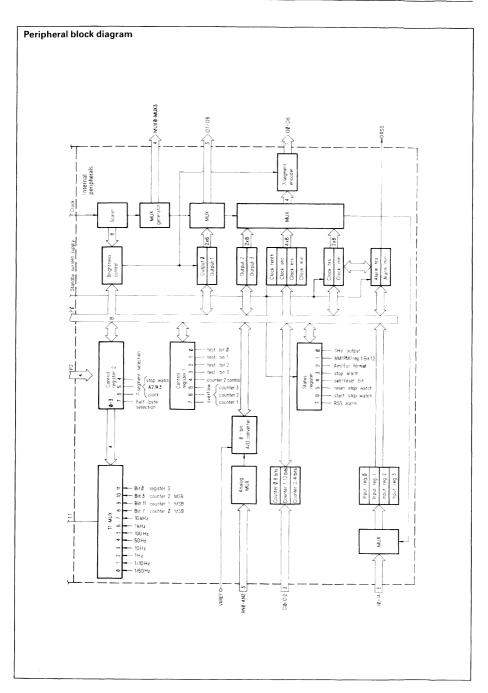
The SAB 80215 contains a complete standard 8-bit microcomputer and powerful peripheral circuits on the same chip. The core of the device equals the SAB 8021 but with the program memory increased in size to 2048×8 bits and the data memory to 128×8 bits. The peripheral components comprise a quasi-bidirectional 8-bit input/output port, an 8-bit and 12-bit timer/counter and an additional 4-bit and 8-bit counter, an 8-bit analog/digital converter with 3 multiplexed inputs, a clock that can be programmed for American or European notation.

In addition, 20 keys, four 7-segment displays, and further LEDs can be connected directly. The brightness can be controlled. The operation of the keys. LEDs, and 7-segment displays is controlled by an integrated multiplexer. In standby mode, the contents of the RAM is retained, the clock and alarm functions continue to run, and the switching signal of the alarm re-enables the full supply voltage. For more exacting applications, this microcomputer is available with more closely specified electrical parameters under type designations SLE 43215 and SLE 43315.

1 Pin Description

Description (Symbol)	Pin number	Input (I) Output (O)	Function
0Ø to 09	2 to 11	0	Outputs for LED/vaccum fluorescent displays 00 to 06 deliver the decoded 7-segment information. 07 to 09 controls three columns x 4 LEDs/VFDs. Together with MUX 0 to 3 outputs, 4 digits and 12 LEDs are controlled. The numerical information may come from the clock, the stop watch, or two 8-bit display registers. Brightness is controlled by pulse width modulation.
CIØ CI1 CI2	14 13 12	I	8, 12, 4-bit counter The counting frequency is from Ø to 100 kHz. The 12-bit counter can also be programmed as a timer.
10 11 12 13	15 16 17 18 19	I	Key inputs Together with outputs MUX Ø to 3, a matrix with 20 keys can be constructed.
MUX Ø MUX 1 MUX 2 MUX 3	24 23 22 21	0	Multiplex outputs for displays and keys These outputs serve to operate four 7-segment displays, 12 additional LEDs, and a matrix of 20 keys.
XTAL 1 XTAL 2	25 26	0	Clock oscillator control inputs At these pins, a frequency-determining crystal or an external clock (XTAL 1) is connected. Frequency 3 MHz.
P 10 to P 17	27 to 34	1/0	Quasi-bidirectional 8-bit input/output port Data can be written to or read from this port.
VAREF	35	1	Reference voltage for A/D converter The reference voltage can be between 1 V and 5 V.
AN 0 AN 1 AN 2	38 37 36	I	A/D converter inputs (multiplexed) The converter (successive approximation) has 8-bit resolution, a max. input voltage of 5 V, conversion time of 24 μ s, and sampling time of 5 μ s.
RSS	39	0	Switching signal output for the standby mode This output is controlled by the alarm circuit and the status register. It can also be used to switch on the supply voltage.
VCC	40	-	Supply voltage (+ 5 V)
VDD	1	-	Standby current supply (+ 5 V) This input supplies in standby state the RAM, clock, stop watch and alarm circuit. The current consumption is very low.
VSS	20	_	Ground (0 V)





2 Functional Description

Basic concept of central processing unit and internal peripheral circuits

As shown in the block diagram, the SAB 80215 consists of a CPU, program and data memories, a directly allocated 8-bit timer/counter and quasi-bidirectional 8-bit input/output port.

The access to the remaining peripheral components is achieved by means of an internal peripheral interface. When the supply voltage is switched on, a RESET pulse is automatically generated.

This sets the SAB 80215 in a start-up state.

An external RESET connection is, therefore,

The internal peripheral components accessible via the internal peripheral interface are:

- 8-bit analog/digital converter with 3 multiplexed inputs
- 4, 8, and 12-bit counters the 12-bit counter can also be used as timer
- clock
- alarm function
- stop watch
- 20-key multiplexer
- four 7-segment displays with BCD 7-segment multiplexed decoder
- 12 additional, multiplexed LEDs

3 Central Processor

The essential functional units of the central processor are:

- · Central arithmetic unit
 - Arithmetic/logic unit (ALU)
 - Accumulator
- Program memory
- Data memory

not necessary.

- Instruction counter and stack pointer
- · Logic for conditional program branching
- Oscillator, clock supply, and time signals
- Automatic RESET
- Timer/counter
- Input/output port 1
- Internal peripheral interface (IPI)
- Test 1 input

3.1 Central arithmetic unit

This unit carries out all logic and arithmetical operations. It consists of:

- Arithmetic/logic unit (ALU)
- Accumulator
- Carry bit
- Auxiliary carry bit

73% of the instructions (46 from 63) refer to the arithmetic unit.

In most cases, data stored in the accumulator is combined with data from other sources e.g. a register, a RAM cell, or an input/output port,

by processing the data in the ALU, and returning the result to the accumulator.

3.1.1 Arithmetic/logic unit (ALU)

The ALU processes 8-bit data words from one or two sources (accumulator or temporary register) and generates an 8-bit result according to instruction type.

The instruction types are:

- · Addition with and without carry bit
- AND, OR, EXCLUSIVE OR combinations
- Increment and decrement by 1
- Complement
- · Shift left or right
- Exchange half-byte
- Decimal correction with BCD operation
- · Clear accumulator

If an addition generates a carry of the most significant bit, the ALU sets the carry bit CY (overflow flag bit). The CY bit can also be modified by shift instructions, by clear instructions CLR C, or by the complement instruction CLP C. The CY bit can be polled directly via the jump instructions JC and JNC. Decimal arithmetic is made possible by the auxiliary carry bit AC (auxiliary overflow flag bit). It sets the overflow from the bit with the significance 2^3 . The AC bit is required exclusively for decimal adjustment with the instruction DA A.

3.1.2 Accumulator

The accumulator is the most important register. 70% of all instructions (44 from 63) relate to the accumulator. It is the source or destination of most transfer instructions. All data from and to the input/output ports, the internal peripheral interface, the register, the RAM, and the timer/counter, flow via the accumulator.

It is also the operand source and result register of all arithmetic and logic instructions which relate to the accumulator.

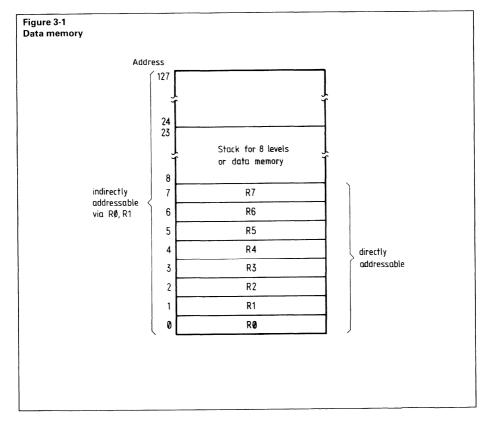
3.2 Program memory

The SAB 80215 contains a mask-programmable 2048×8 -bit program memory. The program memory is not externally extendable. The piggy-back version SAB 80315 allows EPROM SAB 2716 to be used during the program development and in the test phase. The program counter addresses the program memory.

With application of the supply voltage, the program counter is automatically reset, and the program starts with the address Ø. The program memory is divided into 8 pages, each with 256 bytes. This page division is important when using jump instructions. If the program memory overflows, it will be reset to Ø. In the program memory, instruction sequences and constants may be stored. The instruction MOVP A, @ A allows a simple access to tables of constants.

3.3 Data memory

The data memory (figure 3-1) consists of a 128 \times 8-bit dynamic RAM. The addresses \emptyset to 7 are directly addressable as register set by means of additional instructions. The registers \emptyset and 1 allow the indirect addressing of the total RAM area. They, therefore, serve as index register. By means of this, repeated operation to neighbouring memory locations can be comfortably dealt with. The register set with its



8 registers, allows efficient processing of frequently required data.

Memory addresses 8 to 23 can be used as address stack. This stack enables subroutines to be nested to a depth of up to 8 levels.

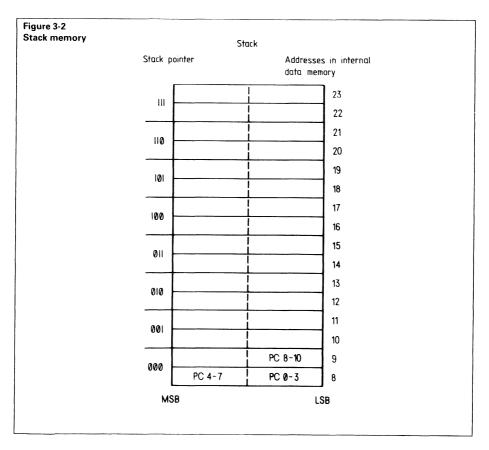
The stack addresses not required in a program can be used like any other RAM location. By applying the supply voltage VCC, the stack pointer is reset to 0, and shows the data memory address 8.

3.4 Instruction counter and stack

The instruction counter controls the program execution. It contains the address of the next instruction to be executed. The instruction counter has a width

of 11 bits, and is thus able to address 2048 bytes. The stack which is to retrieve the return-to-zero addresses in case of subroutine calls, is part of the internal data memory. Each time two bytes of the stack are required to accomodate the instruction counter contents (figure 3-2).

The stack is managed by a 3-bit stack pointer. The stack pointer indicates the next location unoccupied in the stack. If the stack overflows (in case of more than eight levels of subroutine nesting), the stack pointer will again indicate the first address in the stack. After application of the supply voltage, the stack pointer indicates the data memory address 8 and stack address 0. If the instruction counter overflows, program sequence will start again at 0.



3.5 Logic for conditional program branching

The jump logic realized in the central processor, allows the user to poll various conditions.

Table 3-1
Branch instructions

Inquiry unit	Condition	Instruction		
Accumulator	all bits = Ø	not all bits = 0	JZ, JNZ JNC, JC	
Carry bit	0	1		
Timer/counter overflow bit		1	-, JTF	
TEST 1 input T1	0	1	JNT1, JT1	
Register		not all bits = Ø	DJNZ	

3.6 Oscillator, clock supply, and time signals

The SAB 80215 contains also the clock oscillator and the circuit to generate the necessary time signals.

The clock can be supplied by an external 3 MHz crystal between XTAL 1 and XTAL 2, or an external 3 MHz signal applied to XTAL 1. The crystal determines the exact time.

Any internal time slots are derived from the frequency of this oscillator. An instruction cycle consists of 10 states, and each state is a time slot of 3 oscillator periods.

Figure 3-3 shows the oscillator wiring options. The duration of one instruction cycle is 10 us. Via the internal peripheral interface, various internally generated timing pulses can be applied to the T1 input, and polled by means of the conditional branch instructions JT1 and JNT1, or they can be used as clock input of the 8-bit counter. The frequencies are ½60 Hz, ½10 Hz, 1 Hz, 10 Hz, 50 Hz, 100 Hz, 1 kHz, and 10 kHz. Further time signals can be generated by the 8 and 12-bit timers. They are described in paragraph 3.11.

Further timing conditions can be obtained by reading the clock registers. Figure 3-4 shows the time at which the data becomes valid if output at port 1, and when it has to be applied to the input.

3.7 Automatic reset

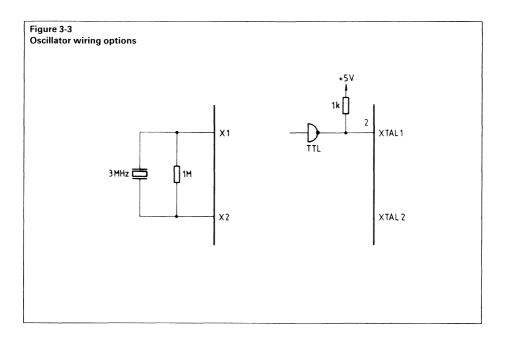
The SAB 80215 has no RESET input as is usual with a microcomputer. The device is automatically set to its initial state by application of the supply voltage. If it is required to reset the computer during operation, this can be done by interrupting the supply voltage.

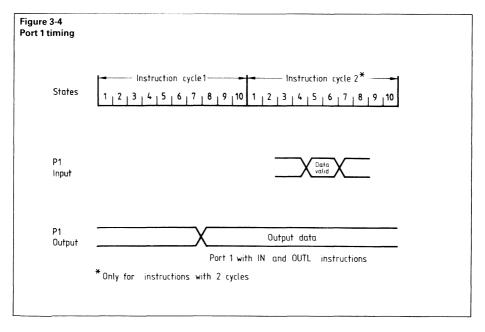
For the RESET signal to be properly applied the following conditions must be observed:

- VDD lies within the specified tolerance
- VCC must be smaller than 0.9 \times VDD for at least 50 μs . This means, that if both voltages are switched on simultaneously, the rise of VCC over VDD must be delayed.

Moreover, it is to be observed that during normal operation VCC should not fall below $0.9 \times \text{VDD}$ (as this would cause a RESET).

The status register bit 4 is set by applying the standby-current supply VDD, and reset by writing in the status register. By means of this bit, it can be ascertained whether the computer was fully powered up initially or whether it was switched from standby to active state. Therefore, appropriate polling enables branching to various start-up programs. In the initial state, the instruction counter, and the stack pointer are set to zero, and port 1 to "1"-The timer/counter is in halt state. The total turn-on time is approx. 20 ms.





3.8 Standby mode

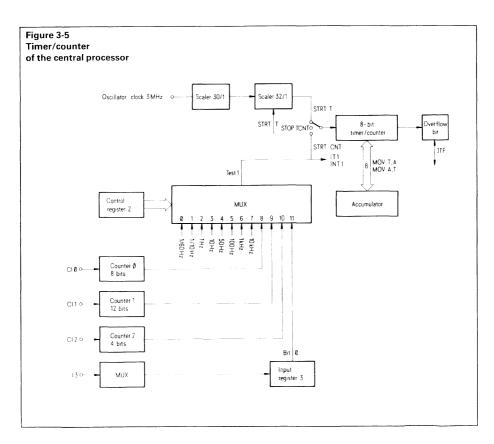
The standby current supply VDD secures the RAM contents, the clock, the stop watch, the alarm function, and some control functions. With the operating voltage VCC switched off, the current consumption is ≤ 5 mA. The operating voltage is turned on again by means of switching signal RSS generated via the alarm. The switching signal RSS can also be controlled by setting/resetting the status register bit 7. Thus the processor can switch over to standby mode under program control.

By reading status register bit 7 after the supply voltage VCC has been switched on, it can be ascertained whether the system was switched on by the alarm or externally by the user, and corresponding program branches can be made.

3.9 Timer/counter

The 8-bit timer/counter of the central processor is described separately as its operation differs considerably from the three counters of the internal peripherals (see figure 3-4).

The timer/counter serves to generate timing signals and/or to count external events which occur during the program flow. The counter is 8 bits wide, counts upwards, and is preset with the MOV T, A instruction and read out by MOV A, T. The counter is not set to 0 at switch-on but it is in halt state. The timer/counter is stopped by the instruction STOP TCNT. It remains in this state until the timer is started with STRT T, or the event counter is started with STRT CNT. After being enabled, the timer/counter is incremented up to FFH and starts again at 0. The counter overflow sets the timer flag.



This bit can be polled by the instruction JTF. After execution of the instruction, the timer flag is cleared.

The timer function is called by instruction STRT T. Thereby, a pulse derived from the oscillator is applied to the timer input.

The input frequency is 3.125 kHz (320 µs) and the corresponding counter output frequency 12.2 Hz (81.92 ms). Longer frequency duration can easily be achieved with the aid of the software. First, the oscillator frequency is internally divided by 30. The resulting clock time corresponds to one instruction cycle (10 µs). An additional 6-bit counter, reset to 0 by instruction STRT T, controls the counter input upon overflow. Thus, the processor input clock can be started with an accuracy of ½2 of the counter clock. In the event counter mode, several timer functions can be similarly implemented. The instruction STRT CNT switches the counter input to Test 1 signal.

By means of the T1 multiplexer, various test fre-

quencies can be applied to the counter input via the internal peripheral interface IPI. The frequencies are 1/60 Hz, 1/10 Hz, 1 Hz, 10 Hz, 50 Hz, 100 Hz, 1 kHz, and 10 kHz. Moreover, the counter outputs of counters 0 to 2 can be applied to T1. Since CI1 can also operate as timer, additionally adjustable time slot patterns result. Operation of the T1 signal and of counters 0 to 2 is described in paragraphs 5.2 and 5.4. In the event counter mode, the central processor can poll the 0 bit of input register 3 via T1. Since the input register's inputs are multiplexed, its use for event counting is limited. Refer also to the description of the MUX input interface in paragraph 5.7.3. To count events, counters Ø to 2 can be directly connected in series with the timer/counter of the central processor, as described in paragraph 5.4.

All signals applied to T1 can be switched to the 8-bit counter of the central processor, i.e. the frequencies are once more divided by 256. The clock which can be set and read by the program, may also gain up to 24 hours from the program time.

Table 3-2 8-bit timer functions of the central processor

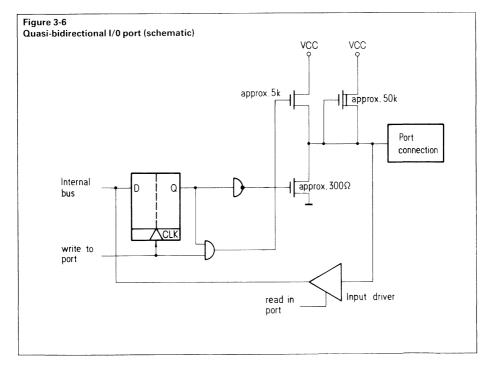
Frequency	Unit	Time	Unit	
timer of the centra	processor only		1	
3.125	kHz	320	μs	
via T1				
1/60	Hz	60	S	
1/10	Hz	10	s	
1	Hz	1	s	
10	Hz	0.1	s	
50	Hz	20	ms	
100	Hz	10	ms	
1	kHz	1	ms	
10	kHz	100	μs	
via T1 and counter	1 as timer			
12.2	Hz	81.92	ms	

3.10 I/O port 1

The 8-bit parallel, quasi-bidirectional I/O port 1 is also a part of the central processor. Quasi-bidirectional means that each port can be used independently of the other for input or output or both. Figure 3-6 shows the corresponding circuit schematic.

The data output by port 1 (OUTL P1, A) is statically stored in the port. The data remains unchanged until the next output instruction occurs. Input data is not stored, i.e. inputs must be esent until read by an input instruction (IN A, P1). If a 0 is written, the output can receive the current of a TTL load. If a 1 is written, a high current ($5\,\mathrm{k}\Omega$ to +) is supplied from the output to

enable fast data transfer. After a short time (1µs), the low pullup resistor is switched off, and a comparatively higher resistor (50 k Ω to +) maintains the ,,1" state, whilst the current suffices for a TTL load. In this state, however, the output can be overwritten by any circuit that is capable of accommodating the low current supplied due to the highly resistive pullup resistor. Thus the output becomes an input readable by an input instruction. This means that by writting a ,,1" to any port bit, this pin serves either as an output line in ,,H" state, or as an internal pullup resistor for an input line. After automatic reset, port 1 is in the ,,H" state.



4 Internal Peripheral Interface IPI

4.1. Data traffic principle

Any data traffic between central processor and internal peripheral components flows through the IPI. The data source/drain is defined by a 4-bit address. The address is provided in the IPI address register (IPIA). The IPIA is loaded with the instruction OUTL P2, A. The assignment of addresses to the internal peripheral components is shown in table 4-1. Data is transferred to the IPI by instruction OUTL P0, A, and from the IPI by instruction IN A, P0.

4.2. IPI addresses and data handling

The data width in the various IPI components is one or two bytes. In the latter case, the two bytes are to be transferred one after the other, and it is sufficient to provide the address of the first byte. The internal execution control increments the address register automatically prior to the 2nd access. The instruction sequence to read the clock might be as follows:

MOV A, # Ø BH; clock address to accumulator
OUTL P2,A; address to IPI address register
IN A, PØ; clock minutes to accumulator
NOV R7, A; clock minutes to register 7
IN A, PØ; clock hours to accumulator

The instruction sequence for writing into an IPI component is effected with the instruction OUTL P0, A accordingly. The addresses flow through the internal port 2, and the data through the internal port 0.

Table 4-1
Assignment of the IPI addresses to the IP components

Address	Byte	Read	Write
Ø	1	Input memory Ø	
	2	Input memory 1	_
1	1	Input memory 2	_
	2	Input memory 3	
2		_	
3			Hours counter + 1
4	1	A/D converter data	A/D control word
5	1	Counter Ø	Counter Ø
6	1	Counter 1, bits Ø to 7	Counter 1, bits Ø to 7
	2	Counter 1, bits 8 to 11, counter 2	Counter 1, bits 8 to 11, counter 2
7	1	Output memory Ø	Output memory Ø
8	1	Output memory 1	Output memory 1
9	1	Output memory 2	Output memory 2
	2	Output memory 3	Output memory 3
Α	1	mays:	Brightness control, bits Ø to 7
	2	-	Brightness control, bit 8
В	1	Clock minutes	Clock minutes
	2	Clock hours	Clock hours
С	1	Alarm memory minutes	Alarm memory minutes
	2	Alarm memory hours	Alarm memory hours
D	1	Control register 1	Control register 1
E	1	Control register 2	Control register 2
F	1	Status register	Status register

5 Internal Peripheral Components

The internal peripheral components are operated via the internal peripheral interface. The exchange of information between the accumulator and the internal peripherals comprises statements to control and to transfer data from or to the individual circuit parts. Test 1 input (T1) is an additional interface to the central processor. It allows different states of the peripherals to be evaluated by direct polling or direct coupling with the input of the central processor's timer/counter.

The internal peripherals include:

- status register
- control registers 1 and 2
- T1 multiplexer
- A/D converter with multiplexer
- 3 timers/counters
- · clock with alarm function
- stop watch
- MUX input interface for 20 keys
- MUX output interface for 12 individual LEDs and 4 x 7-segment displays including encoder and brightness control

5.1 Status and control registers 1 and 2

The status register and both control registers are of central importance for the control of internal peripherals. The registers have read/write capability.

5.1.1 Status register

The access address for the status register is ØFH. The status register indicates various system states, and by setting and resetting certain bits various actions can be triggered. Several bits can be set or cleared at the same time. Some bits are supplied by standby current. These bits are shown in the schematic representation of the status register (figure 5-1). Some status register bits have a different meaning depending on whether reading or writing takes place.

The status register indicates:

- Bit 4 is set to 1 after application of standby current supply VDD. In this way, the central processor can decide after a RESET whether both supply voltages VCC and VDD, or only VCC have been switched off. It is assumed that bit 4 has been cleared in an earlier program section.

 Bit 4 is cleared through every write instruction to the status register. Bit 4 is supplied by the standby current.
- Bit 7 Upon reading, this bit indicates the status of a flip-flop that is set by the alarm. Reading the status register clears this flip-flop.

 The switching of the RSS signal from the high impedance to the low-impedance L

state, caused by the alarm, is not influenced by a clearing of the flip-flop. Bit 7 is supplied by the standby current.

The following are controllable via the status register:

- Bit Ø By means of a written-in 1, it is possible to apply a 1 Hz pulse instead of the contents of bit Ø to the output register 1. This 1 Hz pulse has a duty cycle of t_{in}/t_{out}= 0.4/0.6 seconds.

 Both edges are displaced, compared with the 1 Hz pulse of the T1 multiplexer. An obvious application is a flashing colon between the hours-minutes indication.
- Bit 0 is not supplied by the standby current.

 Bit 1 permits the display of AM or PM information via the MUX interface instead of the output of bits 1 and 2 of output register 1.
 - $\emptyset = \text{output AM}, PM$
 - 1 = output bits 1 and 2 of output register 1 Bit 1 is not supplied by the standby current.
- Bit 2 switches the clock to American display format if it is set to 1.

Ø means European format.

Bit 2 is supplied by the standby current.

- Bit 3 enables the alarm if it is set to 0. If the alarm memory matches the clock time, the circuit sets the alarm flip-flop (readable via status register bit 7) and switches the RSS switching voltage to the "low" state. The "1" state of bit 3 locks the alarm.
- Bit 3 is supplied by the standby current.
- Bit 4 Upon writing, this bit distinguishes between setting or clearing the marked bit position.
 - 1 = all bit positions marked 1 are set to 1
 - Ø = all bit positions marked 1 are reset to Ø
 The unmarked bit positions remain unaltered.
 Bit 4 is not supplied by the standby current.
- Bit 5 resets the stop watch.
 - 1 = RESET
 - $\emptyset = no effect$

The bit is not stored, Ø appears upon reading. Bit 5 is not supplied by the standby current.

- Bit 6 starts and stops the stop watch
 - 1 = start
 - $\emptyset = stop$

Bit 6 is supplied by the standby current
Bit 7 can be set to 1 by the program. In this case,
the switching voltage turns from the high
impedance state to "L". If the program clears
bit 7, RSS switches again to the high impedance state. Thus, the central processor can,
e.g., switch off its own supply voltage via
external components and reactivate it via the
alarm

Bit 7 is supplied by the standby current. The information stored in bits 0 to 3 and 6 can be read out again.

Table 5-1 Status register

	1	T	T	Υ	Γ	T	1	Γ
Bit State	7	6	5	4	3	2	1	ø
Read	alarm flag 1 = on is reset to Ø by reading	stop watch 1 = stop watch runs; Ø = stop watch stops	Ø	1 after application of VDD is cleared to Ø by writing	alarm function Ø = permit 1 = lock	1 = Am.	output Ø = AM PM 1 = output register 1, bits 1,2	output Ø = output register 1, bit Ø 1 = 1 Hz pulse
Standby current supplied	yes	yes	,max.	yes	yes	yes		_
Write	Standby stop watch storemt 1 = stop		stop watch 1 = RESET 0 = no effect		alarm function Ø = permit 1 = lock	function display 0 = permit format		output Ø = output register 1, bit Ø 1 = 1 Hz pulse
Standby current supplied	yes	yes	_	yes	yes	yes		-

5.1.2 Control register 1

The address DH points to control register 1 (see also table 5-2).
Control register 1 indicates:
Bit 5 overflow bit for counter 2
Bit 6 overflow bit for counter 1

Bit 7 overflow bit for counter Ø

Control register 1 enables the following control functions:

Bit 0-3 Internal test procedures (refer to chapter 8) After the microprocessor start, the bits are at 0.

Bit 4 Ø = input of counter 1 is switched to pin 13 (signal Cl 1).

1 = as long as a "1" is present at pin 12 (signal CI 2, the input of counter 2), a 50 kHz signal is present at the input of counter 1 (see figure 5-1). 50 kHz are 20 µs counting increments or 12.2 Hz for one counter run, respectively.

Bit 5-7 The counter carry bits are cleared by reading from or writing to counter 0 to 2, or by a read instruction from control register 1.

5.1.3 Control register 2

The address EH points to control register 2. This register is readable in a parallel manner and can be written to with one half-byte at a time. A survey is provided in table 5-3.

Table 5-2 Control register 1

Bi	t 7	6	5	4	3	2	1	ø
Read	counter Ø overflow	counter 1 overflow	counter 2 overflow	counter 1 control	test bit 3	test bit 2	test bit 1	test bit Ø
	writing to t	l by reading he counters e control reg	and by	Ø = coun- ter 1 = timer 50 Hz	are reset up of IC; serve for ch	oon turn-on nip testing		
Write	no effect			counter 1 control	test bit 3	test bit 2	test bit 1	test bit Ø
			Ø = coun- ter 1 = timer 50 Hz	are reset up of IC; serve for ch				

Control register 2 indicates only those states set by the central processor itself. It is otherwise left unchanged:

Control register 2 is used to control:

Bits Ø-3 Control of test 1 multiplexer (see paragraph 5.2)

Bit 4 7-segment output from stop watch

Bit 5 7-segment output from output registers 2, 3

Bit 6 7-segment output from the clock

If several bits (bits 4 to 6) are set to 1, the corresponding sources are internally connected

Bit 7 Half-byte selection used in writing

 \emptyset = high-order half byte,

bits 4 to 6

("wired OR").

1 = low-order half byte,

bits Ø to 3

Bit 7 ist not stored and is set to \emptyset for reading. In case of reading, bit \emptyset to 6 show the written-in values.

Table 5-3 Control register 2

Bi	it							
State	7	6	5	4	3	2	1	Ø
Read	Ø	time	A2/A3	stop watch	test 1 multi	plexer conti	oller	
Write	half byte selection	7-	7-segment output			plexer contr	oller	
	\emptyset = bits 4 to 6 1 = bits \emptyset to 3		A2/A3	stop watch				

5.2 Test 1 multiplexer

The test 1 multiplexer switches various time and status signals from the internal peripheral components to the test 1 input of the central processor. The test 1 input can be polled immediately by entering the instructions JT1 and JNT1. It can also be applied to the input of the 8-bit counter in the central

processor via the instruction STRT CNT. This allows additional timer functions to be implemented. The corresponding data source is selected on the basis of the contents of bit 0 to 3 in control register 0.

Table 5-4 shows which control word allows signals from the control register 2 to be applied to the T1 input.

Table 5-4 T1 multiplexer setting options

Control register 2 bits Ø to 3	Data source
0	1/60 Hz clock
1	1/10 Hz clock
2	1 Hz clock
3	10 Hz clock
4	50 Hz clock
5	100 Hz clock
6	1 kHz clock
7	10 kHz clock
8	counter Ø bit 7
9	counter 1 bit 11
Α	counter 2 bit 3
В	input register 3 bit Ø
С	VSS
D	VSS
E	VSS
F	VSS

5.3 A/D converter

The 8-bit A/D converter with three multiplexed inputs responds to the address 4H (refer to table 5-5).

Selection of the input port and converter mode is controlled by the write instruction. This instruction interrupts any conversion currently in operation and starts a new one. The converter can also work consecutively.

The converter utilizes the successive approximation technique. Conversion time lasts 23 µs,

sample time 5 μ s. The sample time is part of the conversion time. It is possible to start the converter, and to read out with the next instruction.

Example

OUTL PØ, A (2-cycle instruction, start of converter in first cycle)

IN A, PØ (2-cycle instruction; conversion ends during fist cycle; during the 2nd cycle the result is transmitted and if necessary a new conversion started)

MOV Rr, A (2nd conversion started)

MOV Rr, A (2nd conversion continues)

IN A, PØ (during first cycle 2nd conversions ends, and during 2nd cycle new result is transmitted as well as 3rd conversion is started) etc.

The input voltage at AN0 through AN2 extends from 0V (VSS) up to the reference voltage VAREF. For VAREF, a value between 1 and 5 V may be chosen.

The conversion word is used to control:

Bit $\emptyset = 1$, ANØ is at converter input

Bit 1 = 1, AN1 is at converter input

Bit 2 = 1, AN2 is at converter input; Only one bit can be set to 1.

Bit 3 = 1 Further conversions will follow the present conversion in consecutive order.

In case of reading, always the latest result will be transmitted.

= Ø The converter stops after the present conversion has ended.

Table 5-5 A/D converter control (address 4)

Bit State	7	6	5	4	3	2	1	ø
Read			resi	ult of latest A	./D conversi	on		
Write		а	ny		1 = continuous conversion Ø = stop at end of conversion	AN2	tion of input AN1	port ANØ

5.4 Timer/counter

Three counters are included in the internal peripheral components of the SAB 80215:

Counter Ø 8 bits Counter 1 12 bits Counter 2 4 bits

Three counters can be directly operated via inputs CI0 to CI2. Counter 1 can also be used as a timer. The counters are constructed for synchronous mode.

Table 5-6 Counter 1 (12 bits) and counter 2 (4 bits)

5.4.1 Structure of the event c

Due to the byte structure of the internal peripheral interface, the three counters are compressed into three bytes.

Counter Ø bits Ø to 7 address 5 Counter 1 bits Ø to 7 address 6 byte 1 Counter 1 bits 8 to 11 address 6 byte 2 Counter 2 bits Ø to 3 address 6 bvte 2 Table 5-6 shows the allocation of counter 1 to the accumulator bits.

Byte No.		1											2			
Accu. bit	7	6	5	4	3	2	1	Ø	7	6	5	4	3	2	1	Ø
Counter		counter 1								cour	nter 2			cour	nter 1	
Bit	7	6	5	4	3	2	1	Ø	7	6	5	4	3	2	1	Ø

5.4.2 Pulse shaping at the input, and input frequency

Every counter is provided with a pulse shaping circuit. This enables pulses with a slow rise time as well as pulses with a minimum width of 100 ns to be counted. The positive edge of the pulse increments the counter. The input frequency range extends from 0 to 100 kHz.

5.4.3 Setting and reading the event counter

Since the counters run synchronously with the computer clock, they can be read from or written to by the central processor without any difficulty. When byte 1 of counter 1 is written, the clock input of counter 1 is blocked until byte 2 of counters 1 and 2 has also been written to. When reading the first byte (counter 1, bits 0 to 7), bits 8 to 11 of counter 1, and bits 0 to 3 of counter 2 are buffered, and transferred to the accumulator when the 2nd byte is read. The manner of switching chosen prevents errors from occurring during the 2-byte transmission phase by transferring bit 7 to 8 of counter 1.

5.4.4 Counter overflow

Each counter has been assigned with a bit in control register 1. This bit is set by the overflow of the corresponding counter.

Counter Ø bit 7 in control register 1
Counter 1 bit 6 in control register 1
Counter 2 bit 5 in control register 1
Writing to or reading from a counter, or reading from the control register 1 resets these bits.

The overflow information of each counter — a falling edge at the highest order output — can be directed to the T1 input of the central processor by setting the T1 multiplexer accordingly. This allows the cascading of one of the counters \emptyset to 2 through the 8-bit counter of the central processor.

5.4.5 Timer mode of counter 1

The 12-bit counter 1 can optionally be used as a timer by means of bit 4 in control register 1. If bit 4 in control register 1 is set to 1, a 50 kHz pulse is available at counter 1 input. The input of counter 2 serves as gate.

Cl2 = 1, counter 1 runs

 $CI2 = \emptyset$, counter 1 stops

5.5 Clock

Hours and minutes are represented internally in BCD code.

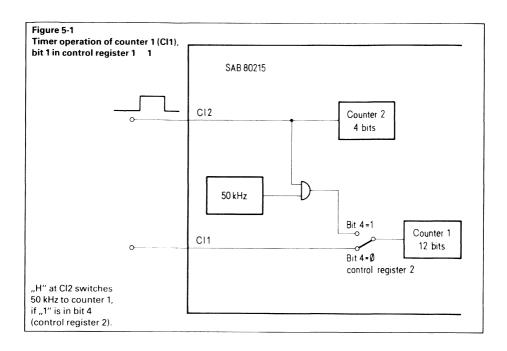
The minutes counter has 7 bits, and the hours counter 6 bits. A comparator circuit continuously checks on a correspondence between the clock time and the contents of the alarm memory. Should they be equal, the alarm flip-flop is set and the signal RSS put to 0 provided that the alarm is enabled.

The clock registers time either in the European (0:00 to 23:59) or the American (1:00 to 12:59 AM/PM) way.

The clock is supplied by the standby current.

5.5.1 Setting, reading, and displaying the time

Clock counters can be read from and written to by the central processor via address BH. The first byte



transmitted contains the number of minutes, the second the number of hours.

Loading the minutes counter resets the internal clock which operates at 100 kHz. Thereafter, the minutes counter resumes counting after a lapse of about one minute. Thus, there is sufficient time to set the hours. Each time the address BH is written to, the hours counter is incremented by 1. The state of the accumulator is of no importance at the time the write instruction is issued. Carries from the minutes counter, possibly occurring during clock setting, become also effective. When setting the clock, attention must be given to the type of notation chosen, i.e. European or American.

Setting bit 6 in control register 2 switches the contents of the clock counters to the inputs of the 7-segment decoders. Unusable bit positions take a 0.

contents of the clock counters to the inputs of the 7-segment decoders. Unusable bit positions take a 0. The leading 0 in the tens is suppressed when hours are displayed. Table 5-7 gives a survey of the various formats used by the hours counter for reading, writing, and displaying.

The PM information for the American time notation is contained in bit 5 of the hours counter. This should be noted when reading or writing. Bit 1 in the status register determines whether, during the MUX 2 phase, the PM information instead of output register 1, bit 2, or the inverse signal (AM) instead of output register 1, bit 1, is output.

5.5.2 Setting European or American time notation

In the European time notation system, the clock runs from 0:00 to 23:59. In the American system, it runs from 1:00 to 12:59 AM/PM. Switching from one system to the other is carried out by setting bit 2 in the status register accordingly.

Bit 2 = 1 American system Bit $2 = \emptyset$ European system

5.5.3 Alarm

The alarm memory can be written to and read from via the address CH. The difference between the European and American manner of notating hours should be taken into account when loading the alarm memory. If the contents of the clock counter corresponds to the contents of the alarm memory and bit 3 in the status register is set to Ø (alarm enable), bit 7 in the status register will be set. This bit can be read by the central processor. In addition, RSS switches to the active state. By this means, the operating voltage VCC can be switched on for a computer in standby state (supplied with standby current).

Table 5-7
Formats of the hours counter

Europea	n format	America	n format	Europea	n format	America	n format
display	write/ read	display	write/ read	display	write/ read	display	write/ read
Ø	00	12 (AM)	12	13	13	1 (PM)	21
1	Ø1	1 (AM)	Ø1	14	14	2 (PM)	22
2	Ø 2	2 (AM)	Ø 2	15	15	3 (PM)	23
3	Ø 3	3 (AM)	Ø 3	16	16	4 (PM)	24
4	04	4 (AM)	04	17	17	5 (PM)	25
5	Ø 5	5 (AM)	0 5	18	18	6 (PM)	26
6	Ø 6	6 (AM)	ø 6	19	19	7 (PM)	27
7	07	7 (AM)	07	20	20	8 (PM)	28
8	Ø 8	8 (AM)	08	21	21	9 (PM)	29
9	09	9 (AM)	ø 9	22	22	10 (PM)	30
10	10	10 (AM)	10	23	23	11 (PM)	31
11	11	11 (AM)	11				
12	12	12 (PM)	32				

5.6 Stop watch

The standby current-supplied stop watch runs internally in BCD code. The time is measured in hours, minutes, seconds, and tenths of seconds. The maximum timing range encompasses 60 hours. If this timing range is exceeded the stop watch will begin again at 0.

5.6.1 Stop watch operation

The stop watch cannot be written to or read from by the central processor. Start, stop, and reset is, however, enabled through the status register. Status register bit 6 = 1 stop watch is running

 $\begin{array}{lll} \mbox{Status register} & \mbox{bit } 6=\emptyset & \mbox{stop watch has stopped} \\ \mbox{Status register} & \mbox{bit } 5=1 & \mbox{stop watch is reset to } \emptyset. \\ \mbox{This bit is not stored in} & \mbox{the status register.} \\ \end{array}$

5.6.2 Stop watch display

If bit 4 in control register 2 is set to 1, the stop watch outputs will be switched to the 7-segment encoder. The current contents of the stop watch, i.e. the time measured, determines which part of the stop watch counter is output in the individual MUX phases. Table 5-8 shows the relationships. Leading zeroes are not displayed.

Table 5-8
Display of stop watch contents in relation to MUX clock and running period

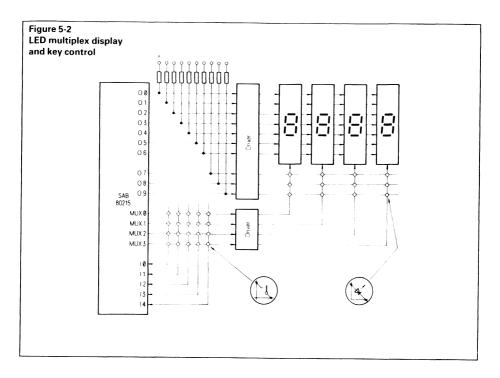
Stop watch running period (t)	MUX phase 3	MUX phase 2	MUX phase 1	MUX phase Ø
$\emptyset \le t < 1 \min$ $1 \min \le t < 1 \text{ hr}$ $1 \text{ hr} \le t < 60 \text{ hrs}$	seconds: tens	seconds: ones	seconds: 10ths	-
	minutes: tens	minutes: ones	seconds: tens	seconds: ones
	hours: tens	hours: ones	minutes: tens	minutes: ones

5.7 MUX I/O interface

The MUX I/O interface operates the multiplexed keyboard input and the 7-segment display. 20 keys can be connected directly in a 4 x 5 matrix without additional hardware or software expenditure. Four 7-segment digits and 12 individual LEDs

are available as indicators. The principal wiring configurations for LEDs are shown in figure 5-2.

The number of display elements and keys can be increased with minimum additional expense. Individual LEDs can principally be combined to form 7-segment indicators.



5.7.1. Principle and extent of data traffic

A 4-stage multiplex procedure controls key scanning and data display. Each phase is utilized twice. Pins 00 to 09 have the output information for the paralleled segments of all 7-segment displays (00 to 06) and for the 12 individual LEDs (07-09).

Information from the key matrix columns is read via the inputs I0 to I4. The multiplex signals select the 7-segment digits and the lines of the key matrix with the signals MUX 0 ... 3 (see figure 5.4). Each multiplex phase lasts 1 ms, a cycle 4 ms. No synchronization exists between central processor and I/O multiplexer.

Multiplex outputs:

During the four multiplex phases, pins MUX Ø to MUX 3 go successively to "H" level for 1 ms each. The other pins stay at "L" level.

Multiplex ouput ports:

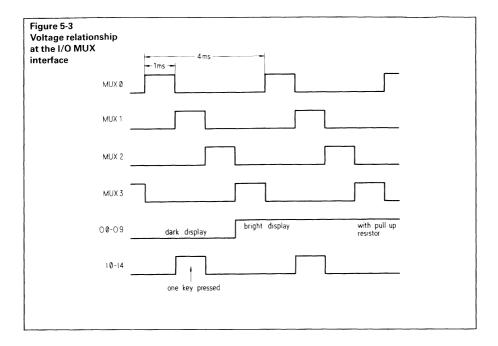
During a multiplex phase, information coming from the 7-segment decoder lies at outputs 00 to 06. Outputs 07 to 09 show part of the contents of the output register 0 and 1, i.e. AM/PM information or 1 Hz pulse.

Whenever an individual display element is to light up, the relevant output must turn to a high-impedance state in the corresponding MUX phase. If the element is to remain dark, the output has to lie at "L" level. The brightness control can draw the potential of the output lines to "L" even before a MUX phase has ended. The outputs 00 to 09 have open drains.

Multiplexer input channels

Each MUX phase sets one row of the keyboard to "H" level. After this state has been reached, information is taken from the key matrix to the input register assigned to the corresponding MUX phase. Internal resistance to VSS draws the input line to "L" level for keys that have not been activated yet. Otherwise, the line will be at "H" level at the given moment. In normal operation no more than one key of the keyboard should be closed. If several keys have been pressed, normal functioning of the key input and display can no longer be assured.

If necessary, the key matrix can be decoupled from the MUX outputs e.g. by means of diodes.



5.7.2 Assigning the MUX phases to the IPI

The MUX input interface has 5 bits, the MUX output interface 10 bits. Tables 5-9 and 5-10 show how they are adapted to the IPI interface.

5.7.3 Input registers

The four 5-bit input registers can only be supplied via inputs IØ to I4 in the corresponding MUX phase. Table 5-9 shows the assignment between input pins, input registers, and accumulator. Input

lines IØ to I4 correspond to bits Ø to 4 of the input registers.

The central processor can read input registers 0 and 1 with address 0, and input registers 2 and 3 with address 1. After reading, bits 0 to 4 of the input register are located in bits 0 to 4 of the accumulator. Bits 5 to 7 of the accumulator are set to 0. Bit 0 of input register 3 can be directed to the T1 input of the central processor (compare description of T1 multiplexer), and can then be directly queried by the central processor. The program should take into account the possibility of key bouncing.

Table 5-9
Assignment MUX input signals — accumulator

MUX phase	Accumulator after input register read-in							
	7	6	5	4	3	2	1	Ø
Ø 1 2 3		Ø			In In	put registe put registe put registe put registe	r 1 r 2	
					M	UX input pi	ins	
			Signal	14	13	12	11	ΙØ
			Pin	19	18	17	16	15

Table 5-10
Output of output registers 2 and 3 via 7-segment encoder

MUX phase 3	MUX phase 2	MUX phase 1	MUX phase Ø
output r	egister 3	output r	egister 2
higher nibble	lower nibble	higher nibble	lower nibble

Table 5-10a Output via lines 07 to 09

Signal	09	08	07				
Pin	11	10	Ø 9				
MUV phase 0		output register ∅					
MUX phase Ø	2	2	Ø				
MALLY Land		output register Ø					
MUX phase 1	6	5	4				
		output register 1					
MUX phase 2	2	1	Ø				
or.pilass 2		or					
	PM	AM	sec. clock				
MUV phage 2		output register 2					
MUX phase 3	6	5	4				

5.7.4 Output registers

The output registers \emptyset and 1 can be written to and read from by the program via the addresses 7H and 8H. They are each 6 bits wide and intended to drive 12 individual LEDs. Accumulator bits \emptyset , 1, 2, and 4, 5, 6 correspond to register bits \emptyset , 1, 2, and 4, 5, 6.

During a multiplex clock pulse the circuit outputs half of one of the two output registers, at 07 to 09. Table 5-10 shows the process.

If bit Ø is set in the status register, a clock pulse over one second (0.4 s on, 0.6 s off) is emitted via output register 1. If bit 1 of the status register has been cleared, the highest order bit 5 of the hours counter will lie at the output instead of the signal from bit 2 of output register 1. Simultaneously with the employment of bit 1 from output register 1, the corresponding, inverse signal is output. This serves for displaying AM/PM if the American time notation has been selected.

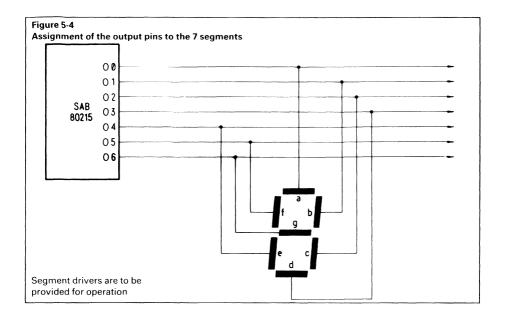
Output registers 2 and 3 can be written to and read from by the program via address 9H. The first byte addresses register 2, the second byte register 3. These registers are provided to display any information on a 4-digit, 7-segment display. The contents of each 4-bit half of the register is converted in the 7-segment encoder during a multiplex clock pulse and output at lines 00 to 06. This assumes that the data registers were selected as data source. Table 5-10 a shows this in schematic form.

5.7.5 7-segment encoder

The encoder converts data coming from the clock, the stop watch, or the output registers 2 and 3, from 4-bit BCD format into 7-segment code. Figure 5.4 shows how signals fed to outputs 00 to 06 are connected with the segments of the display. The assignment of 4-bit date display to output dates can be taken from table 5-11. To display the required digit, the segments are driven via binary numbers 0 to 9 at the input of the 7-segment decoder. With AH, only the center segment will light up. With BH to FH, the display will remain dark.

Table 5-11
Assignment of I/O date and 7-segment display

4-bit input date (bits Ø to 3)	Display	7-bit output date (00 to 06 = a to g)
Ø		3F
1	!	06
2	5	5B
3	טייט פין דט רטיבי פיט מט	4F
4	4	66
5	5	6D
6	5	7D
7	-;	07
8	8	7F
9	5	6F
А	_	40
В		00
С		00
D	dark	00
E		00
F		00



5.7.6 Brightness control

When a programmable period of time has elapsed after the beginning of a multiplex phase, the brightness control sets output lines 00 to 09 to 0 for the rest of the phase. There are two temporal (i.e. brightness) ranges.

In the lower (dark) range, the time can be set in 1 μs units between 0 and 99. In the upper (bright) range, the values can be selected in 10 μs units between 0 and 99. In each case, the range comprises 100 steps. Thus, a matching to the logarithmic eye-sensitivity curve is possible.

Using the address AH, the program writes a number between \emptyset and 99 in BCD code into the first byte. The range is chosen according to the state of bit \emptyset in the second byte.

 $\emptyset = 1$ us steps in the dark range 1 = 10 us steps in the bright range

If a number larger than 99 is written into the highorder or low-order tetrade, 1000 us will always be set. This makes it possible to select the entire brightness range within each 1 ms MUX phase. Table 5-12 shows the control format.

Table 5-12 Brightness control

Bit	7	6	5	4	3	2	1 .	Ø	
Byte 1	-	_	_	_	_	_		_	
		increments in BCD code from Ø to 99							
Bit	7	6	5	4	3	2	1	Ø	
Byte 2	-	-	_	_	_	_	_	$0 = 1 \mu s$ $1 = 10 \mu s$	

SAB 80215

6 Instruction Set

6.1 Symbols and abbreviations

A	Accumulator
AC	Auxiliary carry
Addr	Program memory addresses
An	Accumulator contents before shift instruction
An + 1	Accumulator contents after shift instruction
CY	Carry
CNT	Event counter
Data	8-bit number or expression
IPI	Internal peripheral interface (PØ)
IPIA	Internal peripheral interface address (P2)
P	I/O port
Page	Program memory block with 256 addresses
PC	Program counter
Rr	Register Ø to 7
SP	Stack pointer
Т	Timer
TF	Timer/counter – overflow flag
\rightarrow	is moved to
\longleftrightarrow	is exchanged with
()	Contents
(())	Contents of contents
#	Immediate data prefix, 8 bits
@	Indirect address prefix contained in registers 0 and 1
\uparrow	Instruction activates flag

6.21	nstruction	set	summary
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Mnemonic	Function	Description	Hex code	Flag	Bytes	Cycles
Accumulator and r	egister move instru	ctions				
MOV A, Rr	(Rr) → A	Move register	F8 to FF		1	1
MOV A,@Rr	((Rr)) → A	to accumulator Move data memory to accumulator	FØ to F1		1	1
MOV A, #data	data → A	Move immediate data to accumulator	23		2	2
MOV Rr, A	(A) → Rr	Move accumulator to register	A8 to AF		1	1
MOV @Rr,A	(A) → (Rr)	Move accumulator to data memory	AØ to A1		1	1
MOV Rr, #data	data → Rr	Move immediate data to register	B8 to BF		2	2
MOV @Rr, #data	data → (Rr)	Move immediate data to data memory	BØ to B1		2	2
XCH A,Rr	(Rr) ↔ (A)	Exchange register with accumulator	28 to 2F		1	1
XCH A,@Rr	((Rr)) ↔ (A)	Exchange data memory with accumulator	20 to 21		1	1
XCHD A,@Rr	((Rr)) Ø to 3 ↔ (A)	Exchange bits Ø to 3 of data memory with accumulator	30 to 31		1	1
MOVP A,@A	(PC) save (A) \rightarrow PC 0 to 7 ((PC)) \rightarrow A (PC) restore	Move current page data to accumulator	А3		1	2
SWAP A	(AØ to 3) ↔ (A4 to 7)	Swap nibbles of accumulator	47		1	1
Timer/counter mo	ve instructions			1		
MOV A,T	(T) → A	Move timer/counter	42		1	1
MOV T,A	(A) → T	to accumulator Move accumulator to timer/counter	62		1	1
Internal peripheral	interface move inst	ructions		1	1	
OUTL P2,A	(A) → P2	Output accumulator	3A		1	2
IN A, PØ	$(P\emptyset) \rightarrow A$	to IPI address register Input IPI data (P0) to	Ø8		1	2
OUTL PØ,A	(A) → PØ	accumulator Output accumulator data to IPI (PØ)	90		1	2
Port 1 move instru	ctions					
IN A, P1	(P1) → A	Input port 1 data to accumulator	Ø9		1	2
OUTL P1, A	(A) → P1	Output accumulator data to port 1	39		1	2

Mnemonic	Function	Description	Hex code	Flag	Bytes	Cycles
Arithmetic accumulator inst	ructions					
ADD A, Rr	$(A) + (Rr) \rightarrow A$	Add register to accumulator	68 to 6F	AC, CY	1	1
ADD A,@Rr	$(A) + ((Rr)) \rightarrow A$	Add data memory to accumulator	60 to 61	AC, CY	1	1
ADD A, #data	(A) + data → A	Add immediate data to accumulator	03	AC, CY	2	2
ADDC A, Rr	(A) + (Rr) + (CY) → A	Add register and carry to accumulator	78 to 7F	AC, CY	1	1
ADDC A,@Rr	$(A) + ((Rr)) + (CY) \rightarrow A$	Add data memory and carry to accumulator	70 to 71	AC, CY	1	1
ADDC A, #data	(A) + data + (CY) → A	Add immediate data and carry to accumulator	13	AC, CY	2	2
INC A	(A) + 1 → A	Increment accumulator	17		1	1
DEC A	$(A) - 1 \rightarrow A$	Decrement accumulator	07	ė	1	1
DA A	(A HEX) → (A BCD))	57	CY	1	1
Arithmetic register instruction	ons					
INC Rr	(Rr) + 1 → Rr	Increment register	18 to 1F		1	1
INC @ Rr	$((Rr)) + 1 \rightarrow (Rr)$	Increment data memory	10 to 11		1	1
DJNZ Rr, addr	$(Rr) - 1 \rightarrow Rr$ if (Rr) not \emptyset addr $\rightarrow PC$	Decrement register and jump if not zero	E8 to EF		2	2
Logical accumula register instruction						
ANL A, Rr	$(A) \land (Rr) \rightarrow A$	Logical AND register to accumulator	58 to 5F		1	1
ANL A, @ Rr	$(A) \wedge ((Rr)) \rightarrow A$	Logical AND data memory to accumulator	50 to 51		1	1
ANL A, #data	(A) ∧ data → A	Logical AND immediate data to accumulator	53		2	2
ORL A, Rr	$(A) \lor (Rr) \rightarrow A$	Logical OR register to accumulator	48 to 4F		1	1
ORL A, @ Rr	$(A) \lor ((Rr)) \rightarrow A$	Logical OR data memory to accumulator	40 to 41		1	1
ORL A, #data	(A) ∨ data → A	Logical OR immediate data to accumulator	43		2	2

Mnemonic	Function	Description	Hex code	Flag	Bytes	Cycles
XRL A, Rr	(A) ∨ (Rr) → A	Logical EXCLUSIVE OR register to accumulator	D8 to DF		1	1
XRL A, @ Rr	(A) ∨ ((Rr)) → A	Logical EXCLUSIVE OR data memory to accumulator	DØ to D1		1	1
XRL A, #data	(A) ∨ data → A	Logical EXCLUSIVE OR immediate data to accumulator	D3		2	2
CLR A CPL A	$\emptyset \to A$ $(\overline{A}) \to A$	Clear accumulator Complement accumulator	27 37		1	1

Rotate instructions

RL A	$(An) \rightarrow An + 1$ A7 $\rightarrow A\emptyset$	Rotate accumulator left	E7		1	1
RLC A	$(An) \rightarrow An + 1$ $(CY) \rightarrow A\emptyset$ $(A7) \rightarrow CY$	Rotate accumulator left through carry	F7	CY	1	1
RR A	$(An + 1) \rightarrow An$ $A\emptyset \rightarrow A7$	Rotate accumulator right	77		1	1
RRC A	$(An + 1) \rightarrow An$ $(CY) \rightarrow A7$ $(A\emptyset) \rightarrow CY$	Rotate accumulator right through carry	67	CY	1	1

Flag instructions

CLR C	$\emptyset \to CY$	Clear carry bit	97	CY	1	1
CPL C	$(\overline{CY}) \to CY$	Complement carry bit	A7	CY	1	1

Branch instructions

JMP addr	addr0 to 10 →	Jump to address page Ø	04	T	2	2
	PCØ to 10	1	24		2	2
		2	44		2	2
		3	64		2	2
		4	84		2	2
		5	A4		2	2
		6	C4		2	2
		7	E4		2	2
JMPP @ A	$((A)) \rightarrow PC \emptyset \text{ to } 7$	Jump to address of	B3		1	2
		program memory				1
JC addr	(CY) = 1, addr →	Jump to address if	F6		2	2
	PCØ to 7	carry is set			_	_
	$(CY) = \emptyset,$	·	1			
	$(PC) + 2 \rightarrow PC$					
JNC addr	$(CY) = \emptyset$, addr \rightarrow	Jump to address if	E6	l	2	2
	PC Ø to 7	carry is not set				
	(CY) = 1, (PC) + 2					
	\rightarrow PC]				

Mnemonic	Function	Description	Hex code	Flag	Bytes	Cycles
JZ addr	$(A) = \emptyset$ addr \rightarrow PC \emptyset to 7, (A) = 1, (PC) $+ 2 \rightarrow$ PC	Jump if accumulator is 0	C6		2	2
JNZ addr	(A) = 1, addr $\rightarrow PC \emptyset$ to 7 $(A) = \emptyset (PC) + 2 \rightarrow PC$	Jump if accumulator is not Ø	96		2	2
JT1 addr	T1 = 1, addr \rightarrow PC 0 to 7 T1=0,(PC)+2 \rightarrow PC	Jump if test input is 1	56		2	2
JNT1 addr	T1 = \emptyset , addr \rightarrow PC \emptyset to 7 T1 = 1, (PC) + 2 \rightarrow PC	Jump if test input is Ø	46		2	2
JTF addr	TF = 1, addr \rightarrow PC Ø to 7, Ø \rightarrow TF TF = Ø, (PC) + 2 \rightarrow PC	Jump if timer/counter flag is 1	16		2	2
Subroutine instr	uctions		•			
CALL addr	$ (PC0 \text{ to } 10) \rightarrow (SP) $ $ (SP) + 1 \rightarrow SP $ $ addr \emptyset \text{ to } 7 \rightarrow PC \emptyset \text{ to } 7 $ $ addr 8 \text{ to } 10 \rightarrow PC 8 \text{ to } 10 $	Jump to subroutine page 0 1 2 3 4 5 6 7	14 34 54 74 94 B4 D4 F4		2 2 2 2 2 2 2 2 2	2 2 2 2 2 2 2 2 2
RET	$(SP)-1 \rightarrow SP$ $((SP)) \rightarrow PC$	Return from subroutine	83		1	2
Control instruction	ons					
STRT T STRT CNT STOP TCNT NOP		Start timer Start counter Stop timer/counter No operation	55 45 65 00		1 1 1	1 1 1 1

7 Operating Characteristics

7.1 Maximum ratings (referred to VSS = 0 V)

Symbol	Designation	V	alues	Unit
		min.	max.	
VCC	Supply voltage			
VDD	Supply voltage for standby mode	-0.3	6	V
VIN	Input voltage			1
Ptot	Total power dissipation		1	W
PQ	Power dissipation per output	_	30	mW
Tstg	Storage temperature range	-40	150	0.0
Tj	Junction temperature		150	° C
RthSA	Thermal resistance		50	K/W

7.2 Operating conditions (referred to VSS = 0 V)

Symbol	Description	Values			Unit	Test conditions	
		min.	typ.	max.			
VCC	Supply voltage	0.9 VDD	5	5.5	V	-	
ICC	Supply current	_	40	100	mA	VCC = 5 V	
VDD	Supply voltage for standby mode	4.5	5	5.5	v	_	
IDD	Standby current			10	mA	for SAB 80215	
100	Standby Current	-		5	7 1114	for SLE 43215	
Tamb	Ambient temperature range	0	_	70	J c	for SAB 80215	
Tarrib	Ambient temperature range	-30		85	7	for SLE 43215	
trCC	Rise time of supply voltage	300		_	μS	_	

7.3 Characteristics (Tamb = 25° C; VCC = VDD = 5 V; VSS = 0 V; unless specified otherwise) 7.3.1 Input signals (see figure 7-1) Key inputs 10 to 14

Symbol	Description		Values			
		min.	typ.	max.	7	
VIH	H input voltage	2.0		VCC	1,,	
VIL	L input voltage	-0.3	1-	0.8	7 V	
II	Current consumption at VIH = 6 V (internal pull down)	10	40	120	μΑ	
tIBM	Permitted data change before end of MUXn	15				
tIAM	Data hold time after end of MUXn	0	7-	-	μs	

Analog inputs ANØ to AN2 (VCC = 5 V)

Symbol	Designation		Values	;	Unit	Test conditions
		min.	typ.	max.	1	
ANi	Test voltage	VSS		VAREF	V	-
Ri	Internal resistance of measurement source]-	10	kΩ	without external capacitance 1)
CI	Input capacitance		25	-	pF	-
	Non-linearity		±1/2	± 1		
	Offset error	_	-1	-1±1	1	
	Gain error				LSB	VAREF = 5V
	Total error 2) (incl. quantization error)		±1/2	±1		
Ts	Sample time		-	7	μs	clock frequency 3 MHz

Reference voltage VAREF

Symbol	Description		Values			nit Test conditions	
		min.	typ.	max.			
VAREF	Reference voltage	1		VCC+0,5	V	_	
RREF	Internal resistance of ref. voltage source	_		3	kΩ	without external capacitance 1)	
CI	Input capacitance		30	-	pF	_	

Input/output ports P10 bis P17

Symbol	Designation		Value	Unit	Test conditions	
		min.	typ.	max.	1	
VIH	H input voltage	2.0		VCC		_
VOH	H output voltage	2.4	2.4 –			$IOH = -50\mu A$
VIL	L input voltage	-0.3		0.8	\ \	_
VOL	L output voltage	-		0.45	1	IOL = 1.6 mA
tWH	H pulse width	10	1		1	
tWL	L pulse width	10		-	μs	-
II	Input current	-		-500	μА	0.45 V ≤ VI ≤ VCC
CI	Input capacitance			25	pF	_

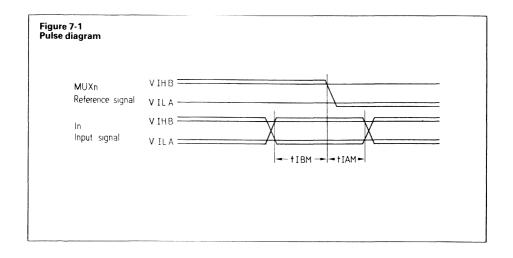
Ports are not short-circuit protected, internal source resistance/load resistance \geq 1 k Ω

7.3.2 Output signals 00 to 09

Symbol	Description		Value	Unit	Test conditions	
		min.	typ.	max.	1	
VQH	H output voltage			-	v	open drain
VQL	L output voltage	_		0.45	7 °	IQL = 4 mA
tDQ	Delay time	0	7-	1	μs	see figure 8-2
IQLEAK	Leakage current	_		-10	μΑ	-0.45 V ≤ VQ ≤ +15 V

¹⁾ Higher values for Ri or RREF can be obtained by connecting an external capactitance between ANi or VAREF and ground.

²⁾ Externally settable; refer to application notes.

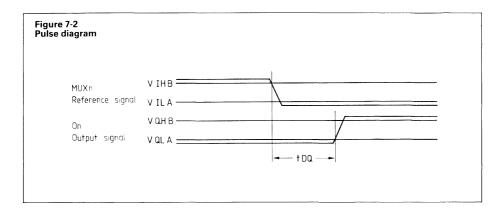


Counter inputs CIØ to CI2

Symbol	Description		Values				
		min.	typ.	max.			
VIH	H input voltage	2.0		VCC	1,,		
VIL	L input voltage	-0.3		0.8	\ \		
tWH	H pulse width	0.1	7-				
tWL	L pulse width	0.1		-	μS		
fl	Input frequency	dc		100	kHz		
CI	Input capacitance	-	20	-	рF		
VHys	Hysteresis		0.1	1	V		

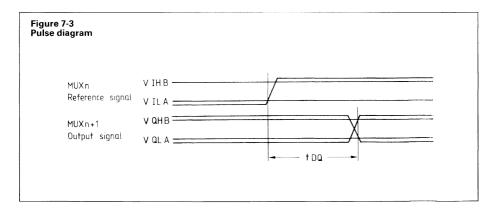
Oscillator input XTAL1

Symbol	Description		Value:	S	Unit	Test conditions
		min.	typ.	max.	1	
VIH	H input voltage	3.8		VCC	1,,	
VIL	L input voltage	-0.3	-0.3		∀ ∨	
tWH	H pulse width	0.1	0.1 - 0.8			external clock
tWL	L pulse width	0.1			μS	to XTAL1
tTHL	L pulse transition time		1	0.00	1	
tTLH	H pulse transition time	_		0.03		
CI	Input capacitance		25		pF	VI = 0V
tCY	Cycle time	0.31	0.33	1.65	μs	_
tEXT	External clock	-	-	-	-	connected to XTAL1



Multiplex outputs MUX Ø to MUX 3

Symbol	Designation		Value	Unit	Test conditions	
		min.	typ.	max.		
VQH	H output voltage	2.4	3.2	1-	.,	IQH = −500 µA
VQL	L output voltage	-		0.45	1	IQL = 2 mA
tDQ	Delay time	0	1	1	μS	see figure 7-3



Standby current switching signal RSS

Symbol	Designation		Value	Unit	Test conditions	
		min.	typ.	max.		
VQH	H output voltage -		V	open drain		
VQL	L output voltage			0.45	7 v	IQL = 2 mA
IQLEAK	Leakage current		-	10	μA	$ \begin{array}{c} -0.45 \text{ V} \leq \\ \text{VQ} \leq +15 \text{ V} \end{array} $
IQL	L output current	6	20	-	mA	VQL = 1V

8 Application Notes

8.1 Circuit example for power supply

The SAB 80215 has two voltage supplies: VCC and VDD. VDD provides the standby current, VCC supplies the central processor and associated components.

With a failure of VCC, the RAM, clock, stop watch, and alarm still remain operable.

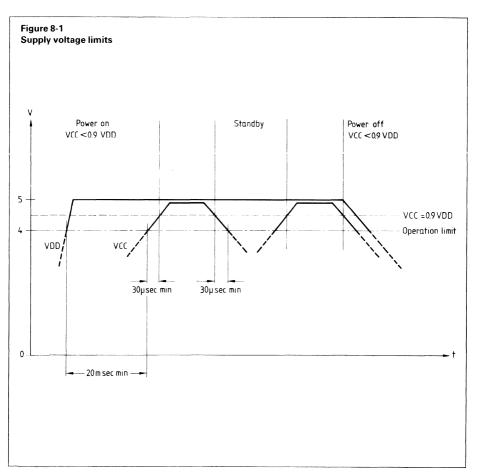
When turned on, the IC automatically carries out a RESET. For trouble-free operation of the RESET and standby-current function, VDD must be applied before VCC when the IC is turned on, and after VCC when it is turned off. In addition, there are specified minimum rise and fall times (figure 8-1).

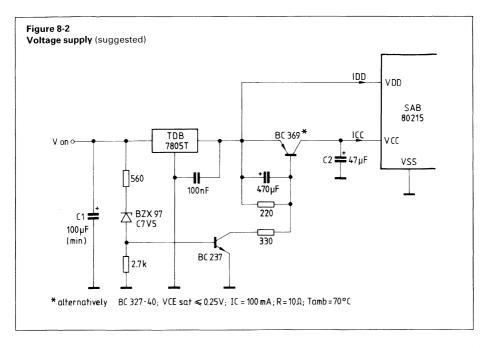
It is important, that the voltage leading and falling edges are symmetrical in operation. No failures in supply are to occur, as may e.g. be caused by switch contact bounce or by regulators vibrating at the switching instant.

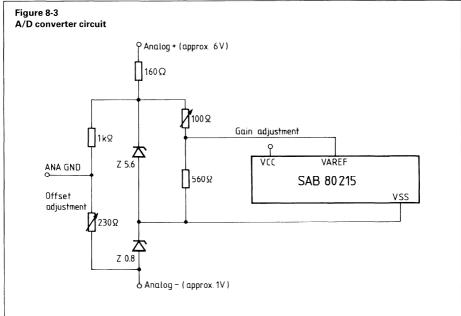
The RESET function can also be forced by applying 12 V to pin 24 signal MUX0 (longer than 100 ms).

8.2 A/D converter circuit

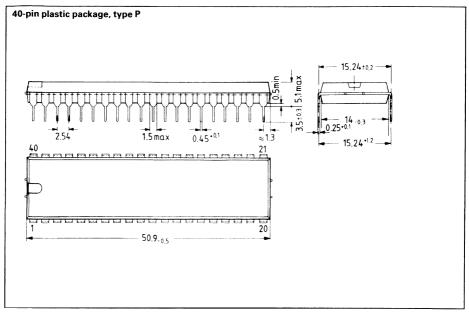
The application circuit (figure 8-3) shows the way in which the total error may be kept low by adjusting amplification and offset.

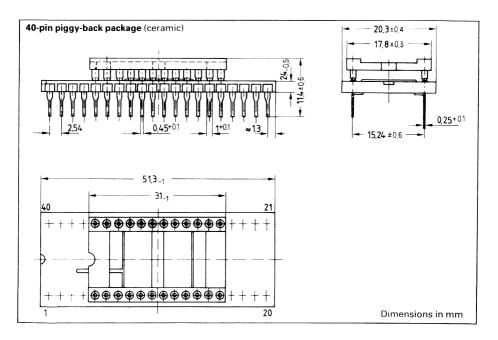






9 Package Outlines





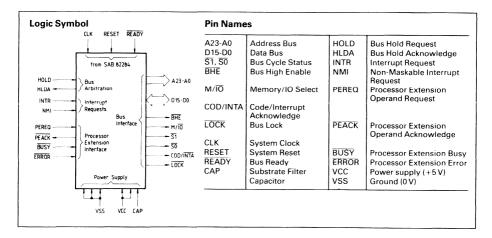
SAB 80215

10 Ordering Information

Туре	Description	Ordering code
SAB 80215 P	8-bit single-chip microcomputer with mask-programmable ROM (plastic)	Q 67120-C81
SAB 80315 D	SAB 80215 ROM-less in piggy-back package (ceramic)	Q 67120-C82
SLE 43215 P	SAB 80215 P with improved data as to operating temperature range and standby current consumption (plastic)	Q 67120-C92
SLE 43315 D	SLE 43215 ROM-less in piggy-back package (ceramic)	Q 67120-C93

SAB 80286 High-Performance Microprocessor with Memory Management and Protection

- High-performance processor (up to six times the SAB 8086)
- Large address space:
 - 16 megabytes physical
 - 1 gigabyte virtual per task
- Integrated memory management, four-level memory protection and support for virtual memory and operating systems
- Two SAB 8086 upward-compatible operating modes:
 - SAB 8086 real address mode
 - protected virtual address mode
- High bandwidth bus interface (8 megabyte/s)
- Full hardware and software support

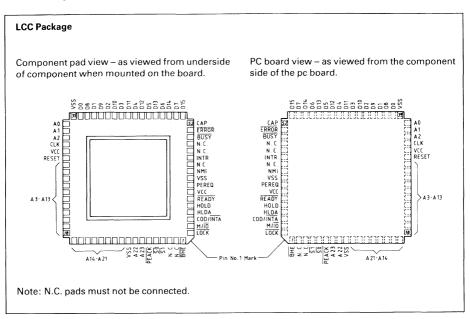


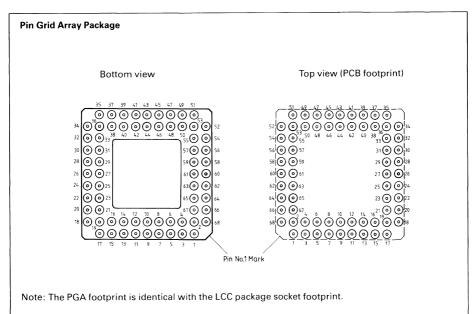
The SAB 80286 is an advanced, high-performance microprocessor with specially optimized capabilities for multiple user and multitasking systems. The SAB 80286 has built-in memory protection that supports operating system and task isolation as well as program and data privacy within tasks. An 8 MHz SAB 80286 provides up to six times greater throughput than the standard 5 MHz SAB 8086. The SAB 80286 includes memory management capabilities that map up to 2³⁰ (one gigabyte) of virtual address space per task into 2²⁴ bytes (16 megabytes) of physical memory.

The SAB 80286 is upward-compatible with SAB 8086/8088 software. Using SAB 8086 real address mode, the SAB 80286 is object code compatible with existing SAB 8086/8088 software. In protected

virtual address mode, the SAB 80286 is source code compatible with SAB 8086/8088 software and may require upgrading to use virtual addresses supported by SAB 80286's integrated memory management and protection mechanism. Both modes operate at full SAB 80286 performance and execute a superset of the SAB 8086/8088 instructions. The SAB 80286 provides special operations to support the efficient implementation and execution of operating systems. For example, one instruction can end execution of one task, save its state, switch to a new task, load its state, and start execution of the new task. The SAB 80286 also supports virtual memory systems by providing a segment-not-present exception and restartable instructions.

Pin Configuration





Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function						
BHĒ	1	0	the data bus byte of the o	D15-8. Ei lata bus v ons. BHE	ght-b would is act	it orie I norr tive lo	ansfer of data on the upper byte of ented devices assigned to the upper mally use BHE to condition chip ow and floats to tristate off		
					BHE	and A	A0 encodings		
			BHE value	A0 value	Func	tion			
			0 0 1 1	0 1 0 1	Byte Byte		nsfer fer on upper half of data bus (D15-8) fer on lower half of data bus (D7-0)		
\$1, \$0	4, 5	0	BUS CYCLE STATUS indicates initiation of a bus cycle with M/IO and COD/INTA, defines the type of bus cycles in a TS state whenever one or both are low, \$1 and active low and float to tristate off during bus hold ack						
			Bus cycle status definition						
			COD/INTA	M/ĪŌ	S1	Sō	Bus cycle initiated		
			0 (low) 0 0 0 0 0 1 (high) 1 1 1 1 1	0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 1 1 1 1	0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0	0 1 0 1 0 1 0 1	Interrupt acknowledge Reserved Rone; not a status cycle IF A1 = 1 then halt; else shutdown Memory data read Memory data write None; not a status cycle Reserved I/O read I/O write None; not a status cycle Reserved Memory instruction read Reserved None; not a status cycle		
PEREQ PEACK	6	0	PROCESSOR EXTENSION OPERAND REQUEST AND ACKNOW-LEDGE extend the memory management and protection capabilities of the SAB 80286 to processor extensions. The PEREC input requests the SAB 80286 to perform a data operand transfer for a processor extension. The PEACK output signals the processor extension when the requested operand is being transferred. PEREQ is active high and floats to tristate off during bus hold acknowledge. PEACK may be asynchronous to the system clock. PEACK is active low.						

Pin Definitions and Functions (cont'd)

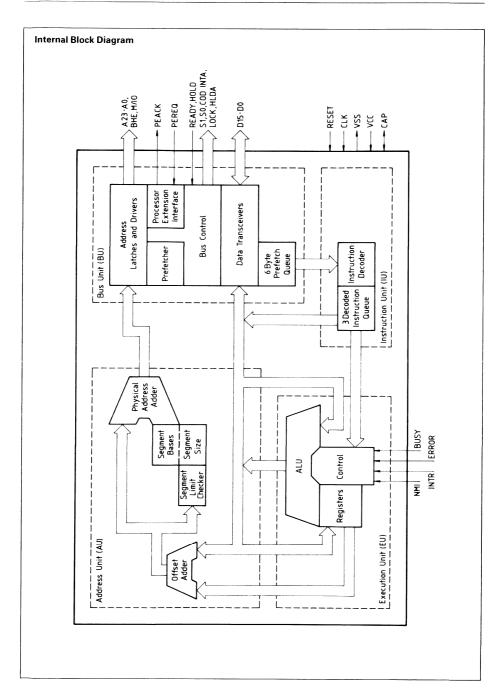
Symbol	Pin	Input (I) Output (O)	Function				
A23-A0	7 – 34	0	ADDRESS BUS outputs physical memory and I/O port addresses A0 is low when data is to be transferred on pins D7–0. A23–A10 are low during I/O transfers. The address bus is active high and floats to tristate off during bus hold acknowledge.				
RESET	29	I	active high. The S. low-to-high transi than 16 system clo	lears the internal logic of the SAB 80286 and is AB 80286 may be reinitialized at any time with a tion on RESET which remains active for more ock cycles. During RESET active, the output pins enter the state shown below:			
				Pin state during reset			
			Pin value	Pin names			
			1 (high) 0 (low) Tristate off	SO, S1, PEACK, A23–A0, BHE, LOCK M/IO, COD/INTA, HLDA D15 – D0			
			Operation of the SAB 80286 begins after a high-to-low transition on RESET. The high-to-low transition of RESET must be synchronous to the system clock. Approximately 50 system clock cycles are required by the SAB 80286 for internal initializations before performing the first bus cycle to fetch code from the power-on execution address. A low-to-high transition of RESET synchronous to the system clock will end a processor cycle at the second high-to-low transition of the system clock. The low-to-high transition of RESET may be asynchronous to the system clock; however, in this case i cannot be predetermined which phase of the processor clock will occur during the next system clock period. Synchronous low-to-high transitions of RESET are required only for systems where the processor clock must be phase-synchronous to another clock.				
CLK	31	I	systems. It is divid processor clock. T	provides the fundamental timing for SAB 80286 ed by two (inside the SAB 80286) to generate the he internal divide-by-two circuitry can be n external clock generator by a low-to-high IESET input.			
D15 - D0	36 – 51	0	ledge read cycles:	data during memory, I/O, and interrupt acknow- outputs data during memory and I/O write us is active high and floats to tristate off knowledge.			
BUSY ERROR	53, 54	1	PROCESSOR EXTENSION BUSY AND ERROR indicate the operating condition of a processor extension to the SAB 80286. An active BUSY input stops the SAB 80286 program execution on WAIT an some ESC instructions until BUSY becomes inactive (high). The SAB 80286 may be interrupted while waiting for BUSY to become inactive. An active ERROR input causes the SAB 80286 to perform processor extension interrupt when executing WAIT or some ESC instructions. These inputs are active low and may be asynchronous to the system clock.				

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
INTR	57		INTERRUPT REQUEST requests the SAB 80286 to suspend its current program execution and service a pending external request. Interrupt requests are masked whenever the interrupt enable bit in the flag word is cleared. When the SAB 80286 responds to an interrupt request, it performs two interrupt acknowledge bus cycles to read an 8-bit interrupt vector that identifies the source of the interrupt. To assure program interruption, INTR must remain active until the first interrupt acknowledge cycle is completed. INTR is sampled at the beginning of each processor cycle and must be active high at least two processor cycles before the current instruction ends in order to interrupt before the next instruction. INTR is level sensitive, active high, and may be asynchronous to the system clock.
NMI	59	I	NON-MASKABLE INTERRUPT REQUEST interrupts the SAB 80286 with an internally supplied vector value of 2. No interrupt acknowledge cycles are performed. The interrupt enable bit in the SAB 80286 flag word does not affect this input. The NMI input is active high, may be asynchronous to the system clock, and is edge-triggered after internal synchronization. For proper recognition, the input must have been previously low for at least four system clock cycles and remain high for at least four system clock cycles.
READY	63		BUS READY terminates a bus cycle. Bus cycles are extended without limit until terminated by READY low. READY is an active low synchronous input requiring setup and hold times relative to the system clock be met for correct operation. READY is ignored during bus hold acknowledge.
HOLD HLDA	64 65	0	BUS HOLD REQUEST AND HOLD ACKNOWLEDGE control ownership of the SAB 80286 local bus. The HOLD input allows another local bus master to request control of the local bus. When control is granted, the SAB 80286 will float its bus drivers to tristate off and then activate HLDA, thus entering the bus hold acknowledge condition. The local bus will remain granted to the requesting master until HOLD becomes inactive which results in the SAB 80286 deactivating HLDA and regaining control of the local bus. This terminates the bus hold acknowledge condition, HOLD may be asynchronous to the system clock. These signals are active high.
COD/INTA	66	0	CODE / INTERRUPT ACKNOWLEDGE distinguishes instruction fetch cycles from memory data read cycles. Also distinguishes interrupt acknowledge cycles from I/O cycles. COD/INTA floats to tristate off during bus hold acknowledge.
M/ĪŌ	67	0	MEMORY / I/O SELECT distinguishes memory access from I/O access. If high during TS, a memory cycle or a halt/shutdown cycle is in progress. If low, an I/O cycle or an interrupt acknowledge cycle is in progress M/IO floats to tristate off during bus hold acknowledge.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
LOCK	68	0	BUS LOCK indicates that other system bus masters are not to gain control of the system bus following the current bus cycle. The LOCK signal may be activated explicitly by the "LOCK" instruction prefix or automatically by SAB 80286 hardware during memory XCHG instructions, interrupt acknowledge, or descriptor table access. LOCK is active low and floats to tristate off during bus hold acknowledge.
VCC	30, 62	_	POWER SUPPLY (+5V)
VSS	9, 35, 60	_	GROUND (0 V)
CAP	52	1	SUBSTRATE FILTER CAPACITOR: a 0.047 µF ±20% 12 V capacitor must be connected between this pin and ground. This capacitor filters the output of the internal substrate bias generator. A maximum DC leakage current of 1 µA is allowed through the capacitor. For correct operation of the SAB 80286 the substrate bias generator must charge this capacitor to its operating voltage. The capacitor's charging time is 5 milliseconds (max.) after VCC and CLK reach their specified AC and DC parameters. RESET may be applied to prevent spurious activity by the CPU during this time. After this time, the SAB 80286 processor clock can be phase-synchronized to another clock by pulsing RESET low synchronous to the system clock.



Functional Description

Introduction

The SAB 80286 is an advanced, high-performance microprocessor with specially optimized capabilities for multiple user and multitasking systems. Depending on the application, the SAB 80286's performance is up to six times faster than that of the standard 5 MHz SAB 8086, while providing complete upward software compatibility with the Siemens 16-bit CPU family (SAB 8086/88, SAB 80186/88).

The SAB 80286 operates in two modes: real address mode (8086 mode) and protected virtual address mode. Both modes execute a superset of the SAB 8086/88 instruction set. In real address mode programs use real addresses with up to one megabyte of address space. Programs use virtual addresses in protected virtual address mode, also called protected mode. In protected mode, the SAB 80286 CPU automatically maps 1 gigabyte of virtual addresses per task into a 16 megabyte real address space. This mode also provides memory protection to isolate the operating system and ensure privacy of each task's programs and data. Both modes provide the same basic instruction set, registers, and addressing modes.

The following functional description describes first the basic SAB 80286 architecture common to both modes, second the real address mode, and third the protected mode.

Basic Architecture

The processors of the Intel/Siemens 16-bit CPU family all contain the same basic set of registers,

instructions, and addressing modes. Therefore, the SAB 80286 processor is upward-compatible with the SAB 8086, 8088 and 80186 CPUs.

Register Set

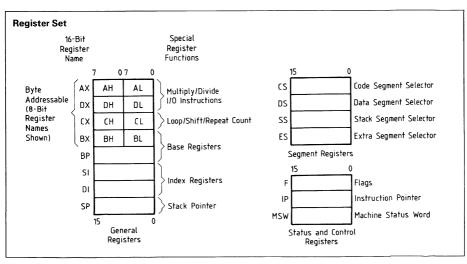
The SAB 80286 basic architecture has fifteen registers as shown below. These registers are grouped into the following four categories:

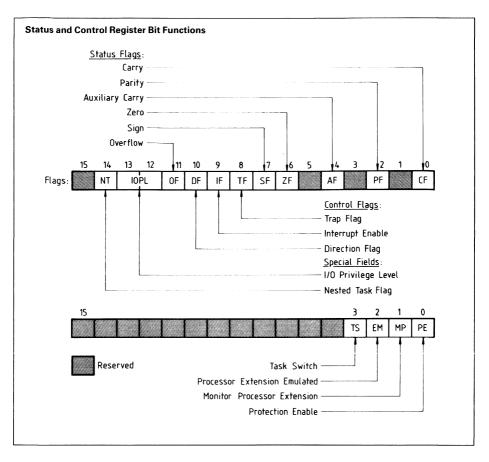
General registers: Eight 16-bit general purpose registers used to contain arithmetic and logical operands. Four of these (AX, BX, CX, and DX) can be used either in their entirety as 16-bit words or split into pairs of separate 8-bit registers.

Segment registers: Four 16-bit special purpose registers select, at any given time, the segments of memory that are immediately addressable for code, stack, and data (For usage, refer to Memory Organization).

Base and index registers: Four of the general purpose registers may also be used to determine offset addresses of operands in memory. These registers may contain base addresses or indexes to particular locations within a segment. The addressing mode determines the specific registers used for operand address calculations.

Status and control registers: The three 16-bit special purpose registers in the figure below record or control certain aspects of the SAB 80286 processor state including the instruction pointer which contains the offset address of the next sequential instruction to be executed.





Flags Word Description

The flags word (flags) records specific characteristics of the result of logical and arithmetic instructions (bits 0, 2, 4, 7, and 11) and controls the operation of the SAB 80286 within a given operating mode (bits 8 and 9). Flags is a 16-bit register. The function of the flag bits is given in table 1.

Instruction Set

The instruction set is divided into seven categories: data transfer, arithmetic, shift/rotate/logical, string manipulation, control transfer, high level instructions, and processor control.

An SAB 80286 instruction can reference zero, one, or two operands; where an operand resides in a register, in the instruction itself, or in memory. Zero-operand instructions (e.g. HLT) are usually

one byte long. One-operand instructions (e.g. INC and DEC) are usually two bytes long but some are encoded in only one byte. One-operand instructions may reference a register or memory location.

Two-operand instructions permit the following six types of instruction operations:

- register to register
- memory to register
- immediate data to register
- memory to memory
- register to memory
- immediate data to memory

Two-operand instructions (e.g. MOV and ADD) are usually three to six bytes long. Memory-to-memory operations are provided by a special class of string instructions requiring one to three bytes. For detailed instruction formats and encodings refer to the instruction set summary.

Table 1 Flags Word Bit Functions

Bit position	Name	Functions
0	CF	Carry Flag – Set on high-order bit carry or borrow; cleared otherwise
2	PF	Parity Flag – Set if low-order 8 bits of result contain an even number of 1-bits; cleared otherwise
4	AF	Set on carry from or borrow to the low-order 4 bits of AL; cleared otherwise
6	ZF	Zero Flag – Set if result is zero; cleared otherwise
7	SF	Sign Flag – Set equal to high-order bit of result (0 if positive, 1 if negative)
11	OF	Overflow Flag – Set if result is a positive number too large or a negative number too small (excluding sign bit) to fit in destination operand; cleared otherwise
8	TF	Single Step Flag – Once set, a single step interrupt occurs after the next instruction has been executed. TF is cleared by the single step interrupt
9	IF	Interrupt Enable Flag – When set, maskable interrupts will cause the CPU to transfer control to an interrupt vector specified location
10	DF	Direction Flag – Causes string instructions to autodecrement the appropriate index registers when set. Clearing DF causes autoincrement

Memory Organization

Memory is organized as sets of variable length segments. Each segment is a linear contiguous sequence of up to 64 K (2¹⁶) 8-bit bytes. Memory is addressed using a two-component address

(a pointer) that consists of a 16-bit segment selector, and a 16-bit offset. The segment selector indicates the desired segment in memory. The offset component indicates the desired byte address within the segment.

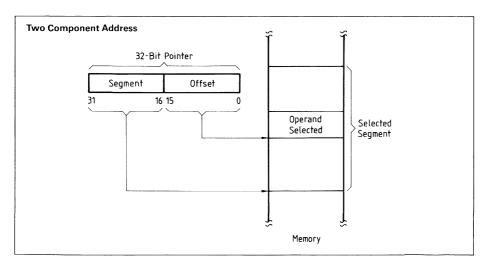


Table 2
Segment Register Selection Rules

Memory reference needed	Segment register used	Implicit segment selection rule
Instructions	Code (CS)	Automatic with instruction prefetch
Stack	Stack (SS)	All stack pushes and pops. Any memory reference which uses BP as a base register
Local data	Data (DS)	All data references except when relative to stack or string destination
Externed (global) data	Extra (ES)	Alternate data segment and destination of string operation

All instructions that address operands in memory must specify the segment and the offset. For speed and compact instruction encoding, segment selectors are usually stored in the high-speed segment registers. An instruction need specify only the desired segment register and an offset in order to address a memory operand.

Most instructions need not explicitly specify which segment register is used. The correct segment register is automatically chosen according to the rules of table 2.

These rules follow the way programs are written as independent modules that require areas for code and data, a stack, and access to external data areas. Special segment override instruction prefixes allow the implicit segment register selection rules to be overridden for special cases. The stack, data, and extra segments may coincide for simple programs. To access operands not residing in one of the four immediately available segments, a full 32-bit pointer or a new segment selector must be loaded.

Addressing Modes

The SAB 80286 provides a total of eight adressing modes for instructions to specify operands. Two addressing modes are provided for instructions that operate on register or immediate operands:

Register operand mode: The operand is located in one of the 8 or 16-bit general registers.

Immediate operand mode: The operand is included in the instruction.

Direct mode: The operand's offset is contained in the instruction as an 8 or 16-bit displacement element.

Register indirect mode: The operand's offset is in one of the registers SI, DI, BX, or BP.

Based mode: The operand's offset is the sum of an 8 or 16-bit displacement and the contents of a base register (BX or BP).

Indexed mode: The operand's offset is the sum of an 8 or 16-bit displacement and the contents of an index register (SI or DI).

Based indexed mode: The operand's offset is the sum of the contents of a base register and an index register.

Based indexed mode with displacement: The operand's offset is the sum of a base register's contents, an index register's contents, and an 8 or 16-bit displacement.

Data Types

The SAB 80286 directly supports the following data types:

Integer:

A signed binary numeric value contained in an 8-bit byte or a 16-bit word. All operations assume a 2's complement representation. Signed 32 and 64-bit integers are supported using the numeric data processor extension.

Ordinal:

An unsigned binary numeric value contained in an 8-bit byte or 16-bit word.

Pointer:

A 32-bit quantity, composed of a segment selector component and an offset component. Each component is a 16-bit word.

String:

A contiguous sequence of bytes or words. A string may contain between 1 byte and 64 Kbytes.

ASCII:

A byte representation of alphanumeric and control characters using the ASCII standard of character representation.

BCD:

A byte (unpacked) representation of the decimal digits 0 to 9.

Packed BCD:

A byte (packed) representation of two decimal digits 0 to 9 storing one digit in each nibble of the byte.

Floating Point:

A signed 32, 64, or 80-bit real number representation (Floating point operands are supported using the extended processor configuration with SAB 80287).

Table 3 Interrupt Vector Assignments

I/O Space

The I/O space consists of 64 K 8-bit or 32 K 16-bit ports. I/O instructions address the I/O space with either an 8-bit port address, specified in the instruction, or a 16-bit port address in the DX register, 8-bit port addresses are zero extended such that A15-A8 are low. I/O port addresses 00F8(H) through 00FF(H) are reserved.

Function	Interrupt Number	Related instructions	Return address before instruction causing exception?
Divide error exception	0	DIV, IDIV	Yes
Single step interrupt	1	All	-
NMI interrupt	2	All	_
Breakpoint interrupt	3	INT	_
INTO detected overflow exception	4	INT0	No
BOUND range exceeded exception	5	BOUND	Yes
Invalid op code exception	6	any undefined op code	Yes
Processor extension not available exception	7	ESC or WAIT	Yes
Reserved	8-15		_
Processor extension error interrupt	16	ESC or WAIT	_
Reserved	17-31		_
User defined	32-255		_

Interrupts

An interrupt transfers execution to a new program location. The old program address (CS:IP) and machine state (flags) are saved on the stack to allow resumption of the interrupted program. Interrupts fall into three classes: hardware initiated, INT instructions, and instruction exceptions. Hardwareinitiated interrupts occur in response to an external input and are classified as non-maskable or maskable. Programs may cause an interrupt with an INT instruction. Instruction exceptions occur when an unusual condition, which prevents further instruction processing, is detected while attempting to execute an instruction. The return address from an exception will always point at the instruction causing the exception and include any leading instruction prefixes.

A table containing up to 256 pointers defines the proper interrupt service routine for each interrupt. Interrupts 0 to 31, some of which are used for instruction exceptions, are reserved. For each inter-

rupt, an 8-bit vector must be supplied to the SAB 80286 which identifies the appropriate table entry. Exceptions supply the interrupt vector internally. INT instructions contain or imply the vector and allow access to all 256 interrupts. Maskable hardware initiated interrupts supply the 8-bit vector to the CPU during an interrupt acknowledge bus sequence. Non-maskable hardware interrupts use a predefined internally supplied vector.

Single Step Interrupt

The SAB 80286 has an internal interrupt that allows programs to execute one instruction at a time. It is called the single step interrupt and is controlled by the single step flag bit (TF) in the flag word. Once this bit is set, an internal single step interrupt will occur after the next instruction has been executed. The interrupt clears the TF bit and uses an internally supplied vector of 1. The IRET instruction is used to set the TF bit and transfer control to the next instruction to be single-stepped.

Interrupt Priorities

When simultaneous interrupt requests occur, they are processed in a fixed order as shown in table 4. Interrupt processing involves saving the flags, return address, and setting CS:IP to point at the first instruction of the interrupt handler. If other inter-

rupts remain enabled they are processed before the first instruction of the current interrupt handler is executed. The last interrupt processed is therefore the first one serviced.

Table 4
Interrupt Processing Order

Order	Interrupt
1	Instruction exception
2	Single step
3	NMI
4	Processor extension segment overrun
5	INTR
6	INT instruction

Initialization and Processor Reset

Processor initialization or start up is accomplished by driving the RESET input pin high. RESET forces the SAB 80286 to terminate all execution and local bus activity. No instruction or bus activity will occur as long as RESET is active. After RESET became inactive and an internal processing interval has elapsed, the SAB 80286 begins execution in real address mode with the instruction at physical location FFFFF0(H). RESET also sets some registers to predefined values as shown in table 5. A23 to A20 will be high when the SAB 80286 performs memory references relative to the CS register until CS is changed. A23 to A20 will be zero for references to the DS, ES, or SS segments. Changing CS in real address mode will force A23 to A20 low whenever CS is used again. The initial CS:IP value of F000:FFF0 provides 64 Kbytes of code space for initialization code without changing CS.

Table 5
SAB 80286 Initial Register State after RESET

Flag word	0002(H)
Machine status word	FFF0(H)
Instruction pointer	FFF0(H)
Code segment	F000(H)
Data segment	0000(H)
Extra segment	0000(H)
Stack segment	0000(H)
· ·	

Machine Status Word Description

The machine status word (MSW) records when a task switch takes place and controls the operating mode of the SAB 80286. It is a 16-bit register of which the lower four bits are used. One bit places the CPU into protected mode, while the other three bits, as shown in table 6, control the processor extension interface. After RESET, this register contains FFF0(H) which places the SAB 80286 in real address mode.

SAB 80286

Table 6
MSW Bit Functions

Bit position	Name	Function
0	PE	Protected mode enable places the SAB 80286 into protected mode and cannot be cleared except by RESET
1	MP	M onitor p rocessor extension allows WAIT instructions to cause a processor extension not present exception (number 7)
2	EM	Emulate processor extension causes a processor extension not present exception (number 7) on ESC instructions to allow emulating a processor extension
3	TS	Task switched indicates that the next instruction using a processor extension will cause exception 7, allowing software to test whether the current processor extension context belongs to the current task

The LMSW and SMSW instructions can load and store the MSW in real address mode. The

recommended use of TS, EM, and MP is shown in table 7.

Table 7
Recommended MSW Encodings For Processor Extension Control

TS	MP	EM	Recommended use	Instructions causing exception 7
0	0	0	Initial encoding after RESET. SAB 20286 operation is identical with SAB 8086/88 operation	none
0	0	1	No processor extension is available. Software will emulate its function	ESC
1	0	1	No processor extension is available. Software will emulate its function. The current processor extension context may belong to another task	ESC
0	1	0	A processor extension exists	none
1	1	0	A processor extension exists. The current processor extension context may belong to another task. The exception on WAIT allows software to test for an error pending from a previous processor extension operation	ESC or WAIT

Halt

The HLT instruction stops program execution and prevents the CPU from using the local bus until restarted. Either NMI, INTR with IF = 1, or RESET

will force the SAB 80286 out of halt. If interrupted the saved CS:IP will point to the next instruction after the HLT.

Real Address Mode

The SAB 80286 executes a fully upward-compatible superset of the SAB 8086's instruction set in real address mode. In real address mode, the SAB 80286 is object code compatible with SAB 8086 and SAB 8088 software. The real address mode architecture (registers and addressing modes) is exactly as described in the SAB 80286 basic architecture section of this functional description.

Memory Size

Physical memory is a contiguous array of up to 1,048,576 bytes (one megabyte) addressed by pins A0 through A19 and BHE. A20 through A23 may be ignored.

Memory Addressing

In real address mode the processor generates 20-bit physical addresses directly from a 20-bit-segment base address and a 16-bit offset.

The selector portion of a pointer is interpreted as the upper 16 bits of a 20-bit segment address. The lower four bits of the 20-bit segment addresses are always zero. Segment addresses, therefore, begin on multiples of 16 bytes. See figure on address calculation for a graphic representation of address formation.

All segments in real address mode are 64 Kbytes in size and may be read, written, or executed. An exception or interrupt can occur if data operands or instructions attempt to wrap around the end of a segment (e.g. a word with its low-order byte at offset FFFF(H) and its high-order byte at offset 0000(H). If, in real address mode, the information contained in a segment does not use the full 64 Kbytes, the unused end of the segment may be overlayed by another segment to reduce physical memory requirements.

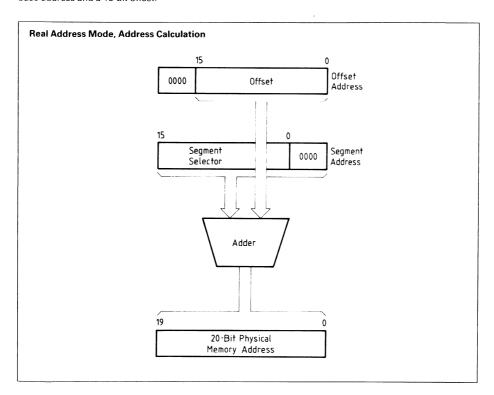


Table 8
Real Address Mode, Addressing Interrupts

Function	Interrupt number	Related instructions	Return address before instruction?
Interrupt table limit too small exception	8	INT vector is not within table limit	Yes
Processor extension segment overrun interrupt	9	ESC with memory operand extending beyond offset FFFF(H)	No
Segment overrun exception	13	Word memory reference with offset = FFFF(H) or an attempt to execute past the end of a segment	Yes

Interrupts

Table 8 shows the interrupt vectors reserved for exceptions and interrupts which indicate an addressing error. The exceptions leave the CPU in the state existing before attempting to execute the failing instruction (except for PUSH, POP, PUSHA, or POPA).

Shutdown

Shutdown occurs when a severe error is detected that prevents further instruction processing by the CPU. Shutdown and halt are externally signalled via a halt bus operation. They can be distinguished by A1 high for halt and A1 low for shutdown. In real address mode, shutdown can occur under two conditions:

- Exceptions 8 or 13 happen and the IDT limit does not include the interrupt vector.
- A CALL, INT or POP instruction attempts to wrap around the stack segment when SP is not even.

An NMI input can bring the CPU out of shutdown if the IDT limit is at least 000F(H) and SP is greater than 0005(H), otherwise shutdown can only be exited via the RESET input.

Protected Virtual Address Mode

The SAB 80286 executes a fully upward-compatible superset of the SAB 8086 instruction set in protected virtual address mode (protected mode). Protected mode also provides memory management and protection mechanisms and associated instructions.

The SAB 80286 enters protected virtual address mode from real address mode by setting the PE (Protection Enable) bit of the machine status word with the Load Machine Status Word (LMSW) instruction. Protected mode offers extended physical and virtual memory address space, memory protection mechanisms, and new operations to support operating system and virtual memory.

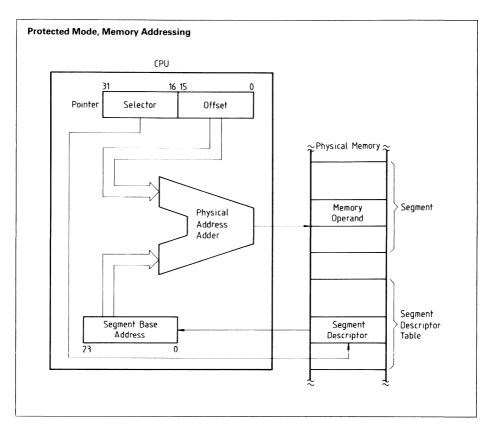
All registers, instructions and addressing modes described in the SAB 80286 basic architecture section of the functional description remain the same. Programs for the SAB 8086, SAB 8088, SAB 80186 and real address mode SAB 80286 can be run in protected mode: however, embedded constants for segment selectors are different.

Memory Size

The protected mode SAB 80286 provides a 1 gigabyte virtual address space per task mapped into a 16 megabyte physical address space defined by the address pins A23—A0 and BHE. The virtual address space may be larger than the physical address space since any use of an address that does not map to a physical memory location will cause a restartable exception.

Memory Addressing

As in real address mode, protected mode uses 32-bit pointers, consisting of 16-bit selector and offset components. The selector, however, specifies an index into a memory resident table rather than the upper 16-bits of a real memory address. The 24-bit base address of the desired segment is obtained from the tables in memory. The 16-bit offset is added to the segment base address to form the physical address as shown in the figure below. The tables are automatically referenced by the CPU whenever a segment register is loaded with a selector. All SAB 80286 instructions which load a segment register will reference the memory-based tables without additional software. The memory-based tables contain 8 byte values called descriptors.

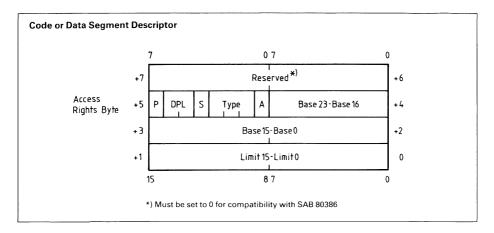


Descriptors

Descriptors define the use of memory. Special types of descriptors also define new functions for transfer of control and task switching. The SAB 80286 has segment descriptors for code, stack and data segments, as well as system control descriptors for special system data segments and control transfer operations. Descriptor accesses are performed as locked bus operations to assure descriptor integrity in multiprocessor systems.

Code and data segment descriptors (S = 1)

Besides segment base addresses, code and data descriptors contain other segment attributes including segment size (1 to 64 Kbytes), access rights (read only, read/write, execute only, and execute/read), and presence in memory (for virtual memory systems; figure and table next page). Any segment usage violating a segment attribute indicated by the segment descriptor will prevent the memory cycle and cause an exception or interrupt.



Access Rights Byte Definition

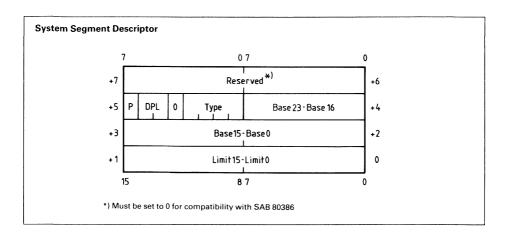
Bit Position	Name		Function	
7	Present (P)	P = 1 P = 0	Segment is mapped into physical memory No mapping to physical memory exists, base and used	limit are not
6-5	Descriptor privilege level (DPL)		Segment privilege attribute used in privilege tests	
4	Segment descriptor (S)	S = 1 S = 0	Code or data (includes stacks) segment descriptor System segment descriptor or gate descriptor	
Type field definition 2 2 1 2 2	Executable (E) Expansion direction (ED) Writeable (W)	E = 0 ED = 0 ED = 1 W = 0 W = 1	Data segment descriptor type is: Expand up segment, offsets must be ≤ limit Expand down segment, offsets must be > limit Data segment may not be written into Data segment may be written into	If data segment (S = 1, E = 0)
Type field	Executable (E) Conforming (C) Readable (R)	E = 1 C = 1 R = 0 R = 1	Code segment descriptor type is: Code segment may only be executed when CPL ≥ DPL and CPL remains unchanged Code segment may not be read Code segment may be read	If code segment (S = 1, E = 1)
0	Accessed (A)	A = 0 A = 1	Segment has not be accessed Segment selector has been loaded into segment re used by selector test instructions	egister or

Code and data (including stack data) are stored in two types of segments: code segments and data segments. Both types are identified and defined by segment descriptors (S=1). Code segments are identified by the executable (E) bit set to 1 in the descriptor access rights byte, whereas the data segments have the E bit set to 0.

System segment descriptors (S = 0, type = 1-3)

In addition to code and data segment descriptors, the protected mode SAB 80286 defines system segment descriptors. These descriptors define special system data segments which contain a table of descriptors (local descriptor table descriptor) or segments which contain the execution state of a task (task state segment descriptor).

The figure and table on next page show the formats for the special system data segment descriptors.



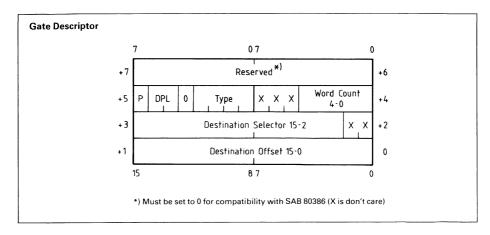
System Segment Descriptor Fields

Name	Value	Description
TYPE	1 2 3	Available task state segment Local descriptor table descriptor Busy task state segment
Р	0	Descriptor contents are not valid Descriptor contents are valid
DPL	0-3	Descriptor privilege level
BASE	24-bit number	Base address of special system data segment in real memory
LIMIT	16-bit number	Offset of last byte in segment

Gate descriptors (S = 0, Type = 4-7)

Gates are used to control access to entry points within the target code segment. The gate descriptors are **call** gates, **task** gates, **interrupt** gates and **trap** gates. Gates provide a level of indirection between the source and destination of the control transfer. This indirection allows the CPU to automatically perform protection checks and control entry point of the destination. Call gates are used to change privilege levels (see privilege), task gates are used to perform a task switch, and interrupt and trap gates are used to specify interrupt service routines. The interrupt gate disables interrupts (resets IF) while the trap gate does not.

The figure and table on the next page show the format of the gate descriptors. The descriptor contains a destination pointer that points to the descriptor of the target segment and the entry point offset. The destination selector in an interrupt gate, trap gate, and call gate must refer to a code segment descriptor. Exception 13 is generated when the gate is used if a destination selector does not refer to the correct descriptor type.



Gate Descriptor Fields

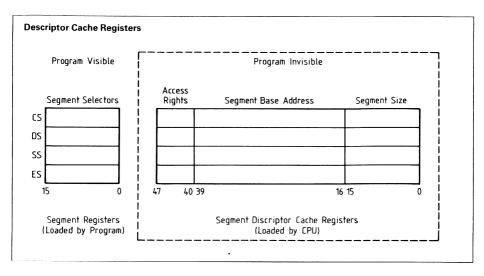
Name	Value	Description	
TYPE	4 5 6 7	 Call gate Task gate Interrupt gate Trap gate 	
Р	0	Descriptor contents are not valid Descriptor contents are valid	
DPL	0-3	Descriptor Privilege level	
WORD COUNT	0-31	Number of words to copy from callers stack to called procedures stack. Only used with call gate	
DESTINATION SELECTOR	16-bit selector	Selector to the target code segment (call, interrupt or trap gate)	
DESTINATION OFFSET	16-bit offset	Entry point within the target code segment	

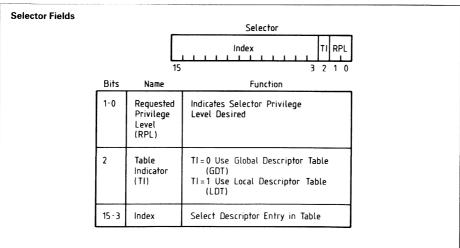
Segment descriptor cache registers

A segment descriptor cache register is assigned to each of the four segment registers (CS, SS, DS, ES). Segment descriptors are automatically loaded (cached) into a segment descriptor cache register (see figure) whenever the associated segment register is loaded with a selector. Only segment descriptors may be loaded into segment descriptor cache registers. Once loaded, all references to that segment of memory use the cached descriptor information instead of reaccessing memory. The descriptor cache registers are not visible to programs. No instructions exist to store their contents. They only change when a segment register is loaded.

Selector fields

A protected mode selector has three fields: descriptor entry index, local or global descriptor table indicator (TI), and selector privilege (RPL) as shown in the figure on selector fields. These fields select one of two memory-based tables of descriptors, select the appropriate table entry and allow highspeed testing of the selector's privilege attribute (refer to privilege discussion below).

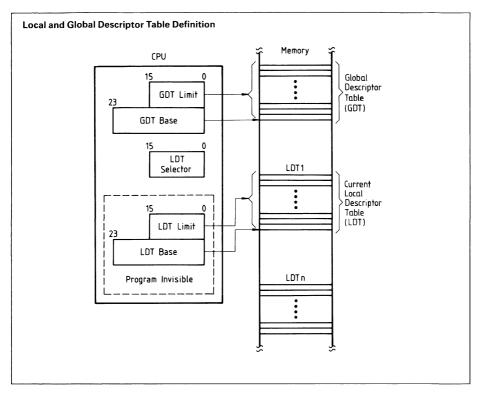


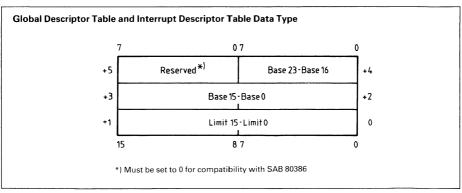


Local and global descriptor tables (LDT, GDT)

Two tables of descriptors, called descriptor tables, contain all descriptors accessible by a task at any given time. A descriptor table is a linear array of up to 8192 descriptors. The upper 13 bits of the selector value are an index into a descriptor table. Each table has a 24-bit base register to locate the

descriptor table in physical memory and a 16-bit limit register that confine descriptor access to the defined limits of the table as shown in the figure below. A restartable exception (13) will occur if an attempt is made to reference a descriptor outside the table limits.

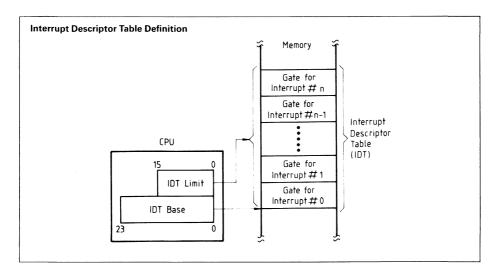




Interrupt descriptor table

The protected mode SAB 80286 has a third descriptor table, called the interrupt descriptor table (DT) (see top figure on next page), used to define up to 256 interrupts. It may contain only task gates, interrupt gates and trap gates. The IDT

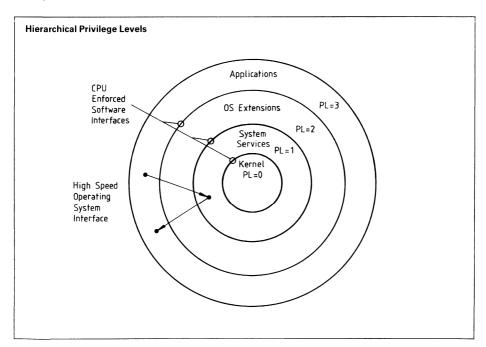
(interrupt descriptor table) has a 24-bit base and 16-bit limit register in the CPU. References to IDT entries are made via INT instructions, external interrupt vectors, or exceptions. The IDT must be at least 256 bytes in size to allocate space for all reserved interrupts.



Privilege

The SAB 80286 has a four-level hierarchical privilege system which controls the use of privileged instructions and access to descriptors

(and their associated segments) within a task (figure below). The privilege levels are numbered 0 through 3. Level 0 is the most privileged level.



Protection

The SAB 80286 includes mechanisms to protect critical instructions that affect the CPU execution state (e.g. HLT) and code or data segments from improper usage. These mechanisms are grouped under the term "protection" and have three forms:

Restricted usage of segments (e.g. no write allowed to read-only data segments). The only segments available for use are defined by descriptors in the local descriptor table (LDT) and global descriptor table (GDT).

Restricted access to segments via the rules of privilege and descriptor usage.

Privileged instructions or operations that may only be executed at certain privilege levels as determined by the CPL and I/O privilege level (IOPL). The IOPL is defined by bits 14 and 13 of the flag word.

These checks are performed for all instructions and can be split into three categories: segment load checks (table 9), operand reference checks (table 10), and privileged instruction checks (table 11). Any violation of the rules shown will result in an exception. A not-present exception related to the stack segment causes exception 12.

The IRET and POPF instructions do not perform some of their defined functions if CPL is not of sufficient privilege (numerically small enough). No exceptions or other indication are given when these conditions occur.

The IF bit is not changed if CPL > IOPL. The IOPL field of the flag word is not changed if CPL > 0.

Table 9
Segment Register Load Checks

Error description	Exception number
Descriptor table limit exceeded	13
Segment descriptor not present	11 or 12
Privilege rules violated	13
Invalid descriptor/segment type segment register load: - read only data segment load to SS - special control descriptor load to DS, ES, SS - execute only segment load to DS, ES, SS - data segment load to CS - read/execute code segment load to SS	13

Table 10 Operand Reference Checks

Error description	Exception number
Write into code segment Read from execute-only code	13
segment	13
Write to read-only data segment	13
Segment limit exceeded 1)	12 or 13

¹⁾ Carry out in offset calculations is ignored.

Table 11 Privileged Instruction Checks

Error description	Exception number
CPL > 0 when executing the following instructions LIDT, LLDT, LGDT, LTR, LMSW, CTS, HLT	13
CPL > IOPL when executing the following instructions INS, IN, OUTS, OUT, STI, CLI, LOCK	13

Exceptions

The SAB 80286 detects several types of exceptions and interrupts in protected mode (see table 12). Most of them are restartable after the exceptional condition is removed. Interrupt handlers for most exceptions receive an error code, pushed on the stack after the return address, that identifies the selector involved (0 if none). The return address normally points to the failing instruction, including all leading prefixes. For a processor extension segment overrun exception, the return address will not point at the ESC instruction that caused the exception; however, the processor extension registers may contain the address of the failing instruction.

Table 12 Protected Mode Exceptions

Interrupt vector	Function	Return address at failing instruction?	Always restart- able?	Error code on stack?
8	Double exception detected	yes	no	yes
9	Processor extension segment overrun	no	no	no
10	Invalid task state segment	yes	yes	yes
11	Segment not present	yes	yes	yes
12	Stack segment overrun or segment not present	yes	yes1)	yes
13	General protection	yes	no	yes

¹⁾ When a PUSHA instruction attempts to wrap around the stack segment, the machine state after the exception will not be restartable. This condition is identified by the value of the saved SP being either 0000(H), 0001(H), FFFE(H), or FFFF(H).

Special Operations

Task switch operation

The SAB 80286 provides a built-in task switch operation which saves the entire SAB 80286 execution state (registers, address space, and a link to the previous task), loads a new execution state, and commences execution in the new task. Like gates, the task switch operation is invoked by executing an inter-segment JMP or CALL instruction which refers to a task state segment (TSS) or task gate descriptor in the GDT or LDT. An INT instruction, exception, or external interrupt may also invoke the task switch operation by selecting a task gate descriptor in the associated IDT descriptor entry.

The TSS descriptor points at a segment (see figure on next page) containing the entire SAB 80286 execution state while a task gate descriptor contains a TSS selector. The limit field must be > 002B(H).

The task state segment is marked busy by changing the descriptor type field from type 1 to type 3. Use of a selector that references a busy task state segment causes exception 13.

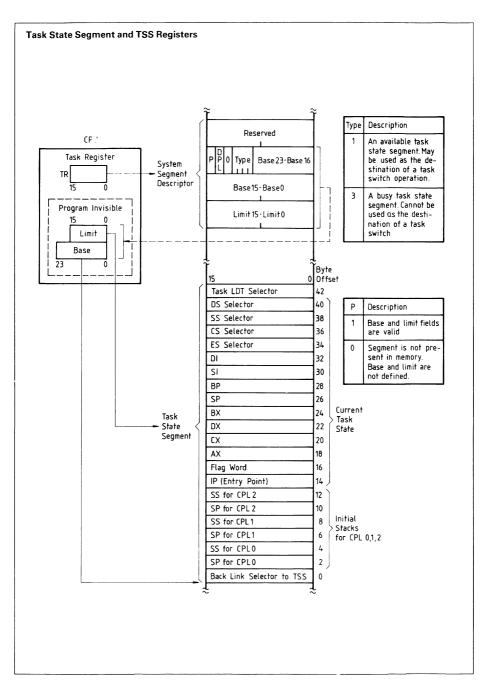
Processor extension context switching

The context of a processor extension (such as the SAB 80287 numerics processor) is not changed by the task switch operation. A processor extension context need only be changed when a different task attempts to use the processor extension (which still contains the context of a previous task).

Whenever the SAB 80286 switches tasks, it sets the task switched (TS) bit of the MSW. TS indicates that a processor extension context may belong to a different task than the current one. The processor extension not present exception (7) will occur when attempting to execute an ESC or WAIT instruction if TS = 1 and a processor extension is present (MP = 1 in MSW).

Double fault and shutdown

If two seperate exceptions are detected during a single instruction execution, the SAB 80286 performs the double fault exception (8). If an exception occurs during processing of the double fault exception, the SAB 80286 will enter shutdown. During shutdown no further instructions or exceptions are processed. Either NMI (CPU remains in protected mode) or RESET (CPU exits protected mode) can force the SAB 80286 out of shutdown. Shutdown is externally signalled via a HALT bus operation with A1 high.



System Interface

The SAB 80286 system interface appears in two forms: a local bus and a system bus. The local bus consists of address, data, status, and control signals at the pins of the CPU. A system bus is any buffered version of the local bus. A system bus may also differ from the local bus in terms of coding of status and control lines and/or timing and loading of signals. The SAB 80286 family includes several devices to generate standard system buses such as the IEEE 796 standard Multibus⁶³.

Bus Interface Signals and Timing

The SAB 80286 local bus interfaces the SAB 80286 to local memory and I/O components. The interface has 24 address lines, 16 data lines, and 8 status and control signals.

The SAB 80286 CPU, SAB 82284 clock generator, SAB 82288 bus controller, SAB 82289 bus arbiter, SAB 8286A/8287A transceivers, and SAB 8282A/8283A latches provide a buffered and decoded system bus interface. The SAB 82284 generates the system clock and synchronizes READY and RESET. The SAB 82288 converts bus operation status encoded by the SAB 80286 into command and bus control signals.

The SAB 82289 bus arbiter generates Multibus bus arbitration signals. These components can provide the timing and electrical power drive levels required for most system bus interfaces including the Multibus.

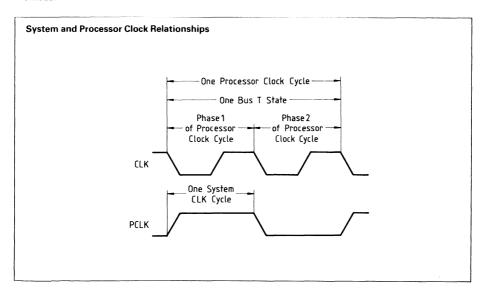
Physical Memory and I/O Interface

A maximum of 16 megabytes of physical memory can be addressed in protected mode. One megabyte can be addressed in real address mode. Memory is accessible as bytes or words. Words consist of any two consecutive bytes addressed with the least significant byte stored in the lowest address.

The I/O address space contains 64 K addresses in both modes. The I/O space is accessible as either bytes or words, as is memory. Byte-wide peripheral devices may be attached to either the upper or lower byte of the data bus. An interrupt controller such as the SAB 8259A must be connected to the lower byte of the data bus (D7-D0) for proper return of the interrupt vector.

Bus Operation

The SAB 80286 uses a double frequency system clock (CLK input) to control bus timing. All signals on the local bus are measured relative to the system CLK input. The CPU divides the system clock by 2 to produce the internal processor clock, which determines bus state. Each processor clock is composed of two system clock cycles named phase 1 and phase 2. The SAB 82284 clock generator output (PCLK) identifies the next phase of the processor clock (see figure on system and processor clock relationship).



Six types of bus operations are supported: memory read, memory write, I/O read, I/O write, interrupt acknowledge, and halt/shutdown. Data can be transferred at a maximum rate of one word per two processor clock cycles.

The SAB 80286 bus has three basic states: idle (TI), send status (TS), and perform command (TC). The SAB 80286 CPU also has a fourth local bus state called hold (TH). TH indicates that the SAB 80286 has surrendered control of the local bus to another bus master in response to a HOLD request.

Each bus state is one processor clock long. The figure below shows the four SAB 80286 local bus states and allowed transitions.

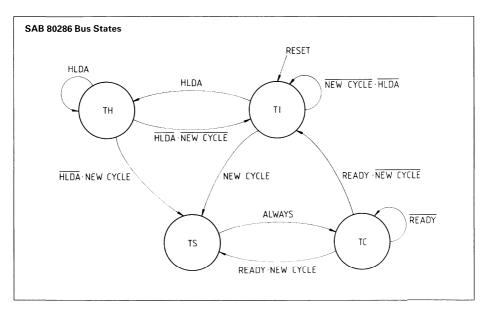
Pipelined Addressing

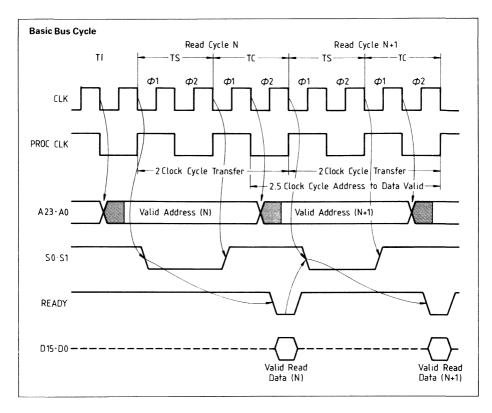
The SAB 80286 uses a local bus interface with pipelined timing to allow as much time as possible for data access. Pipelined timing allows bus operations to be performed in two processor cycles,

while allowing each individual bus operation to last for three processor cycles.

The timing of the address outputs is pipelined such that the address of the next bus operation becomes available during the current bus operation. Or in other words, the first clock of the next bus operation is overlapped with the last clock of the current bus operation. Therefore, address decoder and routing logic can operate in advance of the next bus operation. External address latches may hold the address stable for the entire bus operation, and provide additional ac and dc buffering.

The SAB 80286 does not maintain the address of the current bus operation during all TC states. Instead, the address for the next bus operation may be emitted during phase 2 of any TC. The address remains valid during phase 1 of the first TC to guarantee hold time, relative to ALE, for the address latch inputs.





Bus Cycle Termination

At maximum transfer rates, the SAB 80286 bus alternates between the status and command states. The bus status signals become inactive after TS so that they may correctly signal the start of the next bus operation after the completion of the current cycle. No external indication of TC exists on the SAB 80286 local bus. The bus master and bus controller enter TC directly after TS, and continue executing TC cycles until terminated by READY.

READY Operation

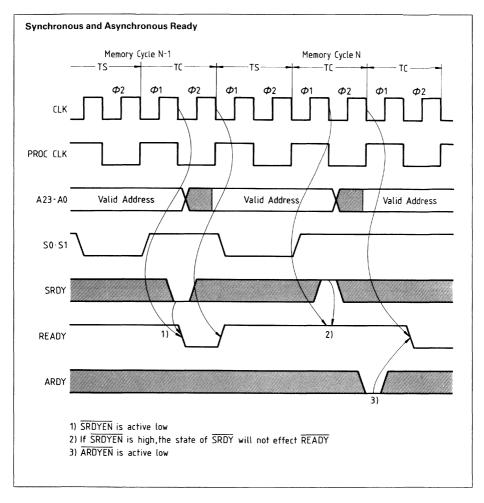
The current bus master and SAB 82288 bus controller terminate each bus operation simultaneously to achieve maximum bus bandwidth. Both are informed in advance by READY active which identifies the last TC cycle of the current bus operation. The bus master and bus controller must see the same sense of the READY signal, there by requiring READY be synchronous to the system clock.

Synchronous Ready

The SAB 82284 clock generator provides READY synchronization from both synchronous and asynchronous sources (see figure on next page). The synchronous ready input (SRDY) of the clock generator is sampled with the falling edge of CLK at the end of phase 1 of each TC. The state of SRDY is then transferred to the bus master and bus controller via the READY output line.

Asynchronous Ready

Many systems have devices of subsystems that are asynchronous to the system clock. As a result, their ready outputs cannot be guaranteed to meet the SAB 82284 SRDY setup and hold time requirements. But the SAB 82284 asynchronous ready input (ARDY) is designed to accept such signals. The ARDY input is sampled at the beginning of each TC cycle by SAB 82284 synchronization logic. This provides one system CLK cycle time to resolve its value before transferring it to the bus master and bus controller.

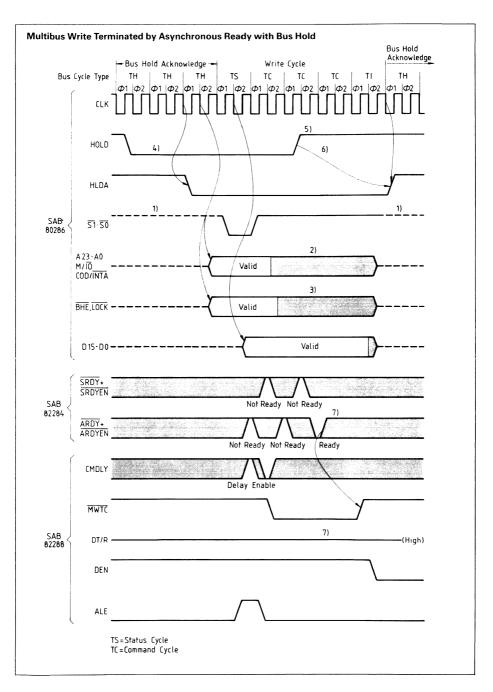


ARDY or ARDYEN must be high at the end of TS.
ARDY cannot be used to terminate a bus cycle with no wait states.

Each ready input of the SAB 82284 has an enable pin (SRDYEN and ARDYEN) to select whether the current bus operation will be terminated by the synchronous or asynchronous ready. Either of the ready inputs may terminate a bus operation. These enable inputs are active low and have the same timing as their respective ready inputs. An address decode logic usually selects whether the current bus operation should be terminated by ARDY or SRDY.

HOLD and HLDA

HOLD and HLDA allow another bus master to gain control of the local bus by placing the SAB 80286 bus into the TH state. The sequence of events required to pass control between the SAB 80286 and another local bus master is shown in the next figure.



- Status lines are not driven by SAB 80286 yet remain high due to pullup resistors in SAB 80288 and SAB 82289 during HOLD state.
- Address, M/IO and COD/INTA may start floating during any TC depending on when internal SAB 80286 bus arbiter decides to release bus to external HOLD. The float starts in ○2 of TC.
- 3) BHE and LOCK may start floating after the end of any TC depending on when internal SAB 80286 bus arbiter decides to release bus to external HOLD. The float starts in ⊘1 of TC.
- 4) The minimum HOLD to HLDA time in shown. Maximum is one TH longer.
- The earliest HOLD time is shown. It will always allow a subsequent memory cycle if pending as shown.
- 6) The minimum HOLD in HLDA time is shown. Maximum is a function of the instruction, type of bus cycle and other machine status (i.e., interrupts, waits, lock, etc.)
- Asynchronous ready allows termination of the cycle. Synchronous ready does not signal ready in this example. Synchronous ready state in ignored after ready is signalled via the asynchronous input.

Processor Extension Transfers

The processor extension interface uses I/O port addresses 00F8(H), 00FA(H), and 00FC(H) which are part of the I/O port address range reserved. An ESC instruction with EM = 0 and TS = 0 will perform I/O bus operations to one or more of these I/O port addresses independent of the value of IOPL and CPL.

ESC instructions with memory references enable the CPU to accept PEREQ inputs for processor extension operand transfers. The CPU will determine the operand starting address and read/write status of the instruction. For each operand transfer, two or three bus operations are performed, one word transfer with I/O port address 00FA(H) and one or two bus operations with memory. Three bus operations are required for each word operand aligned on an odd byte address.

Interrupt Acknowledge Sequence

The figure Interrupt Acknowledge Sequence illustrates a sequence performed by the SAB 80286 in response to an INTR input. An interrupt acknowledge sequence consists of two INTA bus operations. The first allows a master SAB 8259A programmable interrupt controller (PIC) to determine which if any of its slaves should return the interrupt vector. An eight-bit vector is read by the SAB 80286 during the

second INTA bus operation to select an interrupt handler routine from the interrupt table.

The master cascade enable (MCE) signal of the SAB 82288 is used to enable the cascade address drivers, during INTA bus operations (see interrupt acknowledge sequence figure), onto the local address bus for distribution to slave interrupt controllers via the system address bus. The SAB 80286 emits the LOCK signal (active low) during TS of both INTA bus operations. A local bus "hold" request will not be honored until the end of the second INTA bus operation.

Three idle processor clocks are provided by the SAB 80286 between INTA bus operations to allow for the minimum INTA to INTA time and CAS (cascade address) out delay of the SAB 8259A. The second INTA bus operation must always have at least one extra TC state added via logic controlling READY. A23—A0 are in tristate off until the first TC state of the second INTA bus operation. This prevents bus contention between the cascade address drivers and CPU address drivers. The extra TC state provides time for the SAB 80286 to resume driving the address lines for subsequent bus operations.

Local Bus Usage Priorities

The SAB 80286 local bus is shared among several internal units and external HOLD requests. In case of simultaneous requests, their relative priorities are:

(Highest)

Any transfers which assert <u>LOCK</u> either explicitly (via the LOCK instruction prefix) or implicitly (i.e. segment descriptor access, interrupt acknowledge sequence, or an XCHG with memory).

The second of the two byte bus operations required for an odd-aligned word operand.

The second or third cycle of a processor extension data transfer.

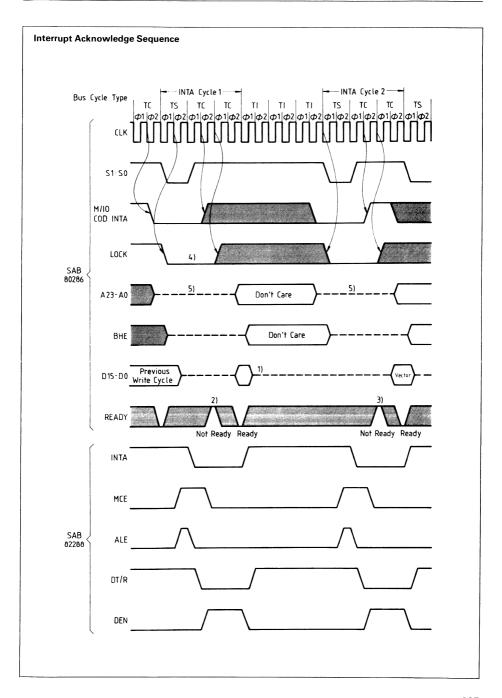
Local bus request via HOLD input.

Processor extension data operand transfer via PEREQ input.

Data transfer performed by EU as part of an instruction.

(Lowest)

An instruction prefetch request from BU. The EU wil inhibit prefetching two processor clocks in advance of any data transfer to minimize waiting by EU for a prefetch to finish.



Halt or Shutdown Cycles

The SAB 80286 externally indicates halt or shutdown conditions as a bus operation. These conditions occur due to an HLT instruction or multiple protection exceptions while attempting to execute one instruction. A halt or shutdown bus operation is signalled when \$1, \$50 and COD/INTA are low and M/IO is high. A1 high indicates halt, and A1 low indicates shutdown. The SAB 82288 bus controller does not issue ALE, nor is READY required to terminate a halt or shutdown bus operation.

During halt or shutdown, the SAB 80286 may service PEREQ or HOLD requests. A processor extension segment overrun exception during shutdown will inhibit further service of PEREQ. Either NMI or RESET will force the SAB 80286 out of halt or shutdown. An INTR, if interrupts are enabled, or a processor extension segment overrun exception will also force the SAB 80286 out of halt.

- 1) Data is ignored.
- First INTA cycle should have at least one wait state inserted to meet SAB 8259A minimum INTA pulse width.
- 3) Second INTA cycle must have at least one wait state inserted since the CPU will not drive A23–A0. BHE, and LOCK until after the first TC state.
 - The CPU-imposed one clock delay prevents bus contention between cascade address buffer being disabled by MCE $_{\downarrow}$ and address outputs. Without the wait state, the SAB 80286 address will not be valid for a memory cycle started immediately after the second INTA cycle. The SAB 8259A also requires one wait state for minimum INTA pulse width.
- LOCK is activated during the INTA cycles to prevent the SAB 82289 from releasing the bus between INTA cycles in a multimaster system.
- A23 A0 exit Tri-state OFF during Ø 2 of the second TC in the INTA cycle.

System Configuration

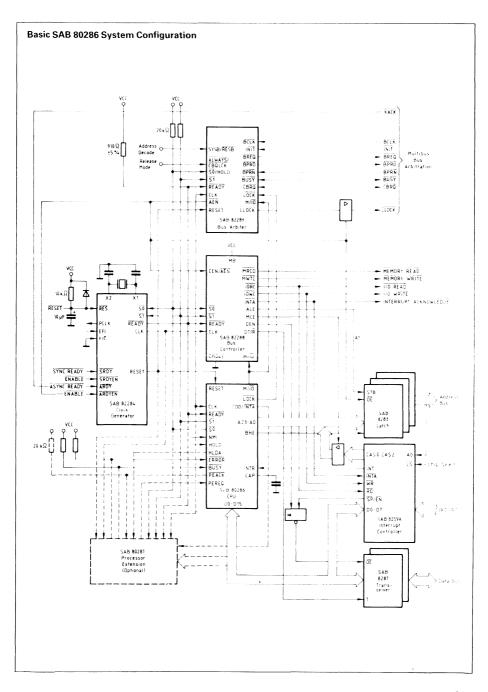
The versatile bus structure of the SAB 80286 microsystem, with a full complement of support chips, allows flexible configuration of a wide range of system. The basic configuration shown above is similar to an SAB 80286 maximum mode system. It includes the CPU plus an SAB 8259A interrupt controller, SAB 82284 clock generator and the SAB 82288 bus controller. The latches (SAB 8282A

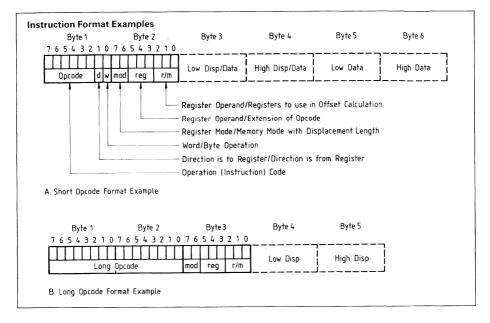
and SAB 8283A) and transceivers (SAB 8286A and SAB 8287A) used in an SAB 8086 system may be used in a SAB 80286 microsystem.

As indicated by the dashed lines in the figure above, the ability to add processor extensions is an integral feature of SAB 80286 microsystems. The processor extension interface allows external hardware to perform special functions and transfer data concurrently with CPU execution of other instructions. Full system integrity is maintained because the SAB 80826 supervises all data transfers and instruction execution for the processor extension. The SAB 80287 numeric processor extension (NPX), for example, uses this interface. The SAB 80287 has all the instructions and data types of an SAB 8087. The SAB 80287 NPX can perform numeric calculations and data transfers concurrently with CPU program execution. Numerics code and data have the same integrity as all other information protected by the SAB 80286 protection mechanism.

The SAB 80286 can overlap chip select decoding and address propagation during the data transfer for the previous bus operation. This information is latched into the SAB 8282A/8283A's by ALE in the middle of a TS cycle. The latched chip select and address information remains stable during the bus operation while the next cycles address is being decoded and propagated into the system. Decode logic can be implemented with a high-speed bipolar PROM.

The optional decode logic shown in the figure on basic system configuration takes advantage of the overlap between address and data of the SAB 80286 bus cycle to generate advance memory and IO-select signals. This minimizes system performance degradation caused by address propagation and decode delays. In addition to selection of memory and I/O, the advance selects may be used with configurations supporting local and system buses to enable the appropriate bus interface for each bus cycle. The COD/INTA and M/IO signals are applied to the decode logic to distinguish between interrupt, I/O, code, and data bus cycles. By adding the SAB 82289 bus arbiter chip, the SAB 80286 provides a Multibus system bus interface. A second SAB 82288 bus controller and additional latches and transceivers could be added to the local bus. This configuration allows the SAB 80286 to support an on-board bus for local memory and peripherals, and the Multibus for system bus interfacing.





SAB 80286 Instruction Set Summary

Instruction Timing Notes

The instruction clock counts listed below establish the maximum execution rate of the SAB 80286. With no delays in bus cycles, the actual clock count of an SAB 80286 program will average 5% more than the calculated clock count, due to instruction sequences which execute faster than they can be fetched from memory.

To calculate elapsed times for instruction sequences multiply the sum of all instruction clock counts, as listed in the table below, by the processor clock period. An 8 MHz processor clock has a clock period of 125 nanoseconds and requires an SAB 80286 system clock (CLK input) of 16 MHz.

Instruction Clock Count Assumptions

- The instruction has been prefetched, decoded, and is ready for execution. Control transfer instruction clock counts include all time required to fetch, decode, and prepare the next instruction for execution.
- 2. Bus cycles do not require wait states.
- There are no processor extension data transfer or local bus HOLD requests.
- 4. No exceptions occur during instruction execution.

Instruction Set Summary Notes

Addressing displacements selected by the MOD field are not shown. If necessary they appear after the instruction fields shown.

Above/below refers to unsigned value

Greater refers to positive signed value

Less refers to less positive (more negative) signed values

if d = 1 then to register; if d = 0 then from register

if w = 1 then word instruction; if w = 0 then byte instruction

if s = 0 then 16-bit immediate data form the operand

if s = 1 then an immediate data byte is signextended to form the 16-bit operand

x don't care

Z used for string primitives for comparison with ZF FLAG

If two clock counts are given, the smaller refers to a register operand and the larger refers to a memory operand

- add one clock if offset calculation requires summing 3 elements
- n = number of times repeated
- m = number of bytes of code in next instruction Level(L) - Lexical nesting level of the procedure

The following comments describe possible exceptions, side effects, and allowed usage for instructions in both operating modes of the SAB 80286.

Real address mode only

- 1. This is a protected mode instruction. Attempted execution in real address mode will result in an undefined opcode exception (6).
- A segment overrun exception (13) will occur if a word operand reference at offset FFFF(H) is attempted.
- This instruction may be executed in real address mode to initialize the CPU for protected mode.
- 4. The IOPL and NT fields will remain 0.
- Processor extension segment overrun interrupt (9) will occur if the operand exceeds the segment limit.

Fither mode

- An exception may occur, depending on the value of the operand.
- LOCK is automatically asserted regardless of the presence or absence of the LOCK instruction prefix.
- LOCK does not remain active between all operand transfers.

Protected virtual address mode only

- 9. A general protection exception (13) will occur if the memory operand can not be used due to either a segment limit or access rights violation. If a stack segment limit is violated, a stack segment overrun exception (12) occurs.
- 10. For segment load operations, the CPL, RPL and DPL must agree with privilege rules to avoid an exception. The segment must be present to avoid a not-present exception (11). If the SS register is the destination and a segment notpresent violation occurs, a stack exception (12) occurs.

- 11. All segment descriptor accesses in the GDT or LDT made by this instruction will automatically assert LOCK to maintain descriptor integrity in multiprocessor systems.
- JMP, CALL, INT, RET, IRET instructions referring to another code segment will cause a general protection exception (13) if any privilege rule is violated.
- A general protection exception (13) occurs if CPL ≠ 0
- A general protection exception (13) occurs if CPL>IOPL.
- The IF field of the flag word is not updated if CPL>IOPL. The IOPL field is updated only if CPL = 0.
- 16. Any violation of privilege rules as applied to the selector operand does not cause a protection exception; rather, the instruction does not return a result and the zero flag is cleared.
- 17. If the starting address of the memory operand violates a segment limit, or an invalid access is attempted, a general protection exception (13) will occur before the ESC instruction is executed. A stack segment overrun exception (12) will occur if the stack limit is violated by the operand's starting address. If a segment limit is violated during an attempted data transfer then a processor extension segment overrun exception (9) occurs.
- The destination of an INT, JMP, CALL, RET or IRET instruction must be in the defined limit of a code segment or a general protection exception (13) will occur.

Instruction Set Summary

		المام	Clock count	1400	Comments
Function	Format	Real address mode	Protected virtual address mode	Real address mode	Protected virtual address mode
Data Transfer					
MOV = MOVE: Register to register/memory	1000100w mod reg r/m	2,3 *	2,3 *	2	6
Register/memory to register	1000101w mod reg r/m	2,5*	2,5 *	2	6
Immediate to register/memory	$1100011 \text{ w} \mod 000 \text{ r/m}$ data data if w = 1	2,3 *	2,3 *	2	6
Immediate to register	1011 w reg data data if $w = 1$	2	2		
Memory to accumulator	1010000w addr-low addr-high	5	2	2	6
Accumulator to memory	1010001w addr-low addr-high	т	ю	2	6
Register/memory to segment register	10001110 mod0reg r/m	2,5 *	17, 19 *	2	9, 10, 11
Segment register to register/memory	10001100 mod0reg r/m	2,3 *	2,3 *	2	6
PUSH = Push:					
Memory	1111111 mod110 r/m	* 2	* 5	2	6
Register	01010 reg	т	ю	2	თ
Segment register	000reg110	ю	8	2	6
Immediate Control Control	O1110 Dec	•	ca.	i.	Ġ
PLESTA EDISHARITATION OF THE STATE OF THE ST	20000110	1-	<u> </u>	•	Ġ.
POP = Pop:	10001111 mod000 r/m	*	*	2	6
×) ц	ы и 		, σ
Register		ი	n 	7	ກ
Segment register	$0.00 \text{ reg } 1111$ (reg $\neq 01$)	22	50	2	9, 10, 11

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

		Clock	Clock count	Com	Comments
Function	Format	Real address mode	Protected virtual address mode	Real address mode	Protected virtual address mode
Data Transfer (cont'd):					
XCHG = Evchange					
Register/memory with register	1000011w mod reg r/m	3,5*	3,5*	2,7	7, 9
Register with accumulator	10010 reg	ю	m		
IN = Input from:					
Fixed port	1110010w port	2	2		14
Variable port	1110110w	Ŋ	2		14
OUT = Output to:			-		
Fixed port	1110011w port	ო	m		14
Variable port	1110111w	က	က		41
XLAT = Translate byte to AL	11010111	2	Ŋ		6
LEA =Load EA to register	10001101 mod reg r/m	* m	* m		
LDS = Load pointer to DS	11000101 mod reg r/m (mod ≠ 11)	7 *	21 *	2	9, 10, 11
LES = Load pointer to ES	11000100 mod reg r/m (mod \neq 11)	7 *	21 *	2	9, 10, 11
LAHF = Load AH with flags	10011111	2	2		
SAHF = Store AH into flags	10011110	2	2		
PUSHF = Push flags	10011100	က	ო	2	6
POPF = Pop flags	10011101	5	2	2, 4	2,4

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

		Clock	Clock count	Comr	Comments
Function	Format	Real address mode	Protected virtual address mode	Real address mode	Protected virtual address mode
Arithmetic ADD = Add:					
Reg/memory with register to either	00000dw modreg.r/m	2,7 *	2, 7*	2	6
Immediate to register memory	$100000 s w \mod 000 r/m$ data data $s w = 01$	3, 7 *	3,7 *	2	б
Immediate to accumulator	0000010 w data data if $w = 1$	ო	က		
ADC = Add with carry:					
Reg memory with register to either	000100dw mod reg r/m	2,7 *	2,7 *	2	6
Immediate to register/memory	$100000sw \mod 010 r/m$ data data if $sw = 01$	3,7 *	3,7 *	2	6
Immediate to accumulator	$\begin{bmatrix} 0.001010 \text{ w} \end{bmatrix}$ data $\begin{bmatrix} \text{data if w} = 1 \end{bmatrix}$	က	က		
INC = Increment					
Register memory	1111111 mod 000 r/m	2,7 *	2,7*	2	6
Register	01000 reg	2	2		
SUB = Subtract					
Reg memory and register to either	001010dw modreg r/m	2,7 *	2,7 *	2	6
Immediate from register memory	$100000sw \mod 101 r/m$ data data if $sw = 01$	3, 7 *	3, 7 *	7	6
Immediate from accumulator	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	က	ю		
SSB = Subtract with borrow:					
Reg/memory and register to either	000110dw mod reg r/m	2,7 *	2,7 *	2	6
Immediate from register/memory	$100000 s w \mod 011 r/m $ data data if $s w = 01$	3,7 *	3,7 *	2	6
Immediate from accumulator	0001110w data data data if w = 1	က	က		

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

		Clock count	count	Comi	Comments
Function	Format	Real address mode	Protected virtual address mode	Real address mode	Protected virtual address mode
Arithmetic (cont'd): DEC = Decrement: Register memory	11111111 mod 0 0 1 r/m	2,7*	2,7*	2	6
Register	01001 reg	2	2		
CMP = Compare : Register memory with register	0011101w mod reg r/m	2,6*	2,6*	2	6
Register with register/memory	0011100w mod reg r/m	2,7*	2,7 *	2	6
Immediate with register memory	100000sw mod 111 r/m data data if sw=01	3,6*	3,6 *	2	6
Immediate with accumulator	$\begin{array}{c c} 0 \ 0 \ 1 \ 1 \ 1 \ 1 \ w \end{array} \qquad \text{data} \qquad \text{data if } \mathbf{w} = 1$	က	ю		
NEG = Change sign	1111011w mod011r/m	2	7 *	2	7
AAA = ASCII adjust for add	00110111	m	ო		
DAA = Decimal adjust for add	00100111	က	ო		
AAS = ASCII adjust for subtract	00111111	e	ო		
DAS = Decimal adjust for substract	00101111	ო	က		
MUL = Multiply (unsigned):	11110111w mod 100 r/m				
register-byte		13	13		
register-word memory-byte		21	21	2	σ
menory-word		24 *	24 *	2 .	. 6
IMUL = Integer multiply (signed): register-byte register-word memory-byte memory-word	1111011w mod 101 r/m	13 21 16 * 24 *	13 21 16 * 24 *	2 2	തത

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

		Clock	Clock count	Comp	Comments
Function	Format	Real address mode	Protected virtual address mode	Real address mode	Protected virtual address mode
Arithmetic (cont'd):					
Milk = locate immediate multible signed				10	u z za
DIV = Divide unsigned):	1111011w mod110 r/m				
register-byte register-word		14	14	9	9
memory-byte memory-word		25 * 25 *	22 * 25 *	2, 6 2, 6	6,9 6,9
IDIV = Integer divide (signed):	1111011w mod111 r/m				
register-byte register-word		17	17	9	9 9
memory-byte memory-word		20 * 28 *	20 * 28 *	2,6	6,9 6,9
AMM = ASCII adjust for multiply	11010100 00001010	16	16		
AAD = ASCII adjust for divide	11010101 00001010	14	14		
CBW = Convert byte to word	10011000	2	2		
CWD = Convert word to double word	10011001	2	7		
Logic Shift/rotate instructions:					
Register/memory by 1	1101000w mod TTT r/m	2,7 *	2,7 *	2	6
Register/memory by CL	1101001w mod TTT r/m	5+n,8+n*	5+n,8+n*	2	б
Resident Control of Control	ALTOGORGOUS modern from the country of the country	10.0.010	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	64	57.
	100 SHL/SAL 101 SHR 111 SAR				

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

				Clock	Clock count	Com	Comments
Function	Format			Real address mode	Protected virtual address mode	Real address mode	Protected virtual address mode
Logic (cont'd): AND = And: Reg/memory and register to either	001000dw modreg r/m	m/1 69		2,7*	2,7 *	5	6
Immediate to register/memory	1000000w mod1	mod 100 r/m data	data if w = 1	3,7*	3,7 *	2	6
Immediate to accumulator	0010010w de	data data f w = '		т	ю		
TEST = And function to flags, no result:	22						
Register/memory and register	1000010w mod r	mod reg r/m		2,6*	2,6 *	2	6
Immediate data and register/memory	1111011w	mod 0 0 0 0 r/m data	data if $w = 1$	3, 6 *	3,6 *	2	6
Immediate data and accumulator	1010100w da	data data if w =	[<u>-</u>	ю	ю		
OR = Or:							
Reg/memory and register to either	000010dw modra	mod reg r/m		2,7 *	2,7 *	2	6
Immediate to register/memory	1000000w mod001 r/m	01 r/m data	data if w = 1	3,7 *	3,7 *	2	6
Immediate to accumulator	0000110w de	data data if w =		က	က		
XOR = Exclusive or:							
Reg/memory and register to either	001100dw mod r	mod reg r/m		2,7*	2,7 *	2	6
Immediate to register/memory	1000000 mod 1	mod 110 r/m data	data if $w = 1$	3,7 *	3,7 *	2	6
Immediate to accumulator	0011010w de	data data if w =		е	т		
NOT = Invert register/memory	1111011w mod 0	mod 0 1 0 r/m		2,7 *	2,7 *	2	6

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

		Clock	Clock count	Comments	nents
Function	Format	Real address mode	Protected virtual address mode	Real address mode	Protected virtual address mode
String Manipulation:					<u>l</u>
MOVS = Move byte word	1010010w	ശ	ഹ	2	ნ
CMPS = Compare byte/word	1010011w	∞	∞	2	6
SCAS = Scan byte/word	1010111w	7	7	2	6
LODS = Load byte/wd to AL/AX	1010110w	S.	2	2	6
STOS = Store byte/wd from AL/A	1010101w	ო	е	2	6
Repeated by count in CX					
MOVS = Move string	11110010 1010010w	5 + 4n	5 + 4n	2	6
CMPS = Compare string	11110012 1010011W	5 + 9n	5 + 9n	2,8	6 '8
SCAS = Scan string	11110012 1010111W	5 + 8n	5 + 8n	2,8	6,8
$\textbf{LODS} = Load \ string$	11110010 1010110w	5 + 4n	5 + 4n	2,8	8, 9
STOS = Store string	11110010 1010101W	4 + 3n	4 + 3n	2, 8	8, 9

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

		Clock	Clock count	Com	Comments
Function	Format	Real address mode	Protected virtual address mode	Real address mode	Protected virtual address mode
Control Transfer: CALL = Call:					
Direct within segment	11101000 disp-low disp-high	7 + m	7 + m	2	18
Register/memory indirect within seament	11111111 mod 010 r/m	7+m,11+m*	7+m,11+m* 7+m,11+m*	2,8	8, 9, 18
Direct intersegment	10011010 segment offset	13 + m	26 + m	2	11,12,18
	segment selector				
Protected mode only (direct intersegment): Via call gate to same privilege level Via call gate to different privilege level	rsegment): level no level no narameters		41 + m		8,11,12,18
Via Call gate to different privilege level, x parameters Via TSS	getevel, x parameters		86+4x+m 177+m		8,11,12,18 8,11,12,18 8,11,12,18
Via task gate			182+m		8,11,12,18
Indirect intersegment	$1111111 \mod 011 r/m$ (mod $\neq 11$)	16+n	29+n*	2	8,9,11,12,18
Protected mode only (indirect intersegment): Via call gate to same privileg level Via call gate different privilege level, no parameters Via call gate to different privilege level, x parameters Via TSS Via task gate	ntersegment): evel e level, no parameters ige level, x parameters		44+m* 83+m* 90-4x+m* 180+m*		8.9.11,12,13 8.9.11,12,13 8.9.11,12,18 8.9,11,12,18

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

					tarios Asolo	+41100	1	Commonte
					CIOCK	n n n		ellis
Function	Format				Real address mode	Protected virtual address mode	Real address mode	Protected virtual address mode
Control Transfer (cont'd):								
JMP = Unconditional jump:								
Short/long	111010111	disp-low		7	7+m	7+m		18
Direct within segment	11101011	disp-low	disp-high	7	7+m	7+m		18
Register/memory indirect within	11101010	mod 0 1 0 r/m			+ m,11+m*	7+m,11+m* 7+m,11+m* 2	2	9, 18
Direct intersegment	11101010	segment offset	offset	~	11+m	23+m		11,12,18
		segment selector	selector					
Protected mode only (direct intersegment):	nent):							
Via call gate to same privilege level Via TSS						38+m 175+m		8,11,12,18
Via task gate						180+m		8,11,12,18
Indirect intersegment	1111111	mod 101 r/m	$(mod \neq 11)$		15+m*	26+m*	2	8,9,11,12,18
Protected mode only (indirect intersegment):	gment):					:		
Via call gate to same privilege level Via TSS						41+m* 178+m*		8,9,11,12,18
Via task gate						183+m*		8,9,11,12,18
RET = Return from CALL:								
Within segment	11000011			-	11+m	11+m	2	8,9,18
Within seg adding immediate to SP	11000010	data-low	data-high	-	11+m	11+m	2	8,9,18
Intersegment	11001011				15+m	25+m	2	8,9,11,12,18
Intersegment adding immediate to SP	11001010	data-low	data-high	==	15+m		2	8,9,11,12,18
Protected mode only (RET):								
To different privilege level						55+m		9,11,12,18

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

			100			
			Clock count	count	Comr	Comments
Function	Format		Real address mode	Protected virtual address mode	Real address mode	Protected virtual address mode
Control Transfer (cont'd):						
JE/JZ = Jump on equal/zero	01110100	dsib	7+m or 3 7+m or 3	7+m or 3		18
JL/JNGE = Jump on less/not greater equal	01111100	dsib	7+m or 3 7+m or	7+m or 3		18
JLE/JNG = Jump on less or equal/not greater	01111110	dsib	7+m or 3 7+m or 3	7+m or 3	Maria dalahan men	18
JB/JNAE = Jump on below/not above or equal	01110010	dsib	7+m or 3 7+m or 3	7+m or 3		18
JBE/JNA = Jump on below or equal/not above	01110110	dsib	7+m or 3 7+m or	7+m or 3		18
JP/JPE = Jump on parity/parity even	01111010	dsib	7+m or 3 7+m or	7+m or 3		18
JO = Jump on overflow	01110000	dsib	7+m or 3 7+m or	7+m or 3		18
$\mathbf{JS} = Jump$ on sign	01111000	disp	7+m or 3 7+m or	7+m or 3		18
JNE/JNZ = Jump on not equal/not zero	01110101	disp	7+m or 3 7+m or	7+m or 3		18
JNL/JGE = Jump on not less/greater or equal	01111101	disp	7+m or 3 7+m or	7+m or 3		18
JNLE/JG = Jump on not less or equal/greater	01111111	disp	7+m or 3 7+m or	7+m or 3		18
JNB/JAE = Jump on not below/above or equal	01110011	disp	7+m or 3 7+m or	7+m or 3		18
JNBE/JA = Jump on not below or equal/above	01110111	disp	7+m or 3 7+m or	7+m or 3		18
JNP/JPO = Jump on not par/par odd	01111011	disp	7+m or 3	7+m or 3		18
JNO = Jump on not overflow	01110001	disp	7+m or 3 7+m or 3	7+m or 3		18
JNS = Jump on not sign	01111001	disp	7+m or 3 7+m or 3	7+m or 3		18
LOOP = Loop CX times	11100010	disp	8+m or 4 8+m or 4	8+m or 4		18
LOOPZ/LOOPE = Loop while zero/equal	11100001	dsib	8+m or 4 8+m or 4	8+m or 4		18
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000	disp	8+m or 4 8+m or	8+m or 4	ATTACAMA MARKATAN	18
JCXZ = Jump on CX zero	11100011	dsib	8+m or 4 8+m or 4	8+m or 4		18

Shaded areas indicate instructions not available in SAR RORR RORR microsystems

		Clock count	count	Comr	Comments
Function	Format	Real address mode	Protected virtual address mode	Real address mode	Protected virtual address mode
Control Transfer (cont'd):					
INT = Interrupt: Type specified	11001101 type	23+m		2, 7, 8	
Type 3	11001100	23+m		2, 7, 8	
INTO = Interrupt on overflow	11001110	24+m or 3 (3 if no	(3 if no	2, 6, 8	
Protected mode only: Via interrupt or trap gate to same privilege level Via interrupt or trap gate to fit different privilege level Via Task Gate	e privilege level fferent privilege level	D	interrupt) 40+m 78+m 167+m		7,8,11,12,18 7,8,11,12,18 7,8,11,12,18
IRET = Interrupt return	11001111	17+m	31+m	2, 4	8,9,11,12,15,18
Protected mode only: To different privilege level To different task $(NT = 1)$			55+m 169+m		8,9,11,12,15,18

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

		Clock	Clock count	Comments	nents
Function	Format	Real address mode	Protected virtual address mode	Real address mode	Protected virtual address mode
Processor Control					
CLC = Clear carry	111111000	2	2		
CMC = Complement carry	11110101	2	2		
STC = Set carry	111111001	2	2		
CLD = Clear direction	11111100	2	2		
STD = Set direction	11111101	2	2		
CLI = Clear interrupt	11111010	ю	ю		14
STI = Set interrupt	111111011	2	2		14
HLT = Halt	11110100	2	2		13
WAIT = Wait	10011011	က	ю		
LOCK = Bus lock prefix	11110000	0	0		14
ESC = Processor extension escape	11011TTT mod LLL r/m (TTLL are encode to processor extension)	9-20 *	9-20 *	5, 8	8, 17
SEG = Segment override prefix	001 reg 110	0	0		

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

Notes:

The effective address (EA) of the memory operand is computed according to the mod and r/m fields:

if mod = 11 then r/m is treated as a REG field if mod = 00 then DISP = 0*, disp-low and disp-high are absent

if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent

if mod = 10 then DISP = disp-high: disp-low

if r/m = 000 then EA = (BX) + (SI) + DISP

if r/m = 001 then EA = (BX) + (DI) + DISP

if r/m = 010 then EA = (BP) + (SI) + DISP

if r/m = 011 then EA = (BP) + (DI) + DISP if r/m = 100 then EA = (SI) + DISP

if r/m = 101 then EA = (DI) + DISP

if r/m = 110 then EA = (BP) + DISP* if r/m = 111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (before data if required)

REG is assigned according to the following table:

16-bit (w = 1)	8-bit ($w = 0$
000 AX	000 AL
001 CX	001 CL
010 DX	010 DL
011 BX	011 BL
100 SP	100 AH
101 BP	101 CH
110 SI	110 DH
111 DI	111 DI

The physical addresses of all operands addressed by the BP register are computed using the SS segment register. The physical addresses of the destination operands of the string primitive operations (those addressed by the DI register) are computed using the ES segment, which may not be overridden.

segment override prefix

reg is assigned according to the following:

	Segment
reg	register
00	ES
01	CS
10	SS
11	DS

^{*} except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

SAB 80286

Table 13 SAB 80286 Systems, Recommended Pullup Resistor Values

SAB 80286 Pin and name	Pullup value	Purpose
4- S1		
5- S 0	20 k $Ω ± 10%$	Pull \$\overline{S0}\$, \$\overline{S1}\$, and \$\overline{PEACK}\$ inactive during \$SAB 80286 hold periods
6-PEACK		
53-ERROR	20 kΩ ± 10%	Pull ERROR and BUSYinactive when SAB 80287 not present
54-BUSY	20 132 _ 10 70	(or temporarily removed from socket)
63-READY	910 Ω ± 5%	Pull READY inactive within required minimum time CL = 150 pF, IR ≤ 7 mA)

Absolute Maximum Ratings *)

Temperature under bias 0 to +70°C for SAB 80286-CG/SAB 80286-6-CG

0 to $+55^{\circ}\text{C}$ for SAB 80286-C/ SAB 80286-6-C

SAB 80286-CG-T0/55/ SAB 80286-6-CG-T0/55

Storage temperature

 $-65 \text{ to } +150^{\circ}\text{C}$

Voltage on any pin with respect to ground

-1.0 to +7V

Power dissipation

3.6W

DC Characteristics

TA = 0 to $70^{\circ}C$ for SAB 80286-CG/SAB 80286-6-CG;

TA = 0 to 55°C for SAB 80286-C/SAB 80286-6-C/SAB 80286-CG-T0/55/SAB 80286-6-CG-T0/55;

 $VCC = +5V \pm 5\%$

Symbol	Parameter	Limit	Limit values		Test condition
Symbol	rafaffietet	min.	max.	Unit	rest condition
VIL	Input low voltage	-0.5	+0.8		_
VIH	Input high voltage	2.0	VCC+0.5	v	
VOL	Output low voltage	-	0.45	•	IOL = 2.0 mA
VOH	Output high voltage	2.4	_		IOH = 400 μA
ICC	Power supply current		600	mA	TA = 0°C
100	Tower supply current	-	390		TA = 70°C
ILI	Input leakage current		± 10		0 V ≤ VIN ≤ VCC
IIL	Input sustaining current on BUSY and ERROR	30	500	μA	VIN = 0 V
ILO	Output leakage current		± 10		0.45 V ≤ VOUT ≤ VCC
ILO	Output leakage current		±1	mA	0 V ≤ VOUT ≤ 0.45 V
VCL	Clock input low voltage	-0.5	+0.6	v	
VCH	Clock input high voltage	3.8	VCC+0.5	•	
CIN	Capacitance of inputs (all input exept CLK)		10		
СО	Capacitance of I/O or outputs]-	20	pF	fC = 1 MHz
CCLK	Capacitance of CLK, READY, BUSY, ERROR, and RESET inputs				

^{*)} Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC Characteristics SAB 80286

 $TA = 0 \text{ to } 70^{\circ}\text{C for SAB } 80286\text{-CG/SAB } 80286\text{-6-CG};$

 $TA = 0 \ to \ 55^{\circ}C \ for \ SAB \ 80286-C/SAB \ 80286-G-C/SAB \ 80286-CG-T0/55/SAB \ 80286-6-CG-T0/55;$

 $VCC = +5V \pm 5\%$

AC timings are referenced to 0.8 V and 2.0 V points of signals as illustrated in data sheet waveforms, unless otherwise noted.

0 1 1	D	Lin	nit values	Unit	Test condition
Symbol	Parameter	min.	max.	Unit	rest condition
1	System clock (CLK) period	62	250		-
2	System clock (CLK) low time	15	225		at 1.0 V
3	System clock (CLK) high time	25	25 235		at 3.6 V
17	System clock (CLK) rise time		10		1.0 V to 3.6 V
18	System clock (CLK) fall time				3.6 V to 1.0 V
4	Async inputs, setup time	20			
5	Async inputs, hold time			ns	1)
6	RESET setup time	28			
7	RESET hold time	5			
8	Read data setup time	10			_
9	Read data hold time	8			
10	READY setup time	38.5			
11	READY hold time	25			
12	Status/PEACK valid delay	1	40		
13	Address valid delay	'	60		2) 3)
14	Write data valid delay				
15	Address/status/data float delay	0	50		2) 4)
16	HLDA valid delay				2) 3)

¹⁾ Asynchronous inputs are INTR, NMI, HOLD, PEREQ, ERROR, and BUSY. The specification is given only for testing purposes, to assure recognition at a specific CLK edge.

²⁾ Delay from 0.8 V on the CLK to 0.8 V or 2.0 V or float on the output as appropriate for valid or floating condition.

³⁾ Output load CL = 100 pF

⁴⁾ Float condition occurs when output current is less than ILO in magnitude.

SAB 82284 Timing Requirements

Symbol	Parameter	Limi	Limit values		Test condition
		min.	max.	Unit	rest condition
11	SRDY/SRDYEN setup time	15	15		
12	SRDY/SRDYEN hold time	//SRDYEN hold time	7_		
13	ARDY/ARDYEN setup time		30	ns	1)
14	ARDY/ARDYEN hold time	30			
19	PCLK delay	0	45		CL = 75 pF IOL = 5 mA IOH = -1 mA

¹⁾ These times are given for testing purposes to assure a predetermined action

SAB 82288 Timing Requirements

Symbol	Parameter		Limit values		Limit	T
Symbol Farameter			min.	max.	Unit	Test condition
12	CMDLY setup time		20			
13	CMDLT hold time		0			-
30	Command delay	Command delay		25		CL = 300 pF max.
29	from CLK Command active		3		ns	IOL = 32 mA max. IOH = -5 mA max.
16	ALE active delay			20		
17	ALE inactive delay			720	113	CL = 150 pF
19	DT/R read active delay			25	1	
22	DT/R read inactiv	e delay	5			
20	DEN read active of	delay	J	35		IOL = 16 mA max. IOH = -1 mA max.
21	DEN read inactive delay		3			
23	DEN write active delay		_	30		
24	DEN write inactiv	e delay	3	30		

AC Characteristics SAB 80286-6

TA = 0 to 70°C for SAB 80286-CG/SAB 80286-6-CG; TA = 0 to 55°C for SAB 80286-C/SAB 80286-6-C/SAB 80286-CG-T0/55/SAB 80286-6-CG-T0/55; VCC = $+5\,V\,\pm5\%$

AC timings are referenced to $0.8\,\mathrm{V}$ and $2.0\,\mathrm{V}$ points of signals as illustrated in data sheet waveforms, unless otherwise noted.

Ch al	Parameter	Limi	Limit values		Test condition
Symbol	Parameter	min.	max.	Unit	rest condition
1	System clock (CLK) period	83 250			_
2	System clock (CLK) low time	20	225		at 1.0 V
3	System clock (CLK) high time	25	230		at 3.6 V
17	System clock (CLK) rise time		10		1.0 V to 3.6 V
18	System clock (CLK) fall time		"		3.6 V to 1.0 V
4	Async inputs, setup time	30			
5	Async inputs, hold time	ns		ns	1)
6	RESET setup time	33			
7	RESET hold time	5	_		
8	Read data setup time	20			_
9	Read data hold time	8			
10	READY setup time	50			
11	READY hold time	35			
12	Status/PEACK valid delay	1	55		
13	Address valid delay	80			2) 3)
14	Write data valid delay		65		
15	Address/status/data float delay	0	80		2) 4)
16	HLDA valid delay				2) 3)

¹⁾ Asynchronous inputs are INTR, NMI, HOLD, PEREQ, ERROR, and BUSY. The specification is given only for testing purposes, to assure recognition at a specific CLK edge.

²⁾ Delay from 0.8 V on the CLK to 0.8 V or 2.0 V or float on the output as appropriate for valid or floating condition.

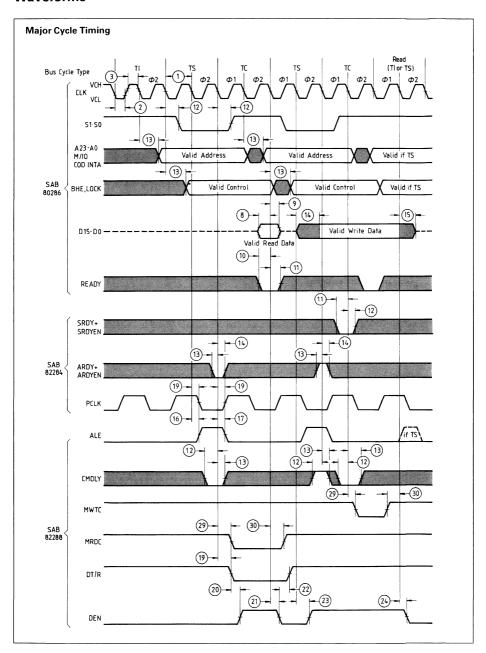
³⁾ Output load CL = 100 pF

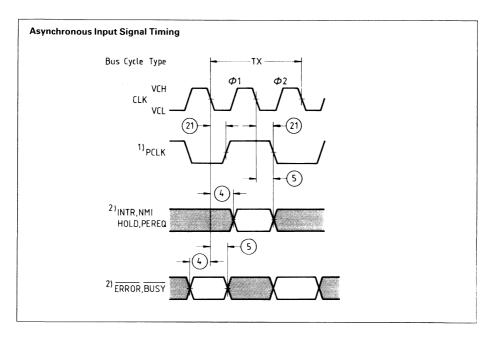
⁴⁾ Float condition occurs when output current is less than ILO in magnitude.

SAB 82288-6 Timing Requirements

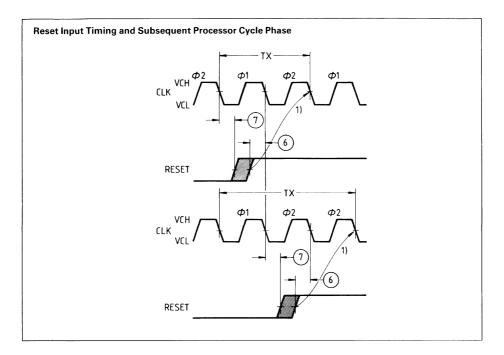
Cumbal	Parameter		Limit values		Unit	Test condition
Symbol	Parameter	rarameter		max.	Onit	
12	CMDLY setup time		25			
13	CMDLT hold time		0	1		
30	Command delay	Command dalay		30		CL = 300 pF max.
29	from CLK	Command active	3	40		IOL = 32 mA max. IOH = -5 mA max.
16	ALE active delay		1	25	ns	
17	ALE inactive dela	У	_	35	113	
19	DT/R read active delay		_	40		
22	DT/R read inactiv	re delay	5	45]	CL = 150 pF
20	DEN read active of	delay]	50		IOL = 16 mA max. IOH = -1 mA max.
21	DEN read inactive delay		3	40]	
23	DEN write active delay		_	35	1	
24	DEN write inactive delay		3	135		

Waveforms

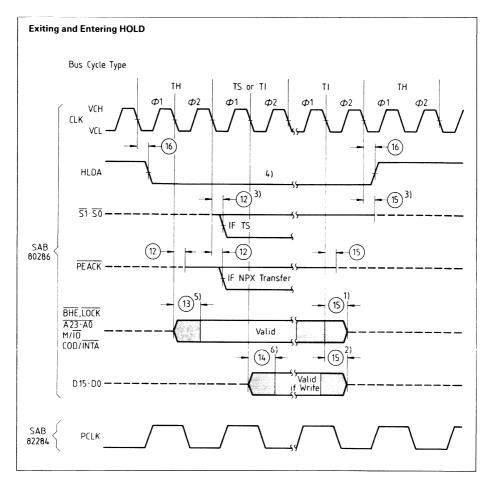




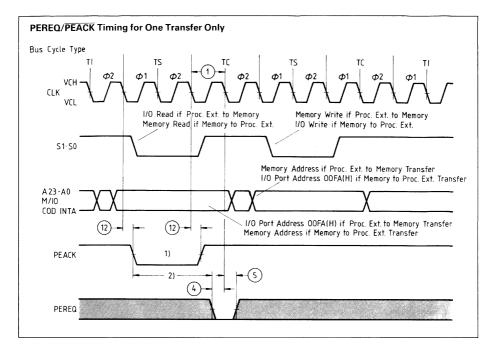
- 1) PCLK indicates which processor cycle phase will occur on the next CLK, PCLK may not indicate the correct phase until the first bus cycle is performed.
- 2) These inputs are asynchronous. The setup and hold times shown assure recognition for testing purposes.



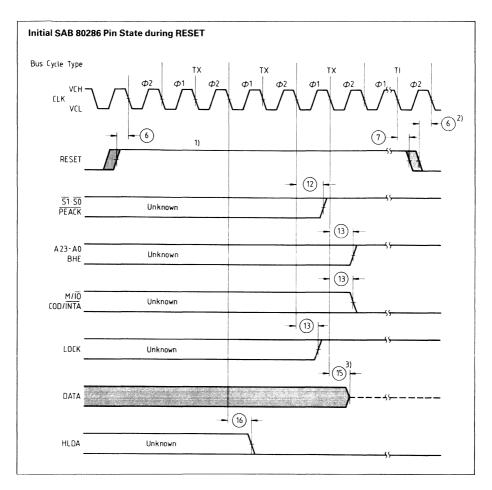
1) When RESET meets the setup time shown, the next CLK will start or repeat ϕ 2 of a processor cycle.



- 1) These signals may not be driven by the SAB 80286 during the time shown. The worst case in terms of latest float time is shown.
- 2) The data bus will be driven as shown if the last cycle before TI in the diagram was a write TC.
- 3) The SAB 80286 floats its status pins during TH. Pullup resistors in SAB 80288 keep these signals high.
- 4) For HOLD request set up to HLDA (refer to figure on Multibus write terminated by async ready).
- 5) BHE and LOCK are driven at this time but will not become valid until TS.
- 6) The data bus will remain in tristate off if a read cycle is performed.

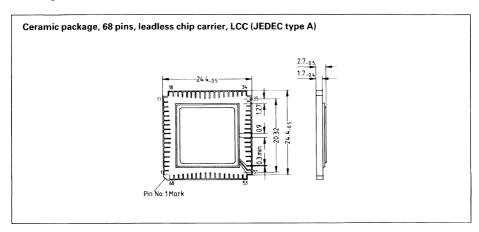


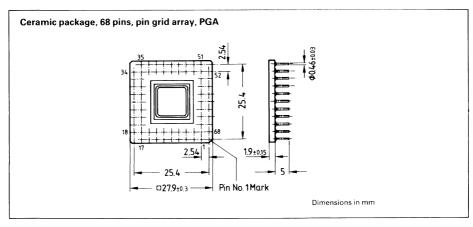
- PEACK always goes active during the first bus operation of a processor extension data operand transfer sequence. The first bus operation will be either a memory read at operand address or I/O read at port address 00FA(H).
- 2) To prevent a second processor extension data operand transfer, the worst case maximum time (shown above) is: 3X (1) (1) max (2) min. The actual, configuration-dependent, maximum time is: 3X (1) (1) max. (2) min + AX2X (1). A is the number of extra TC states added to either the first or second bus operation of the processor extension data operand transfer sequence.



- 1) Setup time for RESET ↑ may be violated with the consideration that ϕ 1 of the processor clock may begin one system CLK period later.
- 2) Setup and hold times for RESET $_{\downarrow}$ must be met for proper operation.
- 3) The data bus is only guaranteed to be in tristate off at the time shown.

Package Outline





Ordering Information

Туре	Description	Ordering code
SAB 80286-C	16-bit microprocessor, 8 MHz (CLCC)	Q67120-C151
SAB 80286-6-C	16-bit microprocessor, 6 MHz (CLCC)	Q67120-C226
SAB 80286-CG	16-bit microprocessor, 8 MHz (pin grid array)	Q67120-C222
SAB 80286-6-CG	16-bit microprocessor, 6 MHz (pin grid array)	Q67120-C228
SAB 80286-CG T0/55	16-bit microprocessor, 8 MHz (PGA, restr. temp.)	Q67120-C255
SAB 80286-6-CG T0/55	16-bit microprocessor, 6 MHz (PGA, restr. temp.)	Q67120-C256

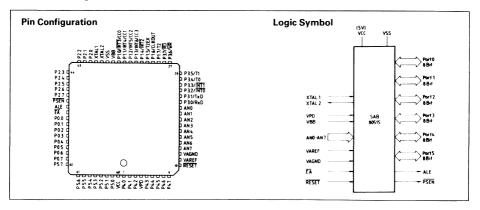
Preliminary

SAB 80515/80535 8-Bit Single-Chip Microcontroller

SAB 80515 SAB 80535 SAB 80515-T40/85 with factory-maskprogrammable ROM Control-oriented CPU with RAM and I/O facilities

SAB 80535-T40/85 Extended temperature range: -40 to +85°C

- 8K × 8 ROM (SAB 80515 only)
- 256 × 8 RAM
- Six 8-bit ports, 48 I/O lines
- Three 16-bit timer/event counters
- Highly flexible reload, capture, compare capabilities
- High-performance full-duplex serial channel
- Twelve interrupt sources, four priority levels
- High-precision 8-bit A/D converter with 8 multiplexed analog inputs and programmable internal reference voltages
- 16-bit watchdog timer
- VPD provides standby current for 40 bytes of RAM
- Boolean processor
- 256 bit-addressable locations
- Most instructions execute in 1 us
- 4 us multiply and divide
- External memory expandable to 128 Kbyte
- Upward-compatible with SAB 8051
- 68-pin plastic leaded chip carrier package (PLCC 68)



The SAB 80515/80535 is the newest member of the Siemens SAB 8051 family of 8-bit microcontrollers. It is fabricated in +5V advanced N-channel, silicongate Siemens MYMOS technology and supplied in 68-pin PLCC package. The SAB 80515/80535 is a stand-alone, high-performance single-chip microcontroller based on the SAB 8051 architecture. While maintaining all the SAB 8051 operating characteristics, the SAB 80515/80535 incorporates several enhancements which significantly increase design flexibility and overall system performance. The SAB 80515 contains a non-volatile 8K \times 8 read-only program memory; a volatile 256 \times 8 read/write data memory; 48 I/O lines; three 16-bit timer/counters, one with highly flexible reload, capture

and compare capabilities; a twelve-source, four-priority level, nested interrupt structure; a serial I/O port for either multiprocessor communication, I/O expansion, or full-duplex UART; an 8-bit A/D converter with eight multiplexed analog inputs and a programmable reference voltage unit; a 16-bit watchdog timer; as well as on-chip oscillator and clock circuits. The SAB 80535 is identical, except that it lacks the program memory.

For systems that require extra capability, the SAB 80515/80535 can be expanded using standard TTL-compatible memories and the byte-oriented SAB 808 and SAB 8085 peripherals.

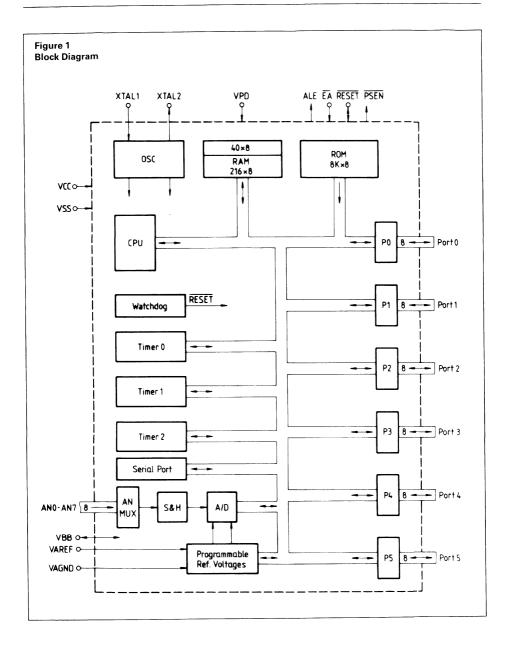
For the industrial temperature range -40 to $+85^{\circ}$ C, the SAB 80515/80535-T40/85 is available. 7.85

Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
P4.0-P4.7	1-3, 5-9	1/0	Port 4 is an 8-bit quasi-bidirectional I/O port. Port 4 can sink/source 4 LS-TTL loads
VPD	4		Power down supply. If VPD is held within its specs while VCC drops below specs, VPD will provide standby power to 40 byte of the internal RAM. When VPD is low, the RAM's current is drawn from VCC.
RESET	10	1	A low level on this pin for the duration of two machine cycles while the oscillator is running resets the SAB 80515. A small internal pullup resistor permits power-on reset using only a capacitor connected to VSS.
VAREF	11		Reference voltage for the A/D converter
VAGND	12		Reference ground for the A/D converter
AN7-AN0	13-20	ı	Multiplexed analog inputs
P3.0-P3.7	21-28	1/0	Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source 4 LS-TTL loads. The secondary functions are assigned to the pins of port 3, as follows: - RxD (P3.0): serial port's receiver data input (asynchronous) or data input/output (synchronous) - TxD (P3.1): serial port's transmitter data output (asynchronous) or clock output (synchronous) - INTO (P3.2): interrupt 0 input / timer 0 gate control input - INT1 (P3.3): interrupt 1 input / timer 1 gate control input - T0 (P3.4): counter 0 input - T1 (P3.5): counter 1 input - WR (P3.6): the write control signal latches the data byte from port 0 into the external data memory - RD (P3.7): the read control signal enables the external data memory to port 0
P1.7-P1.0	29-36	1/0	Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. It also contains the interrupt, timer, clock, capture and compare pins that are used by various options. The output latch must be programmed to a one (1) for that function to operate (except when used for the compare functions). Port 1 can sink/source 4 LS-TTL loads. The secondary functions are assigned to the port 1 pins, as follows: — INT3/CC0 (P1.0): interrupt 3 input/compare 0 output/capture 0 input — INT4/CC1 (P1.1): interrupt 4 input/compare 1 output/capture 1 input — INT5/CC2 (P1.2): interrupt 5 input/compare 2 output/capture 2 input — INT6/CC3 (P1.3): interrupt 6 input/compare 3 output/capture 3 input

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function	
P1.7-P1.0 (cont'd)			 - INT2 (P1.4): interrupt 2 input - T2EX (P1.5): timer 2 external reload trigger input - CLKOUT (P1.6): system clock output - T2 (P1.7): counter 2 input 	
VBB	37		Substrate pin. Must be connected to VSS through a capacitor (500 to 1000 pF) for proper operation of the A/D converter.	
XTAL2	39		XTAL2 is the output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal, ceramic resonator, or external source can be used.	
XTAL1	40		XTAL1 is the input to the oscillator's high gain amplifier. Required when a crystal or ceramic resonator is used. Connect to VSS when external source is used on XTAL2.	
P2.0-P2.7	41-48	1/0	Port 2 is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source 4 LS-TTL loads.	
PSEN	49	0	The program store enable output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods except during external data memory accesses. Remains high during internal program execution.	
ALE	50	0	Provides address latch enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.	
EA	51	I	When held at a TTL high level, the SAB 80515 executes instructions from the internal ROM when the PC is less than 8192. When held at a TTL low level, the SAB 80515 fetches all instructions from external program memory. For the SAB 80535 this pin must be tied low.	
P0.0-P0.7	52-59	1/0	Port 0 is an 8-bit open-drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source 8 LS-TTL loads.	
P5.7-P5.0	60-67	1/0	Port 5 is an 8-bit quasi-bidirectional I/O port. Port 5 can sink/source 4 LS-TTL loads	
VCC	68		POWER SUPPLY (+5V power supply during normal operation and program verification)	
VSS	38		GROUND (0 V)	



Functional Description

The members of the SAB 80515 family of microcontrollers are:

- SAB 80515 with factory mask-programmable
 8 Kbyte on-chip ROM
- SAB 80535 ROMless version of the SAB 80515

The architecture of the SAB 80515 is based on the SAB 8051 microcontroller family. The following features of the SAB 80515 are fully compatible with the SAB 8051 features:

- instruction set
- external memory expansion interface (port 0 and port 2)
- full-duplex serial port
- timer/counters 0 and 1
- alternate functions on port 3
- the lower 128 bytes of internal RAM and the lower
 4 Kbytes of internal ROM

Different to the SAB 8051 are the RAM power-down supply, which supplies 40 byte with a typical current of 1 mA, and the powerful interrupt structure with 12 sources and 4 priority levels.

The SAB 80515 additionally contains 128 byte of internal RAM and 4 Kbyte of internal ROM, that means a total of 256 byte RAM and 8 Kbyte ROM on-chip. The SAB 80515 has a new 16-bit timer/counter with a 2:1 prescaler, reload mode, compare and capture capability. It also contains a 16-bit watchdog timer, an 8-bit A/D converter with 8 analog inputs and programmable reference voltages, two additional quasi-bidirectional 8-bit ports, and a programmable clock output (fosc/12).

Figure 2 shows a detailled block diagram of the SAB 80515.

CPU

The SAB 80515 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in bithandling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 12 MHz crystal, 58% of the instructions execute in 1.0 µs.

Memory Organization

The SAB 80515 manipulates operands in the four memory address spaces described below:

Program memory

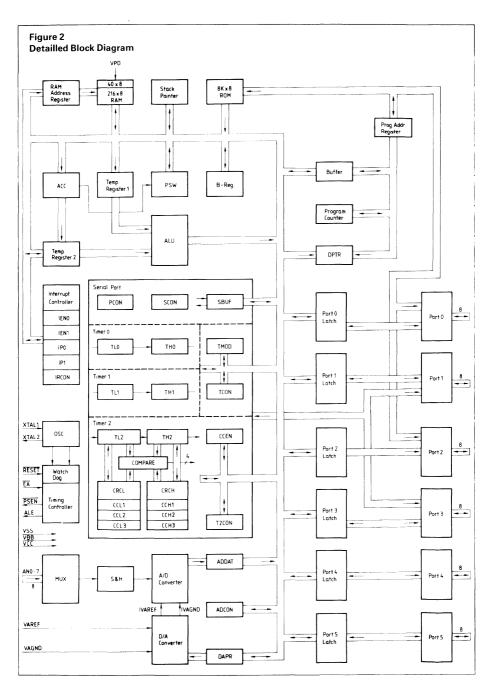
The SAB 80515 has 8 Kbyte of on-chip ROM, while the SAB 80535 has no internal ROM. The program memory can be externally expanded up to 64 Kbyte. If the EA pin is held high, the SAB 80515 executes out of internal ROM unless the address exceeds 1FFFH. Locations 2000H through 0FFFFH are then fetched from the external program memory. If the EA pin is held low, the SAB 80515 fetches all instructions from the external program memory. Since the SAB 80535 has no internal ROM, pin EA must be tied low when using this device.

Data memory

The data memory address space consists of an internal and an external memory space. The internal data memory is divided into three physically separate and distinct blocks: the lower 128 byte of RAM; the upper 128 byte of RAM; and the 128-byte special function register (SFR) area. While the upper 128 byte of data memory and the SFR area share the same address locations, they are accessed through different addressing modes. The lower 128 byte of data memory can be accessed through direct or register-indirect addressing; the upper 128 byte of RAM can be accessed through register-indirect addressing; and the special function registers are accessible through direct addressing.

Four 8-register banks occupy locations 0 through 1FH in the lower RAM area. The next 16 bytes, locations 20H through 2FH, contain 128 directly addressable bit locations. The stack can be located anywhere in the internal data memory address space, and the stack depths can be expanded up to 256 byte.

The external data memory can be expanded up to 64 Kbyte and can be accessed by instructions that use a 16-bit or an 8-bit address.



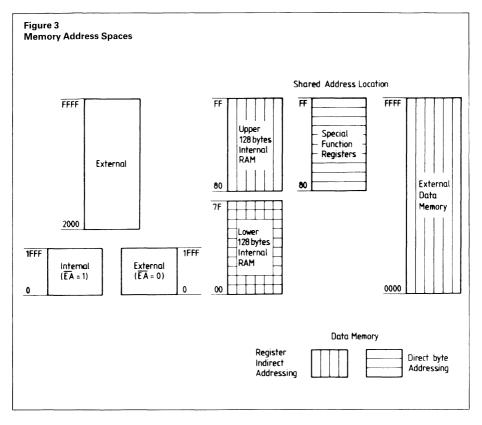
All registers, except the program counter and the four 8-register banks, reside in the special function register area. The 41 special function registers (SFR's) include arithmetic registers, pointers, and registers that provide an interface between the CPU

and the on-chip peripheral functions. There are also 128 directly addressable bits within the SFR area. The special function registers are listed in the following table:

Sy	mbol	Name	Address
*	P0	Port 0	80H
	SP	Stack pointer	81H
	DPL	Data pointer, low byte	82H
	DPH	Data pointer, high byte	83H
	PCON	Power control register	87H
*	TCON	Timer control register	88H
	TMOD	Timer mode register	89H
	TL0	Timer 0, low byte	BAH
	TL1	Timer 1, low byte	8BH
	TH0	Timer 0, high byte	8CH
	TH1	Timer 1, high byte	8DH
*	P1	Port 1	90H
*	SCON	Serial port control register	98H
	SBUF	Serial port buffer register	99H
*	P2	Port 2	0A0H
*	IEN0	Interrupt enable register 0	0A8H
	IP0	Interrupt priority register 0	0A9H
*	P3	Port 3	овон
*	IEN1	Interrupt enable register 1	0B8H
	IP1	Interrupt priority register 1	0В9Н
*	IRCON	Interrupt request control register	0C0H
	CCEN	Compare/capture enable register	0C1H
	CCL1	Compare/capture register 1, low byte	0C2H
	CCH1	Compare/capture register 1, high byte	0C3H
	CCL2	Compare/capture register 2, low byte	0C4H
	CCH2	Compare/capture register 2, high byte	0C5H
	CCL3	Compare/capture register 3, low byte	0C6H
	CCH3	Compare/capture register 3, high byte	0C7H
¥	T2CON	Timer 2 control register	0C8H
	CRCL	Compare/reload/capture register, low byte	0CAH
	CRCH	Compare/reload/capture register, high byte	освн
	TL2	Timer 2, low byte	оссн
	TH2	Timer 2, high byte	0CDH
*	PSW	Program status word register	0D0H
*	ADCON	A/D-converter control register	0D8H
	ADDAT	A/D-converter data register	0D9H
	DAPR	D/A-converter program register	0DAH
+	ACC	Accumulator	0E0H
*	P4	Port 4	0E8H
+	В	B register	оғон
+	P5	Port 5	0F8H

The SFR's marked with an asterisk (*) are both bit and byte-addressable.

Figure 3 illustrates the memory address spaces of the SAB 80515.



I/O Ports

The SAB 80515 has six 8-bit ports. Port 0 is an open-drain bidirectional I/O port, while ports 1 to 5 are quasi-bidirectional I/O ports with internal pullups. That means, when configured as inputs, ports 1 to 5 will pull high and will source current when externally pulled low. Port 0 will float when configured as input.

Port 0 and port 2 can be used to expand the program and data memory externally. During an access to external memory, port 0 emits the low-order address byte and reads/writes the data byte, while port 2 emits the high-order address byte. In this function, port 0 is not an open-drain port, but uses a strong internal pullup FET.

Ports 1 and 3 are provided for several alternate functions, as listed below:

Port	Symbol	Function
P1.0	INT3/CC0	External interrupt 3 input, compare 0 output, capture 0 input
P1.1	INT4/CC1	External interrupt 4 input, compare 1 output, capture 1 input
P1.2	INT5/CC2	External interrupt 5 input, compare 2 output, capture 2 input
P1.3	INT6/CC3	External interrupt 6 input, compare 3 output, capture 3 input
P1.4	INT2	External interrupt 2 input
P1.5	T2EX	Timer 2 external reload trigger input
P1.6	CLKOUT	System clock output
P1.7	T2	Timer 2 external counter input
P3.0	RXD	Serial input port
P3.1	TXD	Serial output port
P3.2	INTO	External interrupt 0 input, timer 0 gate control
P3.3	INT1	External interrupt 1 input, timer 1 gate control
P3.4	T0	Timer 0 external counter input
P3.5	T1	Timer 1 external counter input
P3.6	WR	External data memory write strobe
P3.7	RD	External data memory read strobe

Timer/Counters

The SAB 80515 contains three 16-bit timer/counters which are useful in many applications for timing and counting. The input clock for each timer/counter is 1/12 of the oscillator frequency in the timer operation or can be taken from an external clock source for the counter operation (maximum count rate is 1/24 of the oscillator frequency).

Timer/counters 0 and 1

These timer/counters can operate in four modes:

Mode 0: 8-bit timer/counter with 32:1 prescaler

Mode 1: 16-bit timer/counter

Mode 2: 8-bit timer/counter with 8-bit auto-reload

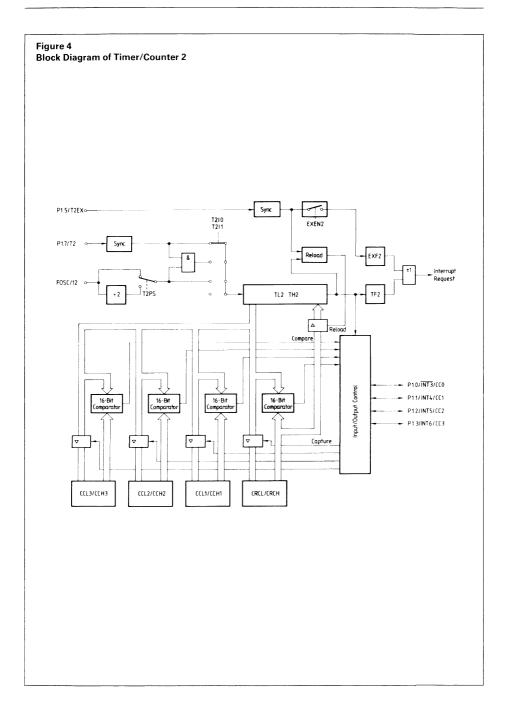
Mode 3: Timer/counter 0 is configured as one 8-bit timer/counter and one 8-bit timer; timer/counter 1 in this mode holds its count.

External inputs INTO and INT1 can be programmed to function as a gate for timer/counters 0 and 1 to facilitate pulse width measurements.

Timer/counter 2

Timer/counter 2 of the SAB 80515 is a 16-bit timer/counter with several additional features. It offers a 2:1 prescaler, a selectable gate function, and compare, capture and reload functions. Corresponding to the 16-bit timer register there are four 16-bit capture/compare registers, one of them can be used to perform a 16-bit reload on a timer overflow or external event. Each of these registers corresponds to a pin on port 1 for capture input/compare output.

Figure 4 shows a block diagramm of the timer/counter 2.



Reload

With the 16-bit CRC register, which is a concatanation of the 8-bit registers CRCL and CRCH, a 16-bit reload can be performed. There are two modes from which to select:

Mode 0: Reload is caused by a timer 2 overflow (auto-reload).

Mode 1: Reload is caused in response to a negative transition at pin T2EX (P1.5), which can also request an interrupt.

Compare

In the compare mode, the 16-bit values stored in the dedicated compare registers are compared to the contents of the timer 2 registers. If the count value in the timer 2 registers matches one of the stored values, an appropriate output signal is generated and an interrupt is requested. Two compare modes are provided:

Mode 0: Upon a match the output signal changes from low to high. It goes back to a low level when timer 2 overflows.

Mode 1: The transition of the output signal can be determined by software. A timer 2 over-flow causes no output change.

Capture

This feature permits saving the actual timer/counter contents into a selected register upon an external event or a software write operation. Two modes are provided to latch the current 16-bit value in timer 2 registers into a dedicated capture register:

Mode 0: Capture is performed in response to a transition at the corresponding port 1 pins CC0 to CC3.

Mode 1: Write operation into the low-order byte of the dedicated capture register causes the timer 2 contents to be latched into this register.

Serial Port

The serial port of the SAB 80515 permits the full duplex communication between microcontrollers or between microcontrollers and peripheral devices. The serial port can operate in 4 modes:

Mode 0: Shift register mode. Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted/received: 8 data bits (LSB first). The baud rate is fixed at 1/12 of the oscillator frequency.

Mode 1: 10 bits are transmitted (through RxD) or received (through TxD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). The baud rate is variable.

Mode 2: 11 bits are transmitted (through RxD) or received (through TxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). The baud rate is programmable to either 1/32 or 1/64 of the oscillator frequency.

Mode 3: 11 bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). Mode 3 is the same as mode 2 in all respects except the baud rate. The baud rate in mode 3 is variable.

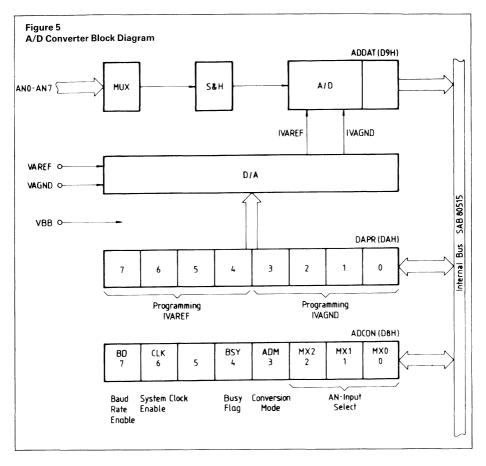
The variable baud rates can be generated by timer 1 or an internal baud rate generator.

A/D Converter

The 8-bit A/D converter of the SAB 80515 has 8 multiplexed analog inputs and is using the successive approximation method. The sampling of an analog signal takes 5 machine cycles, the total conversion time is 15 machine cycles (15 μs at 12 MHz oscillator frequency). Conversion can be programmed to be single or continuous, at the end of a conversion an interrupt can be generated.

The internal reference voltages IVAREF and IVAGND for the A/D converter are programmable in 16 steps with respect to the external reference voltages. This feature permits a second conversion with changed internal reference voltages to gain a higher resolution. In addition, the internal reference voltages can easily be adapted by software to the desired analog voltage range. The D/A conversion of the divide factors for the reference voltages takes 7 machine cycles each (7 µs at 12 MHz oscillator frequency).

Figure 5 shows a block diagram of the A/D converter of the SAB 80515.



Interrupt Structure

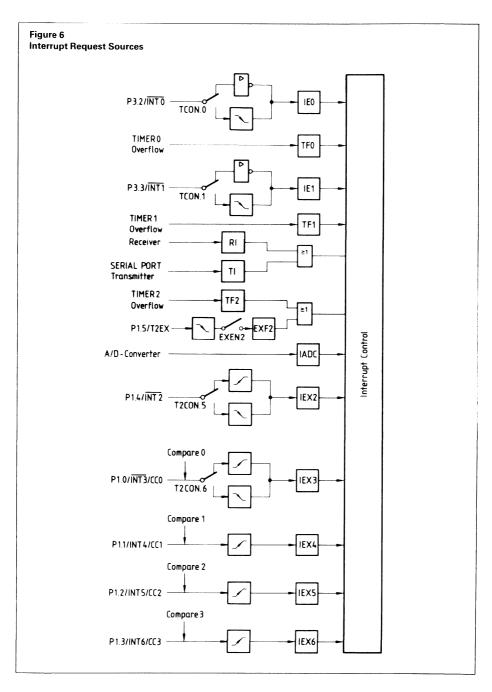
The 12 interrupt sources of the SAB 80515 are organized in 6 pairs:

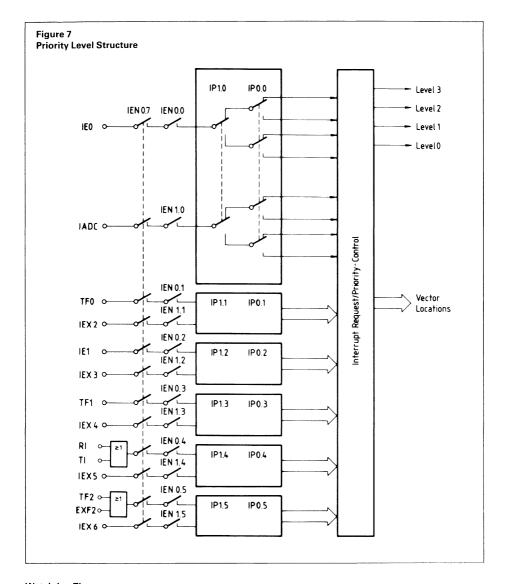
External interrupt 0	_	A/D converter interrupt
External interrupt 1	_	External interrupt 2
Timer 0 interrupt	_	External interrupt 3
Timer 1 interrupt	_	External interrupt 4
Serial port interrupt	_	External interrupt 5
Timer 2 interrupt	_	External interrupt 6

Each interrupt source has its own vector address. It can be programmed to one of four priority levels and can individually be enabled/disabled. The minimum interrupt response time is 3 to 8 machine cycles.

External interrupts 0 and 1 can be activated by a low-level or a negative transition (selectable) at their corresponding input pin, external interrupts 2 and 3 can be programmed to be activated by a negative or a positive transition. The external interrupts 4 to 6 are activated by a positive transition. The interrupts 3 to 6 can be combined with the corresponding alternate functions compare (output) and capture (input) on port 1.

Figure 6 shows the interrupt request sources, and figure 7 illustrates the priority level structure of the SAB 80515.





Watchdog Timer

This feature is provided as a means of graceful recovery from software upset. After a reset, the watchdog timer is cleared and stopped. It can be started and cleared by software, but it cannot be stopped. If the software fails to clear the watchdog timer at least every 65536 machine cycles (about 65 ms if a 12 MHz oscillator frequency is used), a

hardware reset will be initiated. The reset cause (external reset or reset caused by the watchdog) can be examined by software. To clear the watchdog, two bits in two different special function registers must be set by two consecutive instructions. This is done to prevent the watchdog from being cleared by unexpected op codes.

Instruction Set Summary

Mnemonic		Description	Byte	Cycle		
Arithmetic	Arithmetic operations					
ADD	A,Rn	Add register to accumulator	1	1		
ADD	A,direct	Add direct byte to accumulator	2	1		
ADD	A,@Ri	Add indirect RAM to accumulator	1	1		
ADD	A,#data	Add immediate data to accumulator	2	1		
ADDC	A,Rn	Add register to accumulator with carry flag	1	1		
ADDC	A,direct	Add direct byte to A with carry flag	2	1		
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1		
ADDC	A,#data	Add immediate data to A with carry flag	2	1		
SUBB	A,Rn	Subtract register from A with borrow	1	1		
SUBB	A,direct	Subtract direct byte from A with borrow	2	1		
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1		
SUBB	A,#data	Subtract immediate data from A with borrow	2	1		
INC	Α	Increment accumulator	1	1		
INC	Rn	Increment register	1	1		
INC	direct	Increment direct byte	2	1		
INC	@Ri	Increment indirect RAM	1	1		
DEC	Α	Decrement accumulator	1	1		
DEC	Rn	Decrement register	1	1		
DEC	direct	Decrement direct byte	2	1		
DEC	@Ri	Decrement indirect RAM	1	1		
INC	DPTR	Increment data pointer	1	2		
MUL	AB	Multiply A and B	1	4		
DIV	AB	Divide A by B	1	4		
DA	А	Decimal adjust accumulator	1	1		
Logical ope	rations					
ANL	A,Rn	AND register to accumulator	1	1		
ANL	A,direct	AND direct byte to accumulator	2	1		
ANL	A,@Ri	AND indirect RAM to accumulator	1	1		
ANL	A,#data	AND immediate data to accumulator	2	1		
ANL	direct,A	AND accumulator to direct byte	2	1		

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to accumulator	1	1
ORL	A,direct	OR direct byte to accumulator	2	1
ORL	A,@Ri	OR indirect RAM to accumulator	1	1
ORL	A,#data	OR immediate data to accumulator	2	2
ORL	direct,A	OR accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive OR register to accumulator	1	1
XRL	A,direct	Exclusive OR direct byte to accumulator	2	1
XRL	A,@Ri	Exclusive OR indirect RAM to accumulator	1	1
XRL	A,#data	Exclusive OR immediate data to accumulator	2	1
XRL	direct,A	Exclusive OR accumulator to direct byte	2	1
XRL	direct,#data	Exclusive OR immediate data to direct	3	2
CLR	Α	Clear accumulator	1	1
CPL	Α	Complement accumulator	1	1
RL	Α	Rotate accumulator left	1	1
RLC	Α	Rotate A left through carry flag	1	1
RR	Α	Rotate accumulator right	1	1
RRC	Α	Rotate accumulator right through carry flag	1	1
SWAP	Α	Swap nibbles within the accumulator	1	1

Data transfer

MOV	A,Rn	Move register to accumulator	1	1
MOV	A,direct *)	Move direct byte to accumulator	2	1
MOV	A,@Ri	Move indirect RAM to accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	Rn,A	Move accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct	3	2

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move code byte relative to DPTR to accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr.) to accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr.)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr.)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with accumulator	1	1
XCH	A,direct	Exchange direct byte with accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A	1	1

Boolean variable manipulation

CLR	С	Clear carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	С	Set carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	С	Complement carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry flag	2	2
ANL	C,/bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry flag	2	2
ORL	C,/bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry flag	2	1
MOV	bit,C	Move carry flag to direct bit	2	2

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Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Program an	d machine control			
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr.)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if accumulator is zero	2	2
JNZ	rel	Jump if accumulator is not zero	2	2
JC	rel	Jump if carry flag is set	2	2
JNC	rel	Jump if carry flag is not set	2	2
JB	bit,rel	Jump if direct bit is set	3	2
JNB	bit,rel	Jump if direct bit is not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct byte to A and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to A and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp. immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct byte and jump if not zero	3	2
NOP		No operation	1	1

rel

Notes on data addressing modes:

Rn - Working register R0-R7

direct – 128 internal RAM locations, any I/O port, control or status register

@Ri – Indirect internal RAM location addressed

by register R0 or R1

#data - 8-bit constant included in instruction #data 16 - 16-bit constant included as bytes 2 and 3

of instruction

bit – 128 software flags, any I/O pin, control

or status bit

A – Accumulator

Notes on program addressing modes:

addr 16 – Destination address for LCALL and LJMP may be anywhere within the 64-Kbyte program memory address space.

addr 11 – Destination address for ACALL and AJMP will be within the same 2-Kbyte page of program memory as the first byte of the following instruction.

 SJMP and all conditional jumps include an 8-bit offset byte. Range is +127/-128 bytes relative to first byte of the following instruction.

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Instruction Op Codes in Hexadecimal Order

	Ţ-						
Hex code	Number of bytes	Mnemonic	Operands	Hex code	Number of bytes	Mnemonic	Operands
00	1	NOP		34	2	ADDC	A,#data
01	2	AJMP	code addr	35	2	ADDC	A,data addr
02	3	LJMP	code addr	36	1	ADDC	A,@R0
03	1	RR	Α	37	1	ADDC	A,@R1
04	1	INC	A	38	1	ADDC	A,R0
05	2	INC	data addr	39	1	ADDC	A,R1
06	1	INC	@R0	3A	1	ADDC	A.R2
07	1	INC	@R1	3B	1	ADDC	A,R3
80	1	INC	R0	3C	1	ADDC	A,R4
09	1	INC	R1	3D	1	ADDC	A.R5
0A	1	INC	R2	3E	1	ADDC	A,R7
0B	1	INC	R3	3F	l i	ADDC	A,R7
0C	1	INC	R4	40	2	JC	code addr
0D	1	INC	R5	41	2	AJMP	code addr
0E	1	INC	R6	42	2	ORL	data addr,A
0F	1	INC	R7	43	3	ORL	data addr,#data
10	3	JBC	bit addr code addr	44	2	ORL	A,#data
11	2	ACALL	code addr	45	2	ORL	A,data addr
12	3	LCALL	code addr	46	1	ORL	A,@R0
13	1	RRC	A	47	1	ORL	A,@R1
14	1	DEC	A	48	l i	ORL	A,R0
15	2	DEC	data addr	49	l i	ORL	A,R1
16	1	DEC	@R0	4A	1	ORL	A,R2
17	1	DEC	@R1	4B	1	ORL	A,R3
18	1	DEC	R0	4C	1 1	ORL	A,R4
19	1	DEC	R1	4D	1	ORL	A,R5
1A	1	DEC	R2	4E	l i	ORL	A,R6
1B	1	DEC	R3	4F	1	ORL	A,R7
1C	1	DEC	R4	50	2	JNC	code addr
1D	1	DEC	R5	51	2	ACALL	code addr
1E	1	DEC	R6	52	2	ANL	data addr,A
1F	1	DEC	R7	53	3	ANL	data addr.#data
20	3	JB	bit addr code addr	54	2	ANL	A,#data
21	2	AJMP	code addr	55	2	ANL	A,data addr
22	1	RET		56	1	ANL	A,@R0
23	1	RL	Α	57	1	ANL	A,@R1
24	2	ADD	A,#data	58	1	ANL	A,R0
25	2	ADD	A,data addr	59	i	ANL	A,R1
26	1	ADD	A,@R0	5A	i	ANL	A,R2
27	1	ADD	A,@R1	5B	1	ANL	A,R3
28	1	ADD	A,R0	5C	1	ANL	A,R4
29	1	ADD	A,R1	5D	1	ANL	A,R5
2A	1	ADD	A,R2	5E	1	ANL	A,R6
2B	1	ADD	A,R3	5F	1	ANL	A,R7
2C	1	ADD	A,R4	60	2	JZ	code addr
2D	i	ADD	A,R5	61	2		code addr
2E	1	ADD	A,R6	62	2	XRL	
2F	1	ADD	A,R7	63	3		data addr.#data
30	3	JNB	bit addr, code addr	64	2	1	data addr, #data
31	2	ACALL	code addr	65	2	XRL	A,#data
32	1	RETI	oodo addi	66	1		A,data addr A,@R0
33	1	RLC	Α	67	1		
50	·			07	'	∧nL	A,@R1

Instruction Op Codes in Hexadecimal Order (cont'd)

Subsection	Hex code	Number of bytes	Mnemonic	Operands	Hex code	Number of bytes	Mnemonic	Operands
Substant			VDI	A DO	90	1	SLIBB	Λ R4
SUBB			1			1	1	· ·
Name		I		'		1		
Second		1	1	l '		1		· '
Table Tabl								
Fe		1	1					
The code and code a		I .						
1			1					
ACALL				· ·		1 '		
72						1		Ab
73								© D0 .1-11-1-
74 2 MOV A, #data A8 2 MOV R0,data addr 75 3 MOV data addr, #data A9 2 MOV R1,data addr 76 2 MOV @R0, #data AA 2 MOV R1,data addr 77 2 MOV R0, #data AB 2 MOV R3,data addr 78 2 MOV R0, #data AC 2 MOV R4,data addr 79 2 MOV R1, #data AD 2 MOV R4,data addr 7A 2 MOV R3, #data AE 2 MOV R6,data addr 7B 2 MOV R3, #data AE 2 MOV R7,data addr 7C 2 MOV R5, #data B0 2 ANL C,/bit addr 7F 2 MOV R6, #data B2 2 CPL bit addr 81 2 SJMP		1	l .	1 '				l ~ '
Total				~				
MOV	74						I .	
Total	75		MOV				ł.	
78 2 MOV R0,#data AC 2 MOV R4,data addr 79 2 MOV R1,#data AD 2 MOV R5,data addr 7A 2 MOV R2,#data AE 2 MOV R6,data addr 7B 2 MOV R3,#data AF 2 MOV R7,data addr 7C 2 MOV R4,#data B0 2 ANL C,/bit addr 7D 2 MOV R6,#data B1 2 ACALL code addr 7E 2 MOV R6,#data B2 2 CPL bit addr 7E 2 MOV R7,#data B3 1 CPL bit addr 7E 2 MOV R7,#data B3 1 CPL bit addr 7F 2 MOV R7,#data B3 1 CPL bit addr 80 2 SJMP code addr B5<	76	2	MOV	@R0,#data				
79 2 MOV R1, # data AD 2 MOV R5, data addr 7A 2 MOV R2, # data AE 2 MOV R6, data addr 7C 2 MOV R3, # data AF 2 MOV R7, data addr 7C 2 MOV R4, # data B0 2 ANL C,/bit addr 7D 2 MOV R5, # data B1 2 ACALL code addr 7E 2 MOV R6, # data B2 2 CPL bit addr 7F 2 MOV R7, # data B3 1 CPL C 80 2 SJMP code addr B4 3 CJNE A, # data, code addr 81 2 ANL C, bit addr B5 3 CJNE R0, # data, code addr 81 2 ANL C, bit addr B6 3 CJNE R0, # data, code addr 82 2 <	77	2	MOV	@R1,#data	AB		i	
7A 2 MOV R2, #data AE 2 MOV R6, data addr 7B 2 MOV R3, #data AF 2 MOV R7, data addr 7C 2 MOV R4, #data B0 2 ANL C, /bit addr 7D 2 MOV R6, #data B1 2 ACALL code addr 7E 2 MOV R6, #data B2 2 CPL bit addr 7F 2 MOV R7, #data B3 1 CPL C 80 2 SJMP code addr B4 3 CJNE A, #data, code addr 81 2 AJMP code addr B5 3 CJNE A, #data, code addr 82 2 ANL C, bit addr B6 3 CJNE R1, #data, code addr 84 1 DIV AB B8 3 CJNE R1, #data, code addr 85 3 MOV <td>78</td> <td>2</td> <td>MOV</td> <td>R0,#data</td> <td>AC</td> <td></td> <td>i</td> <td></td>	78	2	MOV	R0,#data	AC		i	
7B 2 MOV R3,#data AF 2 MOV R7,data addr 7C 2 MOV R4,#data B0 2 ANL C,/bit addr 7D 2 MOV R5,#data B1 2 ACALL code addr 7E 2 MOV R6,#data B2 2 CPL bit addr 7F 2 MOV R7,#data B3 1 CPL C 80 2 SJMP code addr B4 3 CJNE A,#data,code addr 81 2 AJMP code addr B5 3 CJNE A,#data,code addr 82 2 ANL C,bit addr B6 3 CJNE QR0,#data,code addr 84 1 DIV AB B8 3 CJNE R0,#data,code addr 84 1 DIV AB B8 3 CJNE R1,#data,code addr 85 3 MOV da	79	2	MOV	R1,#data	AD	2	MOV	R5,data addr
7B 2 MOV R3,#data AF 2 MOV R7,data addr 7C 2 MOV R4,#data B0 2 ANL C,/bit addr 7D 2 MOV R5,#data B1 2 ACALL code addr 7F 2 MOV R7,#data B3 1 CPL C 80 2 SJMP code addr B4 3 CJNE A,#data,code addr 81 2 AJMP code addr B5 3 CJNE QR0,#data,code addr 82 2 ANL C,bit addr B6 3 CJNE QR0,#data,code addr 83 1 MOVC A,@A+PC B7 3 CJNE QR1,#data,code addr 84 1 DIV AB B8 3 CJNE R0,#data,code addr 85 3 MOV data addr,data addr B9 3 CJNE R1,#data,code addr 86 2	7A	2	MOV	R2,#data	ΑE	2	MOV	R6,data addr
7C 2 MOV R4,#data B0 2 ANL C,/bit addr 7D 2 MOV R5, #data B1 2 ACALL code addr 7F 2 MOV R6, #data B2 2 CPL bit addr 80 2 SJMP code addr B4 3 CJNE A,#data,code addr 81 2 AJMP code addr B5 3 CJNE A,#data,code addr 81 2 ANL C,bit addr B6 3 CJNE QR0,#data,code addr 82 2 ANL C,bit addr B6 3 CJNE QR0,#data,code addr 83 1 MOV AB B8 3 CJNE R0,#data,code addr 84 1 DIV AB B8 3 CJNE R1,#data,code addr 85 3 MOV data addr,@R0 BA 3 CJNE R2,#data,code addr 86 2			MOV	R3,#data	AF	2	MOV	R7,data addr
7D 2 MOV R5,#data B1 2 ACALL ocde addr bit addr COPL bit addr 7F 2 MOV R7,#data B3 1 CPL C C 80 2 SJMP code addr B4 3 CJNE A,#data,code addr 81 2 AJMP code addr B5 3 CJNE QR0,#data,code addr 81 2 ANL C,bit addr B6 3 CJNE QR0,#data,code addr 83 1 MOVC A,@A+PC B7 B7 3 CJNE QR1,#data,code addr 84 1 DIV AB B8 3 CJNE R0,#data,code addr 85 3 MOV data addr,@R0 B8 3 CJNE R1,#data,code addr 86 2 MOV data addr,@R1 BB 3 CJNE R2,#data,code addr 87 2 MOV data addr,R1 BB 3 CJNE R3,#data,code addr 88 2 MOV data addr,R1 BD 3 CJNE R4,#data,code addr 88 2 MOV data addr,R1 BD 3 CJNE R6			моу	R4,#data	B0	2	ANL	C,/bit addr
7E 2 MOV R6,#data B2 2 CPL bit addr 7F 2 MOV R7,#data B3 1 CPL C 80 2 SJMP code addr B4 3 CJNE A,#data,code addr 81 2 AJMP code addr B5 3 CJNE A,data addr,code addr 82 2 ANL C,bit addr B6 3 CJNE QR0,#data,code addr 83 1 MOVC A,@A+PC B7 3 CJNE QR1,#data,code addr 84 1 DIV AB B8 3 CJNE R1,#data,code addr 85 3 MOV data addr,data addr B9 3 CJNE R1,#data,code addr 86 2 MOV data addr,R1 BB 3 CJNE R2,#data,code addr 87 2 MOV data addr,R1 BD 3 CJNE R3,#data,code addr 88			MOV	R5.#data	B1	2	ACALL	code addr
7F 2 MOV R7,#data B3 1 CPL C 80 2 SJMP code addr B4 3 CJNE A,#data,code addr 81 2 AJMP code addr B5 3 CJNE A,data addr,code addr 82 2 ANL C,bit addr B6 3 CJNE @R1,#data,code addr 83 1 MOV A,@A + PC B7 3 CJNE R0,#data,code addr 84 1 DIV AB B8 3 CJNE R0,#data,code addr 85 3 MOV data addr,@R0 BA 3 CJNE R1,#data,code addr 86 2 MOV data addr,@R1 BB 3 CJNE R2,#data,code addr 87 2 MOV data addr,R0 BC 3 CJNE R3,#data,code addr 88 2 MOV data addr,R1 BD 3 CJNE R6,#data,code addr <td< td=""><td></td><td></td><td></td><td></td><td>B2</td><td>2</td><td>CPL</td><td>bit addr</td></td<>					B2	2	CPL	bit addr
80 2 SJMP code addr B4 3 CJNE A,#data,code addr 81 2 AJMP code addr B5 3 CJNE A,data addr,code addr 82 2 ANL C,bit addr B6 3 CJNE @R0,#data,code addr 83 1 MOVC A,@A+PC B7 3 CJNE QR1,#data,code addr 84 1 DIV AB B8 3 CJNE R0,#data,code addr 85 3 MOV data addr,data addr B9 3 CJNE R1,#data,code addr 86 2 MOV data addr,@R1 BB 3 CJNE R2,#data,code addr 87 2 MOV data addr,R1 BB 3 CJNE R4,#data,code addr 88 2 MOV data addr,R1 BD 3 CJNE R5,#data,code addr 8A 2 MOV data addr,R3 BF 3 CJNE R6,#data,code addr			1	· ·	В3	1	CPL	c
81 2 AJMP code addr B5 3 CJNE A,data addr,code addr 82 2 ANL C,bit addr B6 3 CJNE @R0,#data,code addr 83 1 MOVC A,@A+PC B7 3 CJNE @R1,#data,code addr 84 1 DIV AB B8 3 CJNE R0,#data,code addr 85 3 MOV data addr,data addr B9 3 CJNE R1,#data,code addr 86 2 MOV data addr,@R0 BA 3 CJNE R3,#data,code addr 87 2 MOV data addr,R0 BC 3 CJNE R3,#data,code addr 88 2 MOV data addr,R1 BD 3 CJNE R4,#data,code addr 89 2 MOV data addr,R1 BD 3 CJNE R5,#data,code addr 80 2 MOV data addr,R1 BD 3 CJNE R6,#data,code addr		1 "	1	l '	В4	3	CJNE	A,#data,code addr
82 2 ANL C,bit addr B6 3 CJNE @R0,#data,code addr 83 1 MOVC A,@A+PC B7 3 CJNE @R1,#data,code addr 84 1 DIV AB B8 3 CJNE R0,#data,code addr 85 3 MOV data addr,@R0 BA 3 CJNE R1,#data,code addr 86 2 MOV data addr,@R1 BB 3 CJNE R2,#data,code addr 87 2 MOV data addr,R1 BB 3 CJNE R3,#data,code addr 88 2 MOV data addr,R1 BD 3 CJNE R8,#data,code addr 89 2 MOV data addr,R2 BE 3 CJNE R8,#data,code addr 88 2 MOV data addr,R2 BE 3 CJNE R6,#data,code addr 88 2 MOV data addr,R3 BF 3 CJNE R6,#data,code addr </td <td></td> <td></td> <td></td> <td></td> <td>B5</td> <td>3</td> <td>CJNE</td> <td>A,data addr.code addr</td>					B5	3	CJNE	A,data addr.code addr
83 1 MOVC A,@A+PC B7 3 CJNE @R1,#data,code addr 84 1 DIV AB B8 3 CJNE R0,#data,code addr 85 3 MOV data addr,@R0 BA 3 CJNE R1,#data,code addr 86 2 MOV data addr,@R0 BA 3 CJNE R2,#data,code addr 87 2 MOV data addr,R0 BC 3 CJNE R3,#data,code addr 88 2 MOV data addr,R1 BD 3 CJNE R3,#data,code addr 89 2 MOV data addr,R1 BD 3 CJNE R8,#data,code addr 80 2 MOV data addr,R2 BE 3 CJNE R8,#data,code addr 80 2 MOV data addr,R2 BE 3 CJNE R6,#data,code addr 80 2 MOV data addr,R3 BF 3 CJNE R7,#data,code addr <			1 ' '	1	B6	3	CJNE	@R0,#data.code addr
84 1 DIV AB B8 3 CJNE R0,#data,code addr 85 3 MOV data addr,data addr B9 3 CJNE R1,#data,code addr 86 2 MOV data addr,@R0 BA 3 CJNE R2,#data,code addr 87 2 MOV data addr,R0 BC 3 CJNE R3,#data,code addr 88 2 MOV data addr,R1 BD 3 CJNE R4,#data,code addr 89 2 MOV data addr,R1 BD 3 CJNE R5,#data,code addr 80 2 MOV data addr,R2 BE 3 CJNE R7,#data,code addr 80 2 MOV data addr,R3 BF 3 CJNE R7,#data,code addr 80 2 MOV data addr,R5 C1 2 PUSH data addr 80 2 MOV data addr,R5 C1 2 AJMP code addr		1	1				CJNE	@R1,#data.code addr
85 3 MOV data addr, data addr B9 3 CJNE R1, #data, code addr 86 2 MOV data addr, @R0 BA 3 CJNE R2, #data, code addr 87 2 MOV data addr, R0 BC 3 CJNE R3, #data, code addr 88 2 MOV data addr, R0 BC 3 CJNE R4, #data, code addr 89 2 MOV data addr, R1 BD 3 CJNE R5, #data, code addr 8A 2 MOV data addr, R2 BE 3 CJNE R5, #data, code addr 8A 2 MOV data addr, R3 BF 3 CJNE R7, #data, code addr 8C 2 MOV data addr, R4 C0 2 PUSH data addr 8C 2 MOV data addr, R5 C1 2 AJMP code addr 8E 2 MOV data addr, R6 C2 2 CLR bit a		1			_			
86 2 MOV data addr, @R0 BA 3 CJNE R2, #data, code addr 87 2 MOV data addr, @R1 BB 3 CJNE R3, #data, code addr 88 2 MOV data addr, R0 BC 3 CJNE R4, #data, code addr 89 2 MOV data addr, R1 BD 3 CJNE R5, #data, code addr 8A 2 MOV data addr, R2 BE 3 CJNE R6, #data, code addr 8B 2 MOV data addr, R3 BF 3 CJNE R7, #data, code addr 8C 2 MOV data addr, R4 C0 2 PUSH data addr 8C 2 MOV data addr, R5 C1 2 AJMP code addr 8E 2 MOV data addr, R6 C2 2 CLR bit addr 8F 2 MOV data addr, R6 C2 2 XCH A, data addr </td <td></td> <td></td> <td></td> <td></td> <td></td> <td>-</td> <td></td> <td>, , , , , , , , , , , , , , , , , , ,</td>						-		, , , , , , , , , , , , , , , , , , ,
87 2 MOV data addr, @R1 BB 3 CJNE R3, #data,code addr 88 2 MOV data addr, R0 BC 3 CJNE R4, #data,code addr 89 2 MOV data addr, R1 BD 3 CJNE R5, #data,code addr 8A 2 MOV data addr, R2 BE 3 CJNE R6, #data,code addr 8B 2 MOV data addr, R3 BF 3 CJNE R6, #data,code addr 8C 2 MOV data addr, R3 BF 3 CJNE R7, #data,code addr 8D 2 MOV data addr, R3 BF 3 CJNE R7, #data,code addr 8D 2 MOV data addr, R3 BF 3 CJNE R7, #data,code addr 8D 2 MOV data addr, R5 C1 2 AJMP code addr 8E 2 MOV data addr, R3 C2 2 CLR bit addr<								
88 2 MOV data addr, R0 BC 3 CJNE R4, #data,code addr 89 2 MOV data addr, R1 BD 3 CJNE R5, #data,code addr 8A 2 MOV data addr, R2 BE 3 CJNE R6, #data,code addr 8B 2 MOV data addr, R3 BF 3 CJNE R7, #data,code addr 8C 2 MOV data addr, R4 C0 2 PUSH data addr 8D 2 MOV data addr, R5 C1 2 AJMP code addr 8E 2 MOV data addr, R6 C2 2 CLR bit addr 8F 2 MOV data addr, R7 C3 1 CLR C 90 3 MOV DPTR, #data C4 1 SWAP A 91 2 ACALL code addr C5 2 XCH A,data addr 92 2 <td></td> <td></td> <td></td> <td></td> <td></td> <td>1</td> <td>1</td> <td>1 '</td>						1	1	1 '
89 2 MOV data addr, R1 BD 3 CJNE R5, #data,code addr 8A 2 MOV data addr, R2 BE 3 CJNE R6, #data,code addr 8B 2 MOV data addr, R3 BF 3 CJNE R7, #data,code addr 8C 2 MOV data addr, R4 C0 2 PUSH data addr 8D 2 MOV data addr, R5 C1 2 AJMP code addr 8E 2 MOV data addr, R6 C2 2 CLR bit addr 8F 2 MOV data addr, R7 C3 1 CLR C 90 3 MOV DPTR, #data C4 1 SWAP A 91 2 ACALL code addr C5 2 XCH A,data addr 92 2 MOV bit addr, C C6 1 XCH A,@R0 93 1 MOV			1				1	
8A 2 MOV data addr, R2 BE 3 CJNE R6,#data,code addr 8B 2 MOV data addr, R3 BF 3 CJNE R7,#data,code addr 8C 2 MOV data addr, R4 C0 2 PUSH data addr 8D 2 MOV data addr, R5 C1 2 AJMP code addr 8E 2 MOV data addr, R6 C2 2 CLR Dit addr 8F 2 MOV data addr, R7 C3 1 C CLR C 90 3 MOV DPTR, #data C4 1 SWAP A 91 2 ACALL code addr C5 2 XCH A,data addr 92 2 MOV bit addr, C C6 1 XCH A,@R0 93 1 MOVC A,@A+DPTR C7 1 XCH A,@R1 94 2 SUBB				1				
8B 2 MOV data addr, R3 BF 3 CJNE R7,#data,code addr 8C 2 MOV data addr, R4 C0 2 PUSH data addr 8D 2 MOV data addr, R5 C1 2 AJMP code addr 8E 2 MOV data addr, R6 C2 2 CLR bit addr 8F 2 MOV data addr, R7 C3 1 CLR C 90 3 MOV DPTR, #data C4 1 SWAP A 91 2 ACALL code addr C5 2 XCH A,data addr 92 2 MOV bit addr, C C6 1 XCH A,@R0 93 1 MOVC A,@A+DPTR C7 1 XCH A,@R1 94 2 SUBB A,#data C8 1 XCH A,R1 96 1 SUBB A,@R0 <t< td=""><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>1 '</td></t<>								1 '
8C 2 MOV data addr,R4 C0 2 PUSH data addr 8D 2 MOV data addr,R5 C1 2 AJMP code addr 8E 2 MOV data addr,R6 C2 2 CLR bit addr 8F 2 MOV data addr,R7 C3 1 CLR C 90 3 MOV DPTR,#data C4 1 SWAP A 91 2 ACALL code addr C5 2 XCH A,data addr 92 2 MOV bit addr,C C6 1 XCH A,@R0 93 1 MOVC A,@A+DPTR C7 1 XCH A,@R1 94 2 SUBB A,#data C8 1 XCH A,R0 95 2 SUBB A,@R0 CA 1 XCH A,R2 97 1 SUBB A,@R1 CB 1								1 '
8D 2 MOV data addr,R5 C1 2 AJMP code addr 8E 2 MOV data addr,R6 C2 2 CLR bit addr 8F 2 MOV data addr,R7 C3 1 CLR C 90 3 MOV DPTR,#data C4 1 SWAP A 91 2 ACALL code addr C5 2 XCH A,data addr 92 2 MOV bit addr,C C6 1 XCH A,data addr 93 1 MOVC A,@A+DPTR C7 1 XCH A,@R0 94 2 SUBB A,#ataa C8 1 XCH A,R0 95 2 SUBB A,data addr C9 1 XCH A,R1 96 1 SUBB A,@R0 CA 1 XCH A,R2 97 1 SUBB A,R0 CC 1		_	1	1				1 '
8E 2 MOV data addr,R6 C2 2 CLR bit addr 8F 2 MOV data addr,R7 C3 1 CLR C 90 3 MOV DPTR,#data C4 1 SWAP A 91 2 ACALL code addr C5 2 XCH A,data addr 92 2 MOV bit addr,C C6 1 XCH A,data addr 93 1 MOVC A,@A+DPTR C7 1 XCH A,@R1 94 2 SUBB A,#data C8 1 XCH A,R0 95 2 SUBB A,data addr C9 1 XCH A,R1 96 1 SUBB A,@R0 CA 1 XCH A,R2 97 1 SUBB A,R0 CC 1 XCH A,R3 98 1 SUBB A,R1 CD 1 X							1	
8F 2 MOV data addr,R7 C3 1 CLR C 90 3 MOV DPTR,#data C4 1 SWAP A 91 2 ACALL code addr C5 2 XCH A,data addr 92 2 MOV bit addr,C C6 1 XCH A,@R0 93 1 MOVC A,@A+DPTR C7 1 XCH A,@R1 94 2 SUBB A,#data C8 1 XCH A,R0 95 2 SUBB A,data addr C9 1 XCH A,R1 96 1 SUBB A,@R0 CA 1 XCH A,R2 97 1 SUBB A,R0 CC 1 XCH A,R3 98 1 SUBB A,R1 CB 1 XCH A,R4 99 1 SUBB A,R2 CE 1 XCH <			1					1
90 3 MOV DPTR,#data C4 1 SWAP A 91 2 ACALL code addr C5 2 XCH A,data addr 92 2 MOV bit addr,C C6 1 XCH A,@R0 93 1 MOVC A,@A+DPTR C7 1 XCH A,@R1 94 2 SUBB A,#data C8 1 XCH A,R0 95 2 SUBB A,data addr C9 1 XCH A,R1 96 1 SUBB A,@R0 CA 1 XCH A,R2 97 1 SUBB A,@R1 CB 1 XCH A,R3 98 1 SUBB A,R0 CC 1 XCH A,R4 99 1 SUBB A,R1 CD 1 XCH A,R6 9A 1 SUBB A,R2 CE 1 XCH A,R6							1	
91 2 ACALL code addr C5 2 XCH A,data addr 92 2 MOV bit addr,C C6 1 XCH A,@R0 93 1 MOVC A,@A+DPTR C7 1 XCH A,@R1 94 2 SUBB A,#data C8 1 XCH A,R0 95 2 SUBB A,data addr C9 1 XCH A,R1 96 1 SUBB A,@R0 CA 1 XCH A,R2 97 1 SUBB A,@R1 CB 1 XCH A,R3 98 1 SUBB A,R0 CC 1 XCH A,R4 99 1 SUBB A,R1 CD 1 XCH A,R6 9A 1 SUBB A,R2 CE 1 XCH A,R6				1				-
92							1	
93						1		
94 2 SUBB A,#data C8 1 XCH A,R0 95 2 SUBB A,data addr C9 1 XCH A,R1 96 1 SUBB A,@R0 CA 1 XCH A,R2 97 1 SUBB A,@R1 CB 1 XCH A,R3 98 1 SUBB A,R0 CC 1 XCH A,R4 99 1 SUBB A,R1 CD 1 XCH A,R5 9A 1 SUBB A,R2 CE 1 XCH A,R6		1						
95				,		1 '	1	
96	-			1 '		1 .	1	
97 1 SUBB A,@R1 CB 1 XCH A,R3 98 1 SUBB A,R0 CC 1 XCH A,R4 99 1 SUBB A,R1 CD 1 XCH A,R5 9A 1 SUBB A,R2 CE 1 XCH A,R6			1			1		
98						1 '	1	1 '
99 1 SUBB A,R1 CD 1 XCH A,R5 9A 1 SUBB A,R2 CE 1 XCH A,R6		ľ	1			1		1 '
9A 1 SUBB A,R2 CE 1 XCH A,R6	98	1	SUBB	l '				
0/1	99	1	SUBB	A,R1			1	
9B 1 SUBB A,R3 CF 1 XCH A,R7	9A	1	SUBB	A,R2				
	9B	1	SUBB	A,R3	CF	1	XCH	A,R7

Instruction Op Codes in Hexadecimal Order (cont'd)

		•	
Hex code	Number of bytes	Mnemonic	Operands
D0	2	POP	data addr
D1	2	ACALL	code addr
D2	2	SETB	bit addr
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	data addr,code addr
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,code addr
D9	2	DJNZ	R1,code addr
DA	2	DJNZ	R2,code addr
DB	2	DJNZ	R3,code addr
DC	2	DJNZ	R4,code addr
DD	2	DJNZ	R5,code addr
DE	2	DJNZ	R6,code addr
DF	2	DJNZ	R7,code addr
E0	1	MOVX	A,@DPTR
E1	2	AJMP	code addr
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,data addr *)
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	code addr
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	Α
F5	2	MOV	data addr,A
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	RO,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A
			,.

^{*)} MOV A,ACC is not a valid instruction

SAB 80515/80535

Absolute Maximum Ratings*)

Ambient temperature under bias 0 to + 70°C for SAB 80515/80535

-40 to + 85°C for SAB 80515/80535-T40/85

Storage temperature $-65 \text{ to } + 150^{\circ}\text{C}$ Voltage on any pin with respect to ground (VSS) -0.5 to + 7 V

Voltage on any pin with respect to ground (VSS) -0.9
Power dissipation 2 W

DC Characteristics

VCC = 5V \pm 10%; VSS = 0V; TA = 0 to 70°C; for SAB 80515/80535 TA = -40 to +85°C for SAB 80515/80535-T40/85

Symbol	Parameter	Limi	t values	Unit	Test condition
		min.	max.		
VIL	Input low voltage	-0.5	0.8		
VIH	Input high voltage (except RESET and XTAL2)	2.0	VCC+0.5		
VIH1	Input high voltage to XTAL2	2.5	10010.5		XTAL1 to VSS
VIH2	Input high voltage to RESET	3.0	-	v	_
VPD	Power-down voltage	3	5.5		VCC = 0 V
VOL	Output low voltage, ports 1, 2, 3, 4, 5		0.45		IOL = 1.6 mA
VOL1	Output low voltage, port 0, ALE, PSEN]	0.45		IOL = 3.2 mA
VOH	Output high voltage, ports 1, 2, 3, 4, 5	2.4	_		$IOH = -80 \mu A$
VOH1	Output high voltage, port 0, ALE, PSEN	12.4			IOH = -400 μA
IIL	Logic 0 input current, ports 1, 2, 3, 4, 5		-800	μΑ	VIL = 0.45 V
IIL2	Logic 0 input current, XTAL2		-2.5	mA	XTAL1 = VSS VIL = 0.45 V
IIL3	Input low current to RESET for reset	1_	-500	цА	VIL = 0.45 V
ILI	Input leakage current to port 0, EA]	±10	ļμA	0 V < VIN < VCC
ICC	Power supply current SAB 80515/80535 SAB 80515/80535-T40/85		210 230	mA	all outputs disconnected
IPD	Power-down current		3		VCC = 0 V
CIO	Capacitance of I/O buffer		10	pF	fc = 1 MHz

^{*)} Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

A/D Converter Characteristics

 $VCC = 5V \pm 10\%$; VSS = 0V; $VAREF = VCC \pm 5\%$; $VAGND = VSS \pm 0.2V$;

 $TA = 0 \text{ to } +70^{\circ}\text{C for SAB } 80515/80535$

 $TA = 40 \text{ to } +85^{\circ}\text{C for SAB } 80515/809535\text{-}T40/85$

Symbol	Parameter	Limit values			Unit	Test condition	
		min.	typ.	max.			
VAINPUT	Analog input voltage	VAGND- 0.2	_	VAREF+ 0.2	V		
CI	Analog input capacitance		25	_	pF	1)	
TS	Sample time			5 TCY		L''	
TC	Conversion time (including sample time)			15 TCY		for IVAREF = VAREF and IVAGND = VAGND	
		-	_	22 TCY	μ s	for IVAREF # VAREF and IVAGND = VAGND or for IVAREF = VAREF and IVAGND # VAGND	
				29 TCY		for IVAREF # VAREF and IVAGND # VAGND	
	Differential non-linearity		±1/2	±1		IVAREF =	
	Integral non-linearity		±1/2	± 1	LSB	VAREF = VCC IVAGND =	
	Offset error		±1/2	±1		VAGND = VSS Ri of analog	
	Gain error		±1/2	±1		input source ≤10 kΩ	
IREF	VAREF supply current		_	5	mA	2)	

¹⁾ The internal resistance of the analog source must be less than 10 k Ω to assure full loading of the sample capacitance during sample time.

²⁾ The internal resistance of the analog reference voltage source must be less than 1 k Ω .

AC Characteristics

 $VCC = 5 V \pm 10\%$; VSS = 0 V

 $TA = 0 \text{ to } 70^{\circ}\text{C for SAB } 80515/80535$

 $TA = -40 \text{ to } +85^{\circ}\text{C for SAB } 80515/80535\text{-}T40/85$

(CL for port 0, ALE and \overline{PSEN} outputs = 100 pF; CL for all other outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	Limit values				
•		12 MI	Hz Clock	Variable clock 1/TCLCL = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
TCY	Cycle time	1000	_	12TCLCL		
TLHLL	ALE pulse width	127		2TCLCL-40		
TAVLL	Address setup to ALE	53	_	TCLCL-30		
TLLAX1	Address hold after ALE	48		TCLCL-35		
TLLIV	ALE to valid instruction in	_	233	_	4TCLCL-100	
TLLPL	ALE to PSEN	58		TCLCL-25		ns
TPLPH	PSEN pulse width	215	_	3TCLCL-35		
TPLIV	PSEN to valid instruction in	_	150	-	3TCLCL-100	
TPXIX	Input instruction hold after PSEN	0	_	0	-	
TPXIZ*)	Input instruction float after PSEN	_	63	_	TCLCL-20	
TPXAV*)	Address valid after PSEN	75	_	TCLCL-8	_	
TAVIV	Address to valid instruction in	_	302	_	5TCLCL-115	
TAZPL	Address float to PSEN	0	_	0	-	

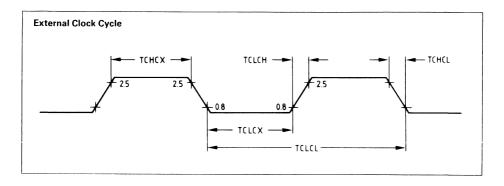
External Data Memory Characteristics

Symbol	Parameter		Limit values				
•		12 MHz Clock		Variable clock 1/TCLCL = 1.2 MHz to 12 MHz			
		min.	max.	min.	max.		
TRLRH	RD pulse width	400		6TCLCL-100			
TWLWH	WR pulse width	400	-	61CLCL-100			
TLLAX2	Address hold after ALE	132		2TCLCL-35			
TRLDV	RD to valid data in	_	250	_	5TCLCL-165		
TRHDX	Data hold after RD	0	_	0	-		
TRHDZ	Data float after RD		97		2TCLCL-70		
TLLDV	ALE to valid data in	_	517	7-	8TCLCL-150	ns	
TAVDV	Address to valid data in		585		9TCLCL-165		
TLLWL	ALE to WR or RD	200	300	3TCLCL-50	3TCLCL+50		
TAVWL	Address to WR or RD	203	-	4TCLCL-130	_		
TWHLH	WR or RD high to ALE high	43	123	TCLCL-40	TCLCL+40		
TDVWX	Data valid to WR transition	33		TCLCL-50			
TQVWH	Data setup before WR	433	7-	7TCLCL-150	7-		
TWHQX	Data hold after WR	33		TCLCL-50	7		
TRLAZ	Address float after RD	-	0	-	0	1	

^{*)} Interfacing the SAB 80515 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

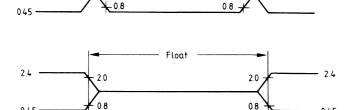
External Clock Drive XTAL2

Symbol	Parameter		Limit values		
		Variable clock Freq. = 1.2 MHz to 12 MHz			
		min.	max.		
TCLCL	Oscillator period	83.3	833.3		
TCHCX	High time	20	TCLCL-TCLCX		
TCLCK	Low time	20	TCLCL-TCHCX	ns	
TCLCH	Rise time		20		
TCHCL	Fall time		20		





0.45 -



Test Points

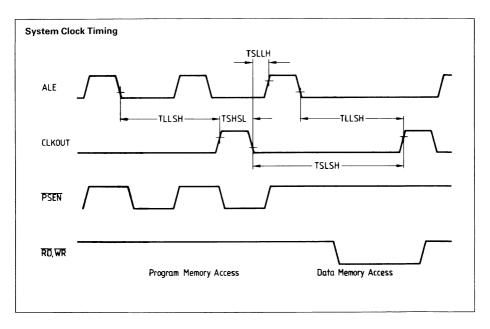
- 2.0

AC testing inputs are driven at 2.4 V for a logic "1" and at 0.45 V for a logic "0". Timing measurements are made at 2.0 V for a logic "1" and at 0.8 V for a logic "0". For timing purposes, the float state is defined as the point where a P0 pin sinks 3.2 mA or sources 400 uA at voltage test levels.

- 0.45

System Clock Timing

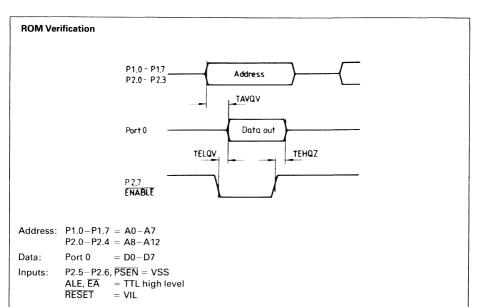
Symbol	Parameter	Limit values				
		12 MHz clock		Variable clock 1/TCLCL = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
TLLSH	ALE to CLKOUT	543		7TCLCL-40		
TSHSL	CLKOUT high time	127	_	2TCLCL-40]-	ns
TSLSH	CLKOUT low time	793		10TCLCL-40	=	
TSLLH	CLKOUT low to ALE high	43	123	TCLCL-40	TCLCL+40]



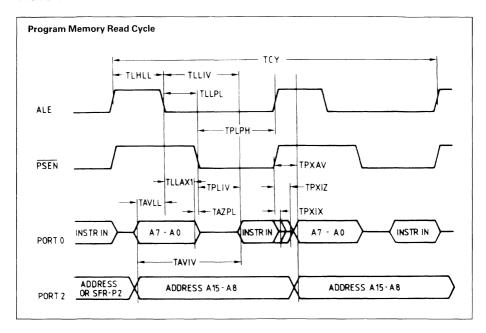
ROM Verification Characteristics

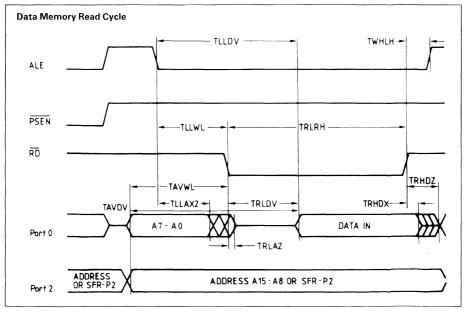
 $TA = 25^{\circ}C \pm^{\circ}C$; $VCC = 5V \pm 10\%$; VSS = 0 V

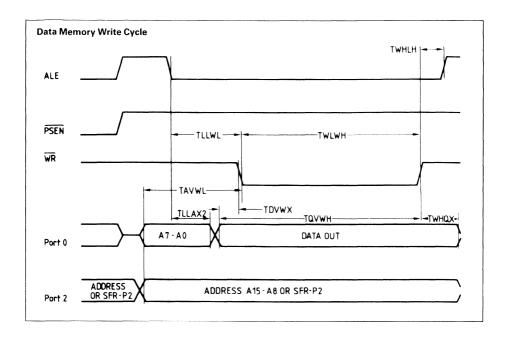
Symbol	Parameter		Unit	
		min.	max.	
TAVQV	Address to valid data			i
TELQV	ENABLE to valid data		48 TCLCL	ns
TEHQZ	Data float after ENABLE	0		
1/TCLCL	Oscillator frequency	4	6	MHz

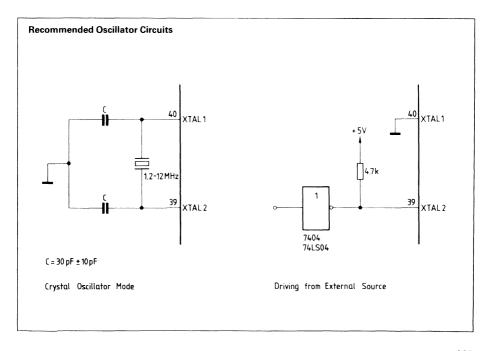


Waveforms

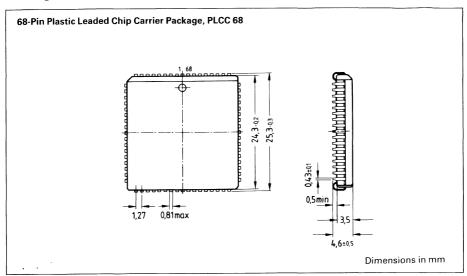








Package Outline



Ordering Information

Туре	Description	Ordering Code
	8-bit single-chip microcomputer	
SAB 80515-N	with mask-programmable ROM (plastic)	Q 67120-C211
SAB 80535-N	for external memory (plastic)	Q 67120-C241
SAB 80515- N -T40/85	with mask-programmable ROM (plastic)	Q 67120-C210
SAB 80535- N-T40/85	for external memory (plastic)	Q 67120-C240

Telephone Controller (Single-Chip 8-Bit CMOS Microcontroller)

Preliminary data

CMOS circuit

Type	Ordering Code	Package
SAB 80 C 482	Q67100-Z154	DIP 40
SAB 80 C 382*)	Q67100-H3205	DIP 40
SAB 80 C 382-PC	Q67100-H3199	Piggyback

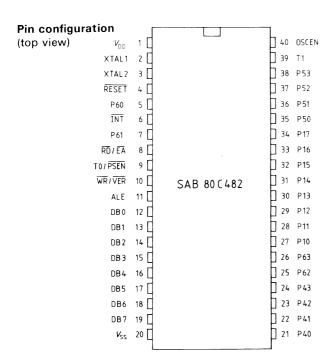
The SAB 80 C 482 is a low-power, advanced CMOS member of the popular SAB 8084 familiy. The SAB 80 C 482 contains double-sized program memory and 4 additional I/O lines. For systems that require extra capability, the SAB 80 C 482 can easily be expanded using CMOS external memories. The on-chip mask-programmable keyboard wake-up offers a convenient solution for a power-saving keyboard scanner. The SAB 80 C 482 has the same cycle time at about half the SAB 8048 clock frequency. The 100% static operation provides the possibility to optimize between power consumption and program speed.

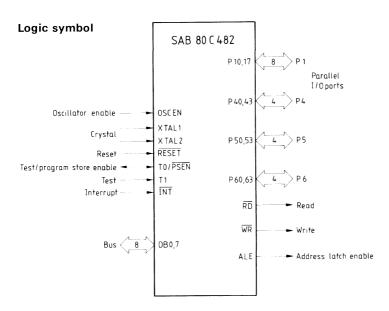
The CMOS design of the SAB 80 C 482 opens new application areas that require battery operation, low power standby, wide voltage range, and the ability to maintain operation during AC power line interruptions. These applications include telecommunications, automotive, consumer, portable, and hand-held instruments.

*) The SAB 80 C 382 is the ROM-less version of the SAB 80 C 482

- 2K × 8 ROM
- 64 × 8 RAM
- 31 I/O lines
- 2.66 µs cycle time (with 3 MHz crystal)
- Automatic power-on reset
- Keyboard wake-up

- Very low power consumption
- Normal: 1.2 mA@5 V@8 µs cycle
- Halt: 0.4 mA@5 V@8 µs cycle
- Standby: 1 µA @5 V
- 100% static operation
- Supply voltage: 2.5 to 6 V

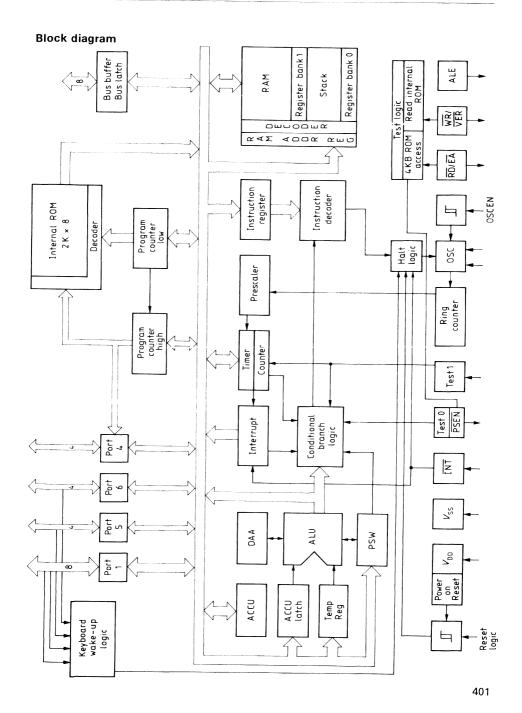




Pin description

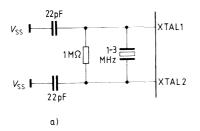
Pin No.	Symbol	Description
2	XTAL1	Oscillator input; one side of crystal input
3	XTAL2	Oscillator output; other side of crystal input
40	OSCEN	Oscillator enable input (Schmitt-Trigger input) A high signal enables oscillator to run A low signal stops oscillator and initializes standby mode
4	RESET	Input used to initialize processor (active low).
6	ĪNT	Interrupt input with internal pull-up resistor. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after reset. HALT mode is terminated by interrupt (active low).
8	RD/EA	Output strobe activated during a bus read. Can be used to enable transfer of data on the bus from an external device. Used as a read strobe to external data memory (active low). External access input which forces all program memory fetches to reference external memory. Active only during the initialization time (RESET at low)! (active low).
9	TO/PSEN	Input pin testable using the instructions JTO and JNTO until disabled through an execution of instructions SEL MBO or SEL MB1. Program store enable. This output is enabled through the first execution of instructions SEL MBO or SEL MB1. It can be disabled only through a new RESET initialization. It occurs only during a fetch to external program memory (active low).
10	WR/VER	Output strobe during a bus write. Used as write strobe to external data memory (active low). ROM verification input is low during the initialization time (RESET at low). The contents of the internal ROM can be read without program execution.

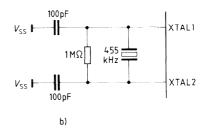
Pin No.	Symbol	Description
11	ALE	Address latch enable. This signal occurs once during each cycle and is useful as clock output. Negative edge of ALE strobes address into external data and program memory.
1219	DBODB7	True bidirectional port which can be written or read synchronously using WR, RD strobes. Contains the 8 low-order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of PSEN. Also contains the address and data during an external RAM data store instruction, under control of ALE, RD, and WR.
2124	P40P43	4-bit quasi-bidirectional port. Internal pull-up resistors. This port contains the four high order program-counter bits during an external program memory fetch.
5, 7,	P60P63	4-bit quasi-bidirectional port. Internal pull-up resistors.
25, 26		Keyboard wake-up capability mask-programmable.
2734	P10P17	8-bit quasi-bidirectional port. Internal pull-up resistors. Keyboard wake-up capability mask-programmable.
3538	P50P53	4-bit quasi-bidirectional port. Internal pull-up resistors. Keyboard wake-up capability mask-programmable.
39	Т1	Input pin testable using JT1, and JNT1 instructions. Can be designated as timer/counter input using the STRT CNT instruction.
1	$V_{ extsf{DD}}$	Power supply
20	$V_{\rm SS}$	Circuit GND potential (0 V)

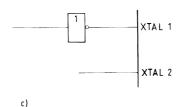


Oscillator

The on-board oscillator is a high-gain resonant circuit with a frequency range between 0 and 3 MHz. The clock frequency is determined by the resonator (e.g. crystal) connected between the pins XTAL1 and XTAL2.







8-bit timer/counter

The SAB 80 C 842 contains a timer/counter to aid the user in counting and generating accurate time delays without placing a burden on the processor for these functions.

Timer

Execution of a START T instruction connects an internal clock to the counter input. The XTAL frequency divided by 256 is the timer input frequency.

Counter

Execution of a START CNT instruction connects the T1 pin to the counter input and enables the counter. Subsequent high-to-low transition on T1 pin must be held low for at least one machine cycle to ensure it is not missed. The counter may be incremented only once throughout three instruction cycles. There is no minimum frequency limit.

Program memory

The resident program memory consists of 2048 bytes. There are three particulary important locations in program memory:

1. Location 0:

Executing the initialization reset causes the first instruction to be fetched from location 0.

2. Location 3:

Execution starts at location 3 after the interrupt input (pin 6) of the processor has gone low (if interrupt is enabled).

3. Location 7:

A timer/counter interrupt resulting from timer/counter overflow (if enabled).

Program memory configurations

1. Internal 2 Kbyte ROM

- pin 9 is available as T0 input
- port 4 serves only as I/O port

2. Internal 2 Kbyte ROM and additional, external 2 Kbyte ROM

- with external access, instruction words are read in via bus (data bus, DB).
- an SEL MB0 or an SEL MB1 instruction must be executed before using the data bus for external program store access.
- execution of SEL MB1 instruction followed by CALL or JMP enables exceeding internal 2 Kbyte limits and accessing of external ROM.
- external program memory access causes loading of program counter bits PC8 through PC11 at port lines 40 to 43. PC0 through PC7 appear on bus during the falling edge of ALE.
- execution of MOVP3 A, @ A instruction causes internal ROM (bank 0) to be selected.
- internal ROM is automatically selected during every execution of an interrupt service routine.
- in second cycle of MOVX instruction no PSEN signal appears and RD or WR signal is active. Port 4 is not affected.

3. External 4 Kbyte ROM, internal ROM disabled

- sole access to external 4 Kbyte ROM is initiated by logic 0 at pin 8 (RD/EA) during initialization time (RESET at low). At the machine cycle T8 test logic calls up status from pin 8.
- pin 9 serves as PSEN output.
- program counter bits PC0 through PC7 appear at DB0 through DB7 and PC8 through PC11 appear at port lines P40 through P43.
- execution of MOVP3 A,@A instruction or interrupt routine selects automatically lower 2 Kbytes of external ROM.

4. Internal ROM verification without program execution

- pin 10 (WR/VER) is tested at the machine cycle T8 during the initialization time (RESET at low). The low level at this pin forces the SAB 80 C 482 to the verification mode.
- contents of internal ROM appear on lines DB0 through DB7
- program-counter bits PC0 through PC7 appear at DB0 through DB7 and PC8 through PC11 at port lines P40 through P43.
- ALF and PSEN are enabled.

Reset

The reset signal sets the microcomputer to a defined initial state. There are two possibilities to reach this state.

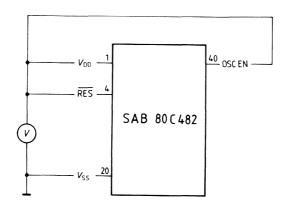
- 1. by an external signal at pin 4 (RESET)
- 2. by an internal signal generated through the built-in power-on-reset circuit.

If the oscillator is enabled (OSCEN at high), reset performs the following functions:

- 1. sets program counter to zero (PC = 000H)
- 2. sets stack pointer to zero (SP = 00H)
- 3. selects register bank 0
- 4. selects memory bank 0 (internal ROM)
- sets bus to high impedance state (except when RD/EA or WR/VER is at low)
- 6. sets ports 1, 4, 5, 6 to input mode
- 7. stops counter/timer
- 8. enables pin 9 as test input TO
- 9. disables interrupts
- 10. clears timer flag
- 11 releases HALT mode
- 12. does not affect internal RAM contents

Timing diagrams for power-on and external reset are shown in fig. a) and b).

Figure a) Internal power-on reset



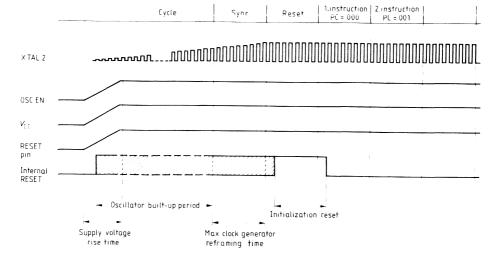
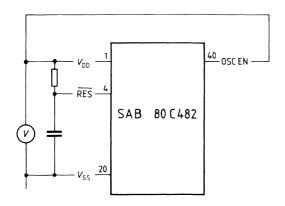
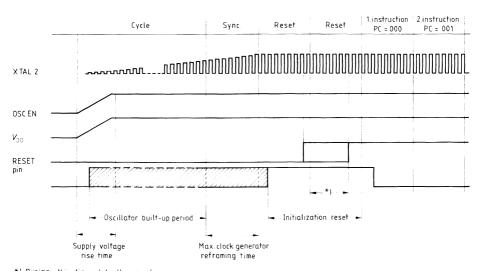


Figure b) External reset





^{*)} During this time-slot the signal at Reset-pin can change to $V_{\rm DD}$ without lengthening the Reset execution

Interrupt

The SAB 80 C 482 has the same interrupt logic as the SAB 8048. The interrupt can be initialized through two possible sources:

- 1. external low active signal at pin INT
- 2. overflow of the internal counter/timer.

Keyboard wake-up

The SAB 80 C 482 has a special on-chip circuitry for a convenient keyboard-scanning named "Keyboard wake-up". Four NAND gates can be connected to the ports P10–13, P14–17, P50–53 and P60–63 by mask programming. The outputs of these gates are interconnected in the NOR manner. The resulting output controls the release from the HALT mode.

This means, the SAB 80 C 482 can be "waked up" on any keystroke without the necessity of using a double contact keyboard.

HALT mode

After execution of the HALT instruction the processor enters the HALT mode where the internal clocks and internal logic are disabled. The oscillator is running. In the HALT mode, power consumption is about 1/3 of normal SAB 80 C 482 operation.

HALT mode can be released in three different ways:

- 1. by low pulse on the RESET pin (program starts at address location 0)
- via keyboard wake-up (program continues at address location PC+1)
- 3. by low pulse on the INT pin (if interrupt is enabled the interrupt subroutine starting at the address location 3 is executed. After its execution, or if interrupt is disabled, program continues at address location PC+1.)

Standby

Standby provides additional, drastic power consumption savings over the HALT mode.

Standby is initiated by forcing the OSCEN pin to low state. Oscillator operation is discontinued. While in standby, the following data is maintained:

- 1. internal RAM
- 2. stack pointer
- 3. program counter
- 4. memory bank status
- 5. TO/PSEN status
- 6. I/O status on all ports
- 7. all internal logic states

It is possible, but not recommended, to put the SAB 80 C482 on standby without regard to the running program. Stopping at any time in the instruction cycle can result in an undefined status. Consequently, it is advisable to enter standby only from the HALT state or if an external reset signal is applied. The RES pin must be forced at least 2.5 cycles earlier to the low level than the OSCEN pin.

If the SAB 80 C 482 has entered the standby from the HALT mode, it is still in the HALT mode after the OSCEN pin has been forced high. In the second case, the RES pin has to be held at least for the oscillator built-up period plus one cycle at low level after the OSCEN pin has been forced high.

Instruction set

There are five new instructions in addition to the SAB 8048 instruction set:

DEC	@ R0	instruction code	CO
DEC	@ R1	instruction code	C1
DJNZ	@ RO, addr	instruction code	EO
DJNZ	@ R1, addr	instruction code	E1
HALT		instruction code	F3

The following SAB 8048 instructions are not available:

IN	A, P2	instruction code	OA
MOVD	A, P7	instruction code	OF
OUTL	P2, A	instruction code	3A
MOVD	P7, A	instruction code	3F
ENTO	CLK	instruction code	75
JF1	addr	instruction code	76
CLR	FO	instruction code	85
ORL	P2, # data	instruction code	A8
ORLD	P7, A	instruction code	8F
CPL	F0	instruction code	95
ANL	P2, # data	instruction code	9A
ANLD	P7, A	instruction code	9F
CLR	F1	instruction code	A5
CPL	F1	instruction code	B5
JF0	addr	instruction code	B6
MOV	A, PSW	instruction code	C7
MOV	PSW, A	instruction code	D7

The opcode of the following instruction has been changed:

JNI addr instructio	n code 66	(8048 = 86)
---------------------	-----------	-------------

Symbols and abbreviations

	Accumulator
A	Accumulator
AC	Auxiliary carry
addr	Program memory address
An	Accumulator bit n
Bb	Bit designator b = 0 to 7
BS	Bank switch
BUS	Bus port
CY	Carry
CLK	Clock
CNT	Event counter
data	8-Bit number or expression
DBF	Memory bank flipflop
1	Interrupt
PC	Program counter
Pp	Port designator p = 4 to 6
P1	Port 1
PSW	Program status word
Ri	Register designator i = 0, 1
Rr	Register designator r = 0 to 7
SP	Stack pointer
T	Timer
TF	Timer/counter flag
TO/T1	Test 0, test 1
Χ	Mnemonic for external RAM
#	Immediate data prefix
@	Indirect address prefix
(X)	Contents of X
(X) ((X))	Contents of A
((^))	addressed by (X)
←	Is replaced by
\leftrightarrow	Is exchanged with
AND	Logical AND operation
OR	Logical OR operation
XOR	Logical EXOR operation

Mnemonic	Function	Description	Hex code	Flag	Bytes	Cycles
Accumulator and i	register move in	structions				
MOV A, Rr	(A) - (Rr)	Move register to accumulator	F8-FF		1	1
MOV A, @ Ri	(A) → ((Ri))	Move data memory to accumulator	FO-F1		1	1
MOV A, # data	(A) ← data	Move data to accumulator	23		2	2
MOV Rr, A	(Rr) + (A)	Move accumulator to register	A8-AF		1	1
MOV @ Ri, A	((Ri)) ← (A)	Move accumulator to data memory	A0-A1		1	1
MOV Rr, # data	(Rr) ← data	Move data to register	B8-BF		2	2
MOV @ Ri, # data	((Ri)) ← data	Move data to data memory	B0-B1		2	2
MOVX A, @ Ri	(A) ← ((Ri))	Move external data to accumulator	80-81		1	2
MOVX @ Ri, A	((Ri)) ← (A)	Move accumulator to external data memory	90-91		1	2
XCH A, Rr	(A) ↔ (R)	Exchange register and accumulator	28-2F		1	1
XCH A, @ Ri	(A) ↔ ((Ri))	Exchange data memory and accumulator	20-21		1	1
XCHD A, @ Ri	(A0−3) ↔ ((Ri0−3))	Exchange nibble of data memory and accumulator	30-31		1	1
MOVP3 A, @ A	save (PC) (PC0-7) ← (A) (PC8-11) ← 011 B (A) ←((PC)) restore PC	Move data from page 3 of program memory to accumulator	E3		1	2
MOVP A, @ A	save (PC) (PC0-7) ← (A) (A) ← ((PC)) restore PC	Move data from current page of program to accumulator	А3		1	2
SWAP A	(A4-7) ↔ (A0-3)	Exchange accumulator nibbles	47		1	1

Mnemonic	Function	Description	Hex code	Flag	Bytes	Cycles
Timer/counter m	ove instructions					
MOV A, T	(A) ← (T)	Read counter/timer into accumulator	42		1	1
MOV T, A	(T) ← (A)	Load counter/timer from accumulator	62	4.470.77	1	1
Port move instru	ctions					
IN A, P1	(A) ← (P1)	Move data at port 1 to accumulator	09		1	2
OUTL P1, A	(P1) ← (A)	Output accumulator on port 1	39		1	2
ANL P1, # data	(P1) ← (P1) AND data	Logical AND port 1 with data	99		2	2
ORL P1, # data	(P1) ← (P1) OR data	Logical OR port 1 with data	89		2	2
IN A, BUS	(A) ← (BUS)	Move data on bus to accumulator	08		1	2
OUTL BUS, A	(BUS) ← A	Output accumulator on bus	02		1	2
ANL BUS, # data	(BUS) ← (BUS) AND data	Logical AND bus with data	98		2	2
ORL BUS, # data	(BUS) ← (BUS) OR data	Logical OR bus with data	88		2	2
MOVD A, Pp	(A0−3) ← (Pp) (A4−7) ← 0	Move data at port 4 – 6 to accumulator	OC-OE		1	2
MOVD Pp, A	(Pp) ← (A0-3)	Output accumulator on port 4 – 6	3C-3E		1	2
ANLD Pp, A	(Pp) ← (A0-3) AND (Pp)	Logical AND accumulator with port 4 – 6	9C-9E		1	2
ORLD Pp, A	(Pp) ← (A0-3) OR (Pp)	Logical OR accumulator with port 4 – 6	8C-8E		1	2

Mnemonic	Function	Description	Hex code	Flag	Bytes	Cycles
Arithmetic accun	nulator instructio	ns				
ADD A, Rr	(A) + (A) + (Rr)	Add register to accumulator	68-6F	AC CY	1	1
ADD A, @ Ri	(A) ← (A) + ((Ri)	Add data memory to accumulator	60-61	AC CY	1	1
ADD A, # data	(A) + (A) + data	Add data to accumulator	03	AC CY	2	2
ADDC A, Rr	(A) + (A) + (Rr) + (CY)	Add register and carry to accumulator	78-7F	AC CY	1	1
ADDC A, @ Ri	(A) + (A) + ((Ri)) + (CY)	Add data memory and carry to accumulator	70-71	AD CY	1	1
ADDC A, # data	(A) ← (A) + data + (CY)	Add data and carry to accumulator	13	AC CY	2	2
INC A	(A) · (A) + 1	Increment accumu- lator by 1	17		1	1
DEC A	(A) ← (A) – 1	Decrement accumulator by 1	07		1	1
DA A		Decimal adjust accumulator	57	AC CY	1	1
Arithmetic regist	er instructions					
INC Rr	(Rr) ← (Rr) + 1	Increment register by 1	18-1F		1	1
DEC Rr	(Rr) ← (Rr) – 1	Decrement register by 1	C8-CF		1	1
DEC @ Ri	((Ri)) ← ((Ri)) + 1	Decrement data memory by 1	C0-C1		1	1
INC @ Ri	((Ri)) ← ((Ri)) + 1	Increment data memory by 1	10-11		1	1
DJNZ Rr, addr	(Rr) ← (Rr) – 1 if (Rr) ≠ 0 (PCO-7)←addr	Decrement register by 1 and jump if register not zero	E8-EF		2	2
OJNZ @ Ri, addr	((Ri)) ← ((Ri)) – 1 if ((Ri)) ‡ 0 (PCO-7)←addr	Decrement data memory by 1 and jump if data memory is not zero	E0-E1		2	2

Mnemonic	Function	Description	Hex code	Flag	Bytes	Cycles
Logical accumul	ator and register i	nstructions				
ANL A, Rr	(A) ← (A) AND (Rr)	Logical AND accumulator with register	58-5F		1	1
ANL A, @ Ri	(A) ← (A) AND ((Ri))	Logical AND accumulator with data memory	50-51		1	1
ANL A, # data	(A) ← (A) AND data	Logical AND accumulator with data	53		2	2
ORL A, Rr	(A) ← (A) OR (Rr)	Logical OR accumulator with register	48–4F		1	1
ORL A, @ Ri	(A) ← (A) OR ((Ri))	Logical OR accumulator with data memory	40–41		1	1
ORL A, # data	(A) ← (A) OR data	Logical OR accumulator with data	43		2	2
XRL A, Rr	(A) ← (A) XOR (Rr)	Logical XOR accumulator with register	D8-DF		1	1
XRL A, @ Ri	(A) ← (A) XOR ((Ri))	Logical XOR accumulator with data memory	D0-D1		1	1
XRL A, # data	(A) ← (A) XOR data	Logical XOR accumulator with data	D3		2	2
CLR A	(Δ) ← 0	Clear accumulator	27		1	1
CPL A	$(A) \leftarrow (\overline{A})$	Complement accumulator	37		1	1

Mnemonic	Function	Description	Hex code	Flag	Bytes	Cycles
Rotate instruct	ions					
RL A	(An + 1) ← (An)	Shift accumulator 1 bit to left	E7		1	1
RLC A	(An + 1) ← (An) (CY) ← (A7) (A0) ← (CY)	Shift accumulator 1 bit to left through carry	F7	CY	1	1
RR A	(An) ← (An + 1)	Shift accumulator 1 bit to right	77		1	1
RRC A	(An) ← (An + 1) (CY) ← (A0) (A7) ← (CY)	Shift accumulator 1 bit to right through carry	67	CY	1	1
Flag instruction	ıs					
CLR C	(CY) ← 0	Clear carry bit	97	CY	1	1
CPL C	(CY) ← (C Y)	Complement carry bit	Α7	CY	1	1

Mnemonic	Function	Description	Hex code	Flag	Bytes	Cycles
Branch instruc	ctions					
JMP addr	(PCO-7) ← addr O-7 (PC8-10) ← addr 8-10 (PC11) ← DBF	Jump to address, page 0 1 2 3 4 5 6	04 24 44 64 84 A4 C4		2 2 2 2 2 2 2 2 2 2	2 2 2 2 2 2 2 2 2 2
JMPP @ A	(PCO-7) ← ((A))	Jump to address defined in program memory	В3		1	2
JC addr	if (CY) = 1 (PCO-7) ← addr	Jump to address if carry = 1	F6		2	2
JNC addr	if (CY) = 0 (PCO-7) ← addr	Jump to address if carry = 0	E6		2	2
JZ addr	if (A) = 0 (PCO-7) ← addr	Jump to address if accumulator = 0	C6		2	2
JNZ addr	if (A) > 0 (PC0-7) ← addr	Jump to address if accumulator > 0	96		2	2
JTO addr	if T0 = 1 (PC0-7) ← addr	Jump to address if TO is High	36		2	2
JNTO addr	if T0 = 0 (PC0-7) ← addr	Jump to address if TO is Low	26		2	2
JT1 addr	if T1 = 1 (PC0-7) ← addr	Jump to address if T1 is High	56		2	2
JNT1 addr	if T1 = 0 (PC0-7) ← addr	Jump to address if T1 is Low	46		2	2
JTF addr	if TF = 1 (PCO-7) ← addr (TF) ← 0	Jump to address if counter/timer flag = 1	16	TF	2	2
JNI addr	if INT = 0 (PCO-7) ← addr	Jump to address if interrupt input Low	66		2	2
JBb addr	if (An) = 1 (PCO-7) ← addr	Jump to address, n=0 if bit n of 1 accumulator = 1 2 3 4 5 6 7	12 32 52 72 92 B2 D2 F2		2 2 2 2 2 2 2 2 2 2	2 2 2 2 2 2 2 2 2 2

Mnemonic	Function	Description	Hex code	Flag	Bytes	Cycles
Subroutine inst	ructions					
CALL addr	((SP)) · (PCO-11, PSW4-7) (SP) · (SP)+1 (PCO-10) · addr O-10 (PC11) · DBF	Jump to page 0 subroutine 1 2 3 4 5 6 7	14 34 54 74 94 B4 D4 F4		2 2 2 2 2 2 2 2 2 2	2 2 2 2 2 2 2 2 2
RET	(SP) · (SP) – 1 (PC) · ((SP))	Return without PSW Restore	83		1	2
RETR	(SP) ← (SP) – 1 (PC) ← ((SP)) (PSW4–7) ← ((SP))	Return with PSW Restore	93	CY AC DBF	1	2

Mnemonic	Function	Description	Hex code	Flag	Bytes	Cycles
Control instruct	ions					
STRT T		Start timer	55		1	1
STRT CNT		Start counter	45		1	1
STOP TCNT		Stop timer/counter	65		1	1
EN TCNTI		Enable timer/ counter interrupt	25		1	1
DIS TCNTI		Disable timer/ counter interrupt	35		1	1
EN I		Enable external interrupt	05		1	1
DIS I		Disable external interrupt	15		1	1
SEL RB0		Select register bank 0	C5	BS	1	1
SEL RB1		Select register bank 1	D5	BS	1	1
SEL MB0		Select program- memory bank 0	E5	DBF	1	1
SEL MB1		Select program- memory bank 1	F5	DBF	1	1
NOP		No operation	00		1	1
HALT		HALT instruction	F3		1	1

Maximum ratings

Ambient temperature under bias	\mathcal{T}_{amb}	0 to 70	°C
Storage temperature	$\mathcal{T}_{ ext{stg}}$	-55 to 125	°C
Supply voltage ref. to GND ($V_{\rm SS}$)	$V_{ exttt{DD}}$	0 to 7	V
Total power dissipation	$P_{ m tot}$	1	w
All input and output voltages		-0.3 to $V_{\rm DD}$	V

DC characteristics

 $T_{\rm amb}$ = 0 to 70°C; $V_{\rm DD}$ = 2.5 to 6 V; $V_{\rm SS}$ = 0 V

		Test conditions	Min.	Тур.	Max.	1
L input voltage (all except XTAL1, XTAL2, RESET)	V_{IL}		-0.1		0.75	٧
L input voltage (XTAL1, XTAL2, RESET)	$oldsymbol{V_{IL1}}{oldsymbol{V_{IL1}}}$	V _{DD} < 4.5 V	-0.1		0.75 0.25	V
H input voltage (all except XTAL1, XTAL2, RESET	V_{IH}		0.7x V _{DD}		V_{DD}	V
H input voltage (XTAL1, XTAL2, RESET	$V_{\text{IH }1}$		0.7x V _{DD}		V_{DD}	V
L output voltage (BUS, RD, WR, PSEN, ALE)	$V_{\rm OL}$	$I_{OL} = 1.0 \text{ mA}$			0.45	V
Loutput voltage (all other outputs)	$V_{\text{OL}1}$	$I_{OL} = 1.0 \text{ mA}$			0.45	V
H output voltage (BUS, RD, WR, PSEN, ALE)	V_{OH}	$I_{OH} = 1.0 \text{ mA}$	0.75x V _{DD}			V
H output voltage; low impedance (all other outputs), high impedance	$V_{ m OH1} \ V_{ m OH1}$	$I_{OH} = 1 \text{ mA}$ $I_{OH} = 1 \mu\text{A}$	0.75x V _{DD} 0.75x V _{DD}			V
Input leakage current (Port1, 4, 5, 6) Input leakage current (RESET, T1) Input leakage current (INT; pullup) Input current XTAL	I_{ILP} I_{ILC} I_{IL}	$ \begin{vmatrix} V_{\text{IN}} \leq V_{\text{IL}} \\ V_{\text{SS}} \leq V_{\text{IN}} \leq V_{\text{DD}} \\ V_{\text{IN}} = V_{\text{DD}} \\ V_{\text{IN}} \leq V_{\text{IL}} \\ V_{\text{SS}} \leq V_{\text{IN}} \leq V_{\text{DD}} \end{vmatrix} $			-5 ±1 +1 -5 ±10	74 74 74 74 74
Output leakage current (For bus and TO in high-impedance states)	I_{OL}	$V_{\rm IN} \leq V_{\rm IL}$			±1	μA
Total supply current	I_{DD}	1 MHz; 5 V 3 MHz; 5 V 500 kHz; 5 V		1.2 4.2 0.9	1.4	mA mA
HALT supply current	I_{DD}	1 MHz; 5 V 3 MHz; 5 V 500 kHz; 5 V		550 250	400	дА Д Д
Power-down mode	I_{DD}	5 V		1	2	μA
Operation supply voltage	$V_{\scriptscriptstyle m DD}$		2.5		6	v
Data retention voltage	$V_{ exttt{DD}}$		1.2		6	V

AC characteristics

 $T_{\rm amb}$ = 0 to 70°C; $V_{\rm DD}$ = 5 V; $V_{\rm SS}$ = 0 V; $f_{\rm OSC}$ = 3 MHz $C_{\rm L}$ = 40 pF

		Test conditions	Min.	Тур.	Max.	
ALE pulse width	$t_{\sf LL}$		800	833		ns
Address set-up before ALE	t_{AL}		120	166		ns
Address hold from ALE	t_{LA}		0		160	ns
Control pulse width			200	000		
PSEN RD, WR	$t_{ m CC} \ t_{ m CC}$		300 1300	333 1333		ns
Data set-up before WR	$t_{\sf DW}$		1300	1333		ns
Data hold after WR	t_{WD}	$t_{\rm CY} = 2.66 \ \mu s$ $C_{\rm L} = 40 \ \rm pF$	300	333		ns
Cycle time	t_{CY}		2.66			μs
Data hold after RD Instr. hold after PSEN	$t_{ m DR} \ t_{ m DR}$		0		300 300	ns ns
RD to data in	t_{RD}				1200	ns
PSEN to data in	t_{RD}				300	ns
Address set-up before WR	t_{AW}		2000			ns
Address set-up to data						
at RD	t_{AD}		3500			ns
at PSEN	t_{AD}		500			ns
Address float to						
RD PSEN	$t_{AFC} \ t_{AFC}$		166 140	333 166		ns ns
WR to ALE	t_{CA}		140	333		ns
PSEN to ALE	t_{CA}			1333		ns
ALE to RD	t_{CA}		0		50	ns
ADDRESS Time Port 4	t_{ADD}			666		ns

Time parameters versus $f_{\rm OSC}$

Symbol	Parameter	
t	1/f _{OSC}	μs
t _{CY}	8 <i>t</i>	μs

Read from external data memory

$\overline{t_{\text{LL}}}$	2.5 t	μs
t_{CA}	_	μs
t_{AFC}	1.0 <i>t</i>	μs
$t_{\rm CC}$	4.0 <i>t</i>	μs
t_{DR}	_	μs
t_{RD}	3.5 <i>t</i>	μs
t _{AD}	10.5 <i>t</i>	μs

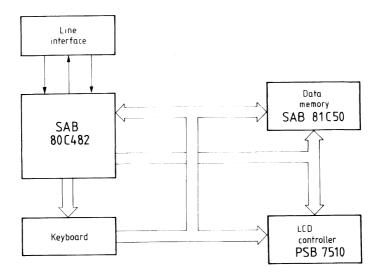
Write into external data memory

t_{CA}	1.0 t	μs	
$t_{\rm CC}$	4.0 t	μs	
t_{WD}	1.0 <i>t</i>	μs	
$t_{\sf DW}$	4.0 t	μs	
t _{AW}	6.0 <i>t</i>	μs	

Instruction fetch from external program memory

t_{AL}	0.5 t	μs
$t_{\sf CA}$	4.0 t	μs
t_{LA}	_	μs
$t_{\rm CC}$	1.0 <i>t</i>	μs
t_{DR}	-	μs
t_{RD}	0.5 t	μs
t_{AD}	1.5 <i>t</i>	μs
t_{ADD}	2.0 t	μs
t _{AFC}	0.5 <i>t</i>	μs

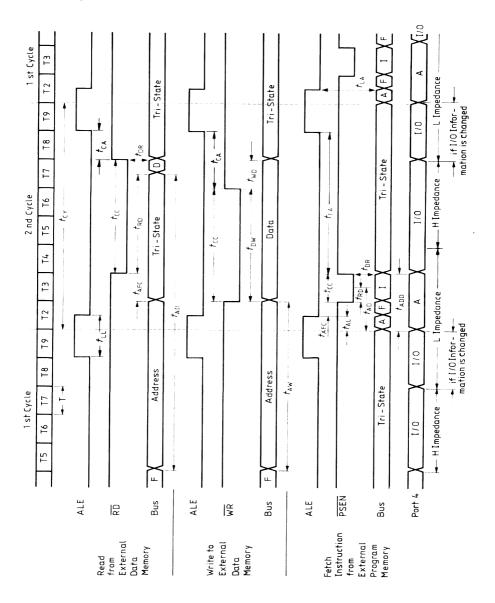
Application example "Intelligent Telephone Set"

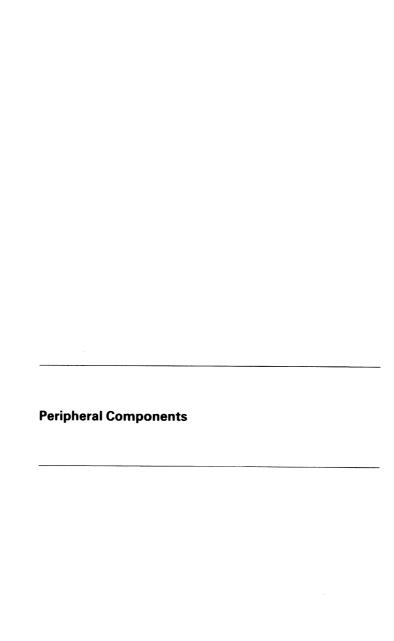


Features of this telephone set

- direct and indirect redialing
- short dialing (10 memories)
- auto dialing by special keys
- babysitter function
- LC-display control
- electronic keylock
- clock function
- rate signaling

Pulse diagram SAB 80 C482





SAB 179X Floppy Disk Formatter/ Controller Family

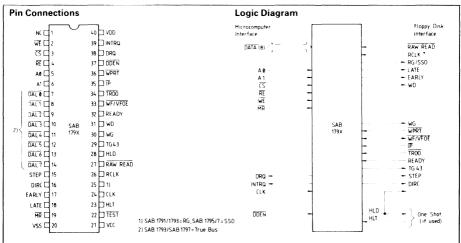
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- Two VFO Control Signals -RG & VFOE
- Soft Sector Format Compatibility
- Automatic Track Seek with Verification
- IBM 3740 Single Density (FM)
 IBM System 34 Double Density (MFM)

 Read Mode
- Read Mode
 Single/Multiple Sector Read with Automatic
 Search or Entire Track Read
 Selectable 128 Byte or Variable length Sector

Accomodates Single and Double Density Formats

- Write Mode
 Single/Multiple Sector Write with Automatic
 Sector Search
 Entire Track Write for Diskette Formatting
- System Compatibility
 Double Buffering of Data 8 Bit Bi-Directional
 Bus for Data, Control and Status
 DMA or Programmed Data Transfers
 All Inputs and Outputs are TTL Compatible
 On-Chip Track and Sector Registers/Comprehensive Status Information
- Programmable Controls
 Selectable Track to Track Stepping Time
 Side Select Compare
- Write Precompensation
- Window Extension
- Incorprorates Encoding/Decoding and Address Mark Circuitry
- For 8" and 514"
 Floppy Disks
- Compatible with Industry Standard 179X



SAB 179X is a floppy disk controller family of N-channel MOS LSI components designed to interface with SAB 8080/8085/8086/8051 family

processors. Its flexibility and ease of use makes it an ideal floppy disk interface between conventional floppy disks and all computer systems.

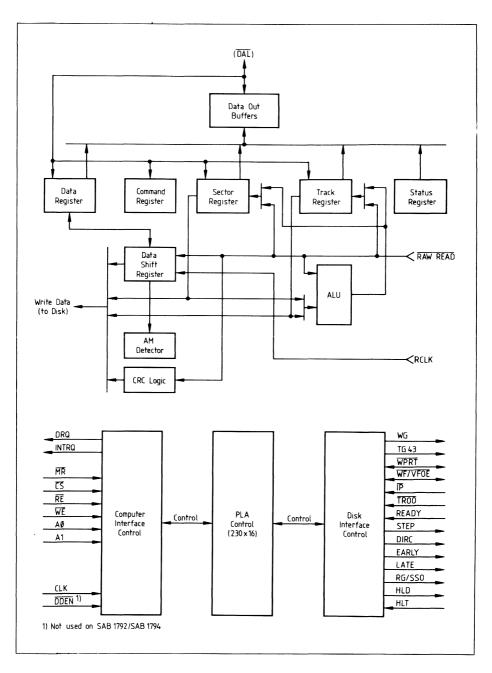
Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function			
NC	1	-	NO CONNECTION – Pin 1 is internally connected to a back bias generator and must be left open by the user.			
MR	19	1	MASTER RESET — A logic low (50μs min.) on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during MR ACTIVE. When MR is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into sector register.			
WE	2	1	$ \overline{\text{WRITE ENABLE}} - \text{A logic low on this input gates data on the DAL} \\ \text{into the selected register when } \overline{\text{CS}} \text{ is low}. $			
CS	3	_	CHIP SELECT – A logic low on this input selects the chip and enables computer communication with the device.			
RE	4		READ ENABLE – A logic low on this input controls the placement of data from a selected register on the DAL when CS is low.			
AØ, A1	5,6	I	REGISTER SELECT LINES – These inputs select the register to receive/transfer data on the DAL lines under RE and WE control: CS A1 A0 RE WE 0 0 0 Status Reg Command Reg 0 0 1 Track Reg Track Reg 0 1 0 Sector Reg Sector Reg 0 1 1 Data Reg Data Reg			
DALØ to DAL7	7 to 14	1/0	DATA ACCESS LINES — Eight bit inverted (SAB 1791/5) or true (SAB 1793/7) bidirectional bus used for transfer of data, control, and status. This bus is receiver enabled by WE or transmitter enabled by RE. Drive capability is 1 TTL Load			
CLK	24	ı	CLOCK – This input requires a free-running square wave clock for internal timing reference. 2 MHz \pm 1% with 50% duty cycle. 1 MHz \pm 1% for mini-floppies.			
DRQ	38	0	DATA REQUEST – This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operations, respectively. Use 10K pull-up resistor to +5V.			
INTRQ	39	0	INTERRUPT REQUEST – This open drain output is set at the completion of any command and is reset when the STATUS register is read or the command register is written to. Use 10K pull-up resistor to +5V.			
STEP	15	0	STEP – The step output contains a pulse for each step.			
DIRC	16	0	DIRECTION – Direction Output is active high when stepping in active low when stepping out.			
EARLY	17	0	EARLY – Indicates that the WRITE DATA pulse occurring while Early is active (high) should be shifted early for write precompensation.			
LATE	18	0	LATE – Indicates that the write data pulse occuring while Late is active (high) should be shifted late for write precompensation.			

		Input (I) Output (O)	Function			
TEST	22	1	TEST – This input is used for testing purposes only and should be tied to +5V or left open by the user unless interfacing to voice coil actuated motors.			
HLT	23	1	HEAD LOAD TIMING – When a logic high is found on the H input the head is assumed to be engaged.			
RG	25	0	READ GATE (SAB 1791/3) – A high level on this output indicates to the data separator circuitry that 2 bytes of zeros in single density, or 4 bytes of either zeros or ones in double density have been encountered, and is used for synchronization.			
SSO	25	0	SIDE SELECT OUTPUT (SAB 1795/1797) — The logic level of the Side Select Output is directly controlled by the ,S' flag in Type II or III commands. When U = 1, SSO is set to a logic 1. When U = 0, SSO is set to a logic 0. The SSO is compared with side information in the sector ID field. If they do not compare, status bit 4 (RNF) is set. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition.			
RCLK	26	1	READ CLOCK – A nominal square-wave clock signal derived from the data stream must be provided to this input. Phasing (i. e. RCLK transitions) relative to RAW READ is important but polarity (RCLK high or low) is not.			
RAW READ	27	1	RAW READ – The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.			
HLD	28	0	HEAD LOAD – The HLD output controls the loading of the Read-Write head against the media.			
TG43	29	0	TRACK GREATER THAN 43 – This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands.			
WG	30	0	WRITE GATE – This output is made valid before writing is to be performed on the diskette.			
WD	31	0	WRITE DATA – A 200 ns (MFM) or 500 ns (FM) output pulse flux transition. WD contains the unique Address marks as was data and clock in both FM and MFM formats.			
READY	32	-	READY – This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.			

Pin Definitions and Functions (continued)

Symbol	Number	Input (I) Output (O)	Function		
WF/VFOE	33	1/0	WRITE FAULT VFO ENABLE — This is a bidirectional signal used to signify writing faults at the drive, and to enable the external PLO data separator. When WG = 1, Pin 33 functions as a WF input. If WF = 0, any write command will immediately be terminated. When WG = 0, Pin 33 functions as a VFOE output. VFOE will go low during a read operation after the head has loaded and settled (HLT = 1). On the SAB 1795/7, it will remain low until the last bit of the second CRC byte in the ID field. VFOE will then go high until 8 bytes (MFM) or 4 bytes (FM) before the Address Mark. It will then go active until the last bit of the second CRC byte of the Data Field. On the SAB 1791/3, VFOE will remain low until the end of the Data Field. This pin has an internal 100 kOhm pull-up resistor.		
TRØØ	34	1	TRACK 00 – This input informs the SAB 179X that the Read/ Write head is positioned over Track 00.		
IP	35	1	NDEX PULSE – This input informs the SAB 179X when the index hole is encountered on the diskette		
WPRT	36	I	WRITE PROTECT – This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.		
DDEN	37	1	DOUBLE DENSITY – This pin selects either single or double density operation. When DDEN = 0, double density is selected. When DDEN = 1, single density is selected.		
VCC	21	-	POWER SUPPLY (+5 V).		
VDD	40	-	POWER SUPPLY (+12 V).		
VSS	20	-	GROUND (0 V)		



General Description

The SAB 179X are MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The SAB 179X is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation.

The processor interface consists of an 8-bit bidirectional bus for data, status, and control word

transfers. The SAB 179X is set up to operate on a multiplexed bus with other bus-oriented devices. The SAB 179X is fabricated in N-channel Silicon Gate MOS technology and is TTL compatible on all inputs and outputs. The SAB 1793 is identical to the SAB 1791 except the DAL lines are TRUE for systems that utilize true data busses. The SAB 1795/7 has a side select output for controlling double sided drives.

Organization

The Floppy Disk Formatter block diagram is illustrated on previous page. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register – This 8-bit register assembles serial data from the Read Data input (RAW READ) during Read operations and transfers serial data to the Write Data output during Write operations. Data Register - This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operation information is transferred in parallel from the Data Register to the Data Shift Register. When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control. Track Register – This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

Sector Register (SR) – This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) – This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR) – This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic – This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

The CRC includes al! information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) – The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control – All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

The SAB 179X has two different modes of operation according to the state of \overline{DDEN} . When $\overline{DDEN}=\emptyset$ double density (MFM) is assumed. When $\overline{DDEN}=1$, single density (FM) is assumed.

AM Detector – The address mark detector detects ID, data and index address marks during read and write operations.

Processor Interface

The interface to the processor is accomplished through the eight Data Access Lines (\overline{DAL}) and associated control signals. The \overline{DAL} are used to transfer Data, Status, and Control words out of, or into the SAB 179X. The \overline{DAL} are three state buffers that are enabled as output drivers when Chip Select (\overline{CS}) and Read Enable (\overline{RE}) are active (low logic state) or act as input receivers when \overline{CS} and Write Enable (\overline{WE}) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and \overline{CS} is made low. The address bits A1 and A0, combined with the signals \overline{RE} during a Read operation or \overline{WE} during a Write operation are interpreted as selecting the following registers:

A1-A0	READ (RE)	WRITE (WE)
00,	Status Register	Command Register
Ø 1	Track Register	Track Register
1 Ø	Sector Register	Sector Register
1 1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the SAB 179X and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data

transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the Status Register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

Because of internal sync cycles, certain time delays must be observed when operating under programmed I/O. They are:

			Delay Req'd. ¹⁾		
Operation	Next Operation	FM	MFM		
Write to Command Reg.	Read Busy Bit (Status Bit 0)	12 μs	6 μs		
Write to Command Reg.	Read Status Bits 1-7	28 μs	14 μs		
Write Any Register	Read From Diff. Register	Ø	Ø		

¹⁾ Times double for CLK=1MHz (Minifloppies)

Floppy Disk Interface

The SAB 179X has two modes of operation according to the state of \overline{DDEN} (Pin 37). When $\overline{DDEN}=1$, single density is selected. In either case, the CLK input (Pin 24) is at 2 MHz. However, when interfacing with the mini-floppy, the CLK input is set at 1 MHz for both single density and double density. When the clock is at 2 MHz, the stepping rates of 3, 6, 10, and 15 ms are obtainable. When CLK equals 1 MHz these times are doubled.

Head Positioning

Five commands cause positioning of the Read-Write head (see Command Section). The period of each positioning step is specified by the r field in bits 1 and 0 of the command word. After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock.If $\overline{\text{TEST}} = \emptyset$, there is zero settling time. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.

The rates can be applied to a Step-Direction Motor through the device interface.

Step – A 2 μ s (MFM) or 4 μ s (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output. **Direction (DIRC)** – The Direction signal is active

Direction (DIRC) – The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12μ s before the first stepping pulse is generated.

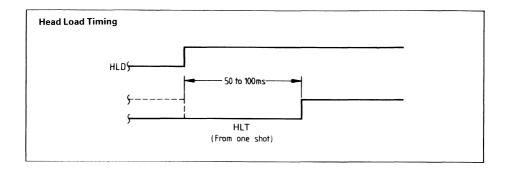
When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register, If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. The SAB 179X must find an ID field with correct track number and correct CRC within 5 revolutions of the media: otherwise the seek error is set and an INTRQ is generated.

Stepping Rates

CLK	2 MHz	2 MHz	1 MHz	1 MHz	2 MHz	1 MHz
DDEN	Ø	1	Ø	1	x	x
R1 RØ	TEST = 1	TEST=1	TEST=1	TEST=1	TEST=0	TEST=0
R1 Ø Ø Ø 1 1 Ø 1 1	3 ms 6 ms 10 ms 15 ms	3 ms 6 ms 10 ms 15 ms	6 ms 12 ms 20 ms 30 ms	6 ms 12 ms 20 ms 30 ms	184 μs 190 μs 198 μs 208 μs	368 μs 380 μs 396 μs 416 μs

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the verify flag (V = 1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h = 0 and V = 0); or if the SAB 179X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load Timing (HLT) is an input to the SAB 179X which is used for the head engage time. When HLT = 1, the SAB 179X assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the SAB 179X.



When both HLD and HLT are true, the SAB 179X will then read from or write to the media. The "and" of HLD and HLT appears as a status bit in Type I status.

In summary for the Type I commands: if $h=\emptyset$ and $V=\emptyset$, HLD is reset. If h=1 and $V=\emptyset$, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay. If $h=\emptyset$ and V=1, HLD is set near the end of the command, an internal 15 ms occurs, and the SAB 179X

waits for HLT to be true. If h=1 and V=1, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the SAB 179X then waits for HLT to occur. For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

General Disk Read Operations

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, DDEN should be placed to logical "1." For MFM formats, DDEN should be placed to a logical "0." Sector lengths are determined at format time by the fourth byte in the "ID" field.

Sector Len	gth Table*)
Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
Ø1 Ø2	256 512
Ø 3	1024

^{*)} SAB 1795/97 may vary - see command summary.

The number of sectors per track as far as the SAB 179X is concerned can be from 1 to 255 sectors.

The number of tracks as far as the SAB 179X is concerned is from Ø to 255 tracks. For read operations in 8" double density the SAB 179X requires RAW READ Data (Pin 27) signal which is a 200 ns pulse per flux transition and a Read clock (RCLK) signal to indicate flux transition spacings. The RCLK (Pin 26) signal is provided by some drives but if not it may be derived externally by Phase locked loop, one shots, or counter technigues. In addition a Read Gate Signal is provided as an output (Pin 25) on SAB 1791/93 which can be used to inform phase lock loops when to acquire synchronization. When reading from the media in FM. RG is made true when 2 bytes of zeroes are detected. The SAB 179X must find an address mark within the next 10 bytes; otherwise RG is reset and

Similarly for MFM, RG is made active when 4 bytes of "00" or "FF" are detected. The SAB 179X must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes. During read operations (WG = 0), the VFOE (Pin 33)

the search for 2 bytes of zeroes begins all over

any useful information from the data stream.

again. If an address mark is found within 10 bytes,

RG remains true as long as the SAB 179X is deriving

is provided for phase lock loop synchronization.

VFOE will got active low when:

- a) Both HLT and HLD are True
- b) Settling Time, if programmed, has expired
- c) The SAB 179X is inspecting data off the disk If WF/VFOE is not used, this pin may be left open, as it has an internal pull-up resistor.

General Disk Write Operations

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the SAB 179X before the Write Gate signal can be activated. Writing is inhibited when the Write Protect input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The Write Fault input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the SAB 179X terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The Write Fault input should be made inactive when the Write Gate output becomes inactive.

For write operations, the SAB179X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of 500 ns pulses in FM ($\overline{DDEN}=1$) and 200 ns pulses in MFM ($\overline{DDEN}=\emptyset$). Write Data provides the unique address marks in both formats.

Also during write, two additional signals are provided for write precompensation. These are EARLY (Pin 17) and LATE (Pin 18). EARLY is active true when the WD pulse appearing on (Pin 30) is to be written EARLY. LATE is active true when the WD pulse is to be written LATE. If both EARLY and LATE are low when the WD pulse is present, the WD pulse is to be written at nominal. Since write precompensation values vary from disk manufacturer to disk manufacturer, the actual value is determined by several one shots or delay lines which are located external to the SAB 179X. The write precompensation signals EARLY and LATE are valid for the duration of WD in both FM and MFM formats.

Ready

Whenever a Read or Write command (Type II or III) is received the SAB 179X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated.

Command Description

The SAB 179X accepts eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is

reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types.

Commands and types are summarized on next page.

Status Register

Upon receipt of any command, except, the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The user has the option of reading the status register through program control or using the DRQ line with DMA or interrupt methods. When the Data register is read the DRQ bit in the status register and the DRQ line are automatically reset. A write to the Data register also causes both DRQ's to reset.

The busy bit in the status may be monitored with a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a busy status check is not recommended because a read of the status register to determine the condition of busy will reset the INTRQ line.

	The first the second se		(B	its)			
7	6	5	4	3	2	1	Ø
S 7	S6	S5	S4	S3	S2	S1	SØ

Status varies according to the type of command executed.

Command Summary

	Commands for SAB 1791, SAB 1793						Con	nma	nds	for S.	AB 1	795,	SAE	1797			
						3its							В	its			
Туре	Command	7	6	5	4	3	2	1	Ø	7	6	5	4	3	2	1	Ø
1	Restore	Ø	Ø	Ø	Ø	h	٧	r ₁	rø	Ø	Ø	Ø	Ø	h	٧	r ₁	rø
1	Seek	Ø	Ø	Ø	1	h	V	r_1	rø	Ø	Ø	Ø	1	h	V	r_1	rø
1	Step	Ø	Ø	1	T	h	V	r_1	rø	Ø	Ø	1	T	h	V	\mathbf{r}_1	rø
- 1	Step-in	Ø	1	Ø	Т	h	V	r ₁	rø	Ø	1	Ø	Т	h	V	r_1	rø
- 1	Step-out	Ø	1	1	T	h	V	\mathbf{r}_1	rø	Ø	1	1	Т	h	V	\mathbf{r}_1	rø
H	Read Sector	1	Ø	Ø	m	S	Ε	С	Ø	1	Ø	Ø	m	L	Ε	U	Ø
11	Write Sector	1	Ø	1	m	S	Ε	С	aø	1	Ø	1	m	L	Ε	U	аø
Ш	Read Address	1	1	Ø	Ø	Ø	Ε	Ø	Ø	1	1	Ø	Ø	Ø	Ε	U	Ø
Ш	Read Track	1	1	1	Ø	Ø	Ε	Ø	Ø	1	1	1	Ø	Ø	Ε	U	Ø
111	Write Track	1	1	1	1	Ø	Ε	Ø	Ø	1	1	1	1	Ø	Ε	U	Ø
IV	Force Interrupt	1	1	Ø	1	13	I_2	I_1	l _o	1	1	Ø	1	I_3	I_2	1,	lø

Flag Summary

Command Type	Bit No(s)		Description
	Ø, 1	r₁ r₀ = Stepping Motor Rate	
1	2	V = Track Number Verify Flag	V = Ø, No verify V = 1, Verify on destination track
1	3	h = Head Load Flag	h = 0, Unload head at beginning h = 1, Load head at beginning
1	4	T = Track Update Flag	T = 0, No update T = 1, Update track register
II & III	Ø	$a_{\emptyset} = Data Address Mark$	$a_{\emptyset} = \emptyset$, FB (DAM) $a_{\emptyset} = 1$, F8 (deleted DAM)
II	1	C = Side Compare Flag	C = Ø, Disable side compare C = 1, Enable side compare
II & III	1	U = Update SSO	U = 0, Update SSO to 0 U = 1, Update SSO to 1
II & III	2	E = 15 ms Delay	E = 0, No 15 ms delay E = 1, 15 ms delay
11	3	S = Side Compare Flag	S = 0, Compare for side 0 S = 1, Compare for side 1
11	3	L = Sector Length Flag	
		L = 1 (implicit) for SAB 1791/3	LSB's Sector Length in ID Field
			L = 0 256 512 1024 128
			L = 1 128 256 512 1024
11	4	m = Multiple Record Flag	m = Ø, Single record m = 1, Multiple records
IV	Ø-3	$\begin{array}{ll} l_x &= \text{Interrupt Condition Flags} \\ l_0 &= 1 \text{ Not Ready To Ready Transi} \\ l_1 &= 1 \text{ Ready To Not Ready Transi} \\ l_2 &= 1 \text{ Index Pulse} \\ l_3 &= 1 \text{ Immediate Interrupt, Requi} \\ l_3 - l_1 &= 0 \text{ Terminate With No Interrupt} \end{array}$	tion ires A Reset

Status F	Reaister	Summary
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		•				
Bit	All Type I Commands	Read Address	Read Sector	Read Track	Write Sector	Write Track
S7 S6		NOT READY Ø	NOT READY Ø	NOT READY Ø	NOT READY WRITE PROTECT	NOT READY WRITE PROTECT
	HEAD LOADED	-	RECORD TYPE	Ø	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	RNF	RNF	0	RNF	Ø
S3	CRC ERROR	CRC ERROR	CRC ERROR	ø	CRC ERROR	Ø
S2	TRACK Ø	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
SØ	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY
				1		

Status for Type I Commands

Bit	Name	Meaning
S7	NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically "ored" with MR.
S6	PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of WRPT input.
S5	HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4	SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3	CRC ERROR	CRC encountered in ID field.
S2	TRACK ØØ	When set, indicates Read/Write head is positioned to Track Ø. This bit is an inverted copy of the TRØ input.
S1	INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{\text{IP}}$ input.
SØ	BUSY	When set command is in progress. When reset no command is in progress.

Status for Type II and III Commands

Bit	Name	Meaning
S7	NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and "ored" with MR. The Type II and III Commands will not execute unless the drive is ready.
S6	WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5	RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. Ø = Data Mark. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4	RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3	CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2	LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1	DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
SØ	BUSY	When set, command is under execution. When reset, no command is under execution.

Formatting the Disk

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA with a large amount of memory. Data and gap information must be provided at the computer interface. Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command.

Upon receipt of the Write Track command, the head is loaded and the Busy Status bis is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeroes is substituted.

This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the SAB 179X detects a data pattern of F5 through FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation.

The CRC generator is initialized when any data byte from F8 to FE is about to be tranferred from the DR to the DSR in FM or by receipt of F5 in MFM. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 through FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

IBM 3740 Format - 128 Bytes/Sector (8")

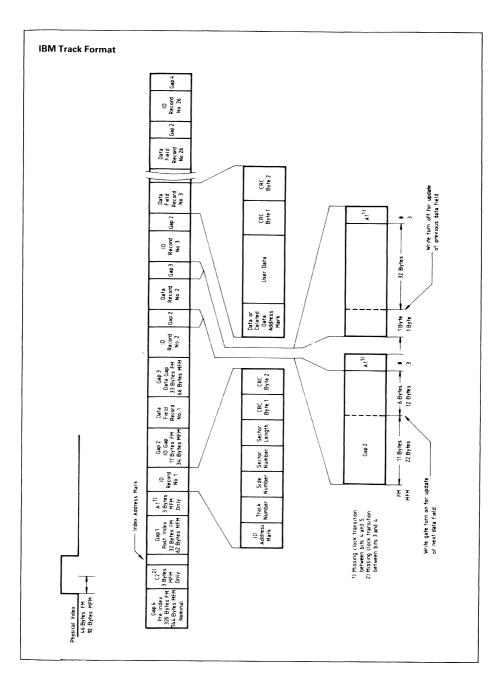
Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one data request.

Number of Bytes	Hex Value of Byte Written
40	FF (or 00) ³
6	00
1	FC (Index Mark)
26	FF (or ØØ)
1) 6	000
1	FE (ID Address Mark)
1	Track Number
1	Side Number (ØØ or Ø1)
1	Sector Number (1 thru 1A)
1	000
1	F7 (2 CRC's written)
11	FF (or 0/0)
6	000
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
27	FF (or 0/00)
247 ²	FF (or 0/00)

¹⁾ Write bracketed field 26 times

²⁾ Continue writing until SAB 179X interrupts out. Approx. 247 bytes.

³⁾ Optional '00' on SAB 1795/7 only.



IBM System 34 Format 256 Bytes/Sector (8")

Shown below is the IBM dual-density format with 256 bytes/sector. In order to format a diskette the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

Number	Hex value of
of Bytes	Byte written
80	4E
12	00
3	F6 (writes C2)
1	FC (Index Mark)
1)50	4E
12	00
3	F5
1	FE (ID Address Mark)
1	Track Number (Øthrough 4C)
1	Side Number (Ø or 1)
1	Sector Number (1 through 1A)
1	Ø1 (Sector length)
1	F7 (2 CRCs written)
22	4E
12	00
3	F5 (writes A1)
1	FB (Data Adress Mark)
256	DATA
1	F7 (2 CRCs written)
54_	4E
598 ²⁾	4E

Shown below is the Recommended single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one data request.

nber F	Hex Value of
ytes [Byte Written
40 F	F (or 00) ³⁾
6 (00
1 1	E (ID Address Mark)
1 -	Frack Numer
1 9	Side Number (00 or 01)
1 :	Sector Number (1through 1A)
1 (00 (Sector length)
1 1	7 (2 CRC's written)
11 1	F (or 00) ³⁾
6 (ðØ
1 1	B (Data Address Mark)
128	Data (IBM uses E5)
1	7 (2 CRC's written)
10	=F (or ØØ) ³⁾
369 ²⁾	⁼ F (or ØØ) ³⁾
40 F 6 6 6 6 6 6 6 6 6	FF (or 00) ³⁾ FF (or 00) ³⁾ FF (ID Address Mark) Frack Numer Frack Number (00 or 01) FF (or 00) ³⁾ FF (or 00) ³⁾ FF (Data Address Mark) FF (2 CRC's written) FF (Or 00) ³⁾

¹⁾ Write bracketed field 16 times

Recommended - 128 Bytes/Sector (Mini-Diskette)

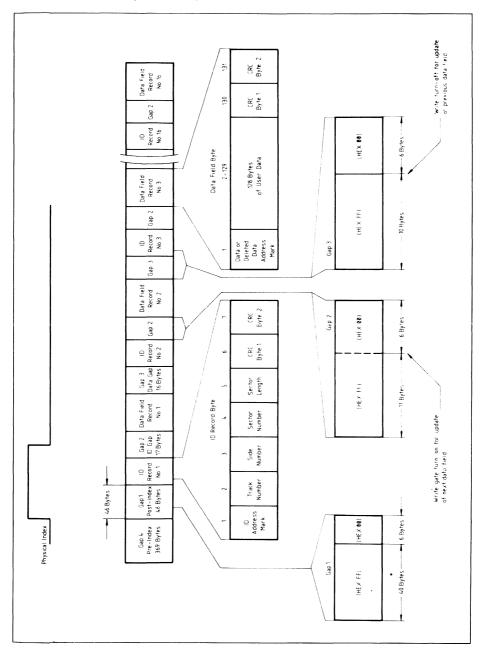
²⁾ Continue writing until SAB 179X interrupts out. Approx 369 bytes.

³⁾ Optional '00' on SAB 1795/7 only.

¹⁾ Write bracketed field 26 times

²⁾ Continue writing until SAB179X interrupts out. Approx. 598 bytes.

Recommended Single Density Format (Mini-Diskette)



256 Bytes/Sector (Mini-Diskette)

Shown below is the recommended dual-density format with 256 bytes/sector. In order to format a diskette the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

Number	Hex value of
of Bytes	Byte written
60	4E
1) 12	00
3	F5 (Writes A1)
1	FE (ID Address Mark)
1	Track Number (Øthrough 4C)
1	Side Number (Ø or 1)
1	Sector Number (1 through 1A)
1	Ø1 (Sector Length)
1	F7 (2 CRCs written)
22	4E
12	00
3	F5 (Writes A1)
1	FB (Data Address Mark)
256	DATA
1	F7 (2 CRCs written)
24	4E
718 ²⁾	4E

Variations in the recommended formats are possible to a limited extent if the following requirements are met:

- 1) Sector size must be 128, 256, 512 of 1024 bytes.
- 2) Gap 2 cannot be varied from the recommended format.
- 3) 3 bytes of A1 must be used in MFM.

In addition, the Index Address Mark is not required for operation by the SAB 179X. Gap 1, 3, and 4 lengths can be as short as 2 bytes for SAB 179X operation, however PPL lock up time, motor speed variation, write-splice area, etc. will add more bytes to each gap to achieve proper operation. It is recommended that the recommended format be used for highest system reliability.

	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
3)	6 bytes 00	12 bytes 00
		3 bytes A1
Gap III	10 bytes FF	24 bytes 4E
4)	4 bytes 00	8 bytes 00
		3 bytes A1
Gap IV	16 bytes FF	16 bytes 4E

Control Bytes for Initialization

Data Pattern in DR (Hex.)	SAB 179X Interpretation in FM (DDEN = 1)	SAB 179X Interpretation in MFM (DDEN = \emptyset)
00 through F4 F5 F6 F7 F8 through FB FC FD FE	Write ØØ through F4 with CLK = FF Not Allowed Not Allowed Generate 2 CRC bytes Write F8 through FB, Clk = C7, Preset CRC Write FC with Clk = D7 Write FD with Clk = FF Write FE, Clk = C7, Present CRC Write FF with Clk = FF	Write Øthrough F4, in MFM Write A1 ¹⁾ in MFM, Preset CRC Write C2 ²⁾ in MFM Generate 2 CRC bytes Write F8 through FB, in MFM Write FC in MFM Write FD in MFM Write FE in MFM Write FE in MFM

¹⁾ Missing clock transition between bits 4 and 5

Non-standards Formats

¹⁾ Write bracketed field 26 times

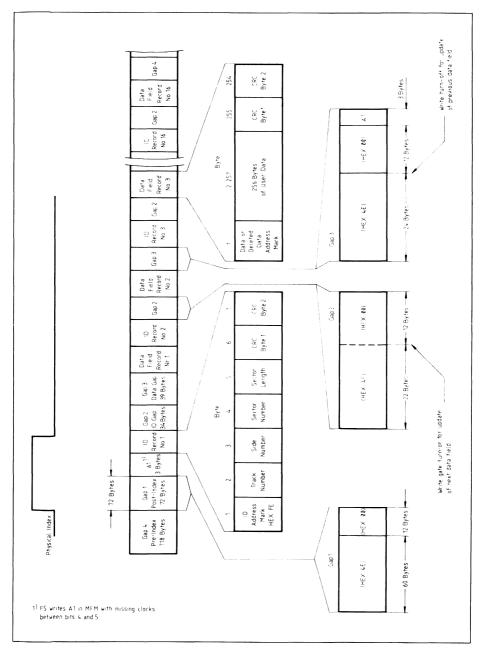
²⁾ Continue writing until SAB 179X interrupts out. Approx. 718 bytes.

³⁾ Byte counts must be exact.

⁴⁾ Byte counts are minimum, except exactly 3 bytes of A1 must be written in MFM.

²⁾ Missing clock transition between bits 3 and 4

Recommended Double Density Format (Mini-Diskette)



Absolute maximum ratings¹⁾

Respect to VSS

D. C. Characteristics

TA = 0 to 70° C; VDD = \pm 12 V \pm 5%; VCC = \pm 5V \pm 5%; VSS = OV

Symbol	Parameter	arameter Limit Values		Unit	Test Condition	
		Min.	Тур.	Max.	1	
IIL	Input Leakage			10	μΑ	VIN = VDD ²¹
IOL	Output Leakage			10	μΑ	VOUT = VDD
VIH	Input High Voltage	2.6]-	-		
VIL	Input Low Voltage	-		0.8	$]_{v}$	
VOH	Output High Voltage	2.8	1	_] `	$IO = -100 \mu A$
VOL	Output Low Voltage		1	0.45		IO = 1.6mA
ICC	Power Supply Current		35	60	mA	
IDD	Power Supply Current		10	15]''''	_
PD	Power Dissipation		_	0.6	W	

Capacitance³⁾

Symbol	Parameter	Limit Value (max.)	Unit	Test Condition
CIN	Input Capacitance	45		Unmeasured pins
COUT	Output Capacitance	15	pF	returned to GND

¹⁾ Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

²⁾ Leakage conditions are for input pins without internal pull-up resistors.

³⁾ This parameter is periodically sampled and not 100% tested.

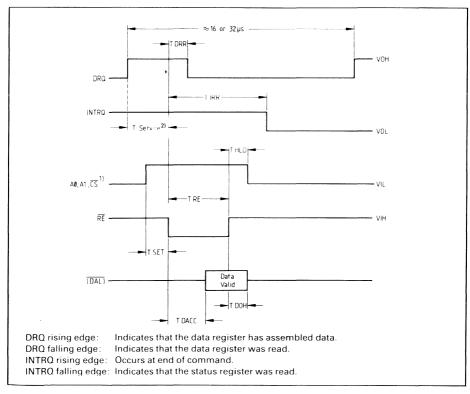
A.C. Characteristics

TA = 0 to 70° C, VDD = + 12 V \pm 5%; VSS = 0V, VCC = + 5V \pm 5%

All timing readings at VOL = 0.8 V and VOH = 2.0 V.

Read Enable Timing

Symbol	Parameter	Limit Values		Unit	Test Condition	
		Min.	Тур.	Max.		
TSET	Setup ADDR & CS to RE	50				-
THLD	Hold ADDR & CS from RE	10	7-	-		
TRE	RE Pulse Width	400	1			CL = 50pf
TDRR	DRQ Reset from RE		400	500	ns	
TIRR	INTRQ Reset from RE	_	500	3000	1	-
TDACC	Data Access from RE			350	1	CI FO-4
TDOH	Data Hold from RE	50		150	1	CL = 50pf



¹⁾ $\overline{\text{CS}}$ may be permanently tied LOW if desired.

²⁾ T Service (worst case)

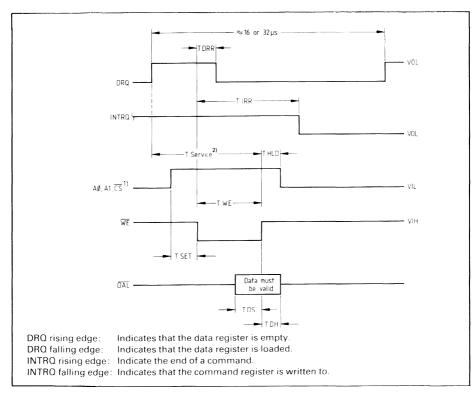
 $^{-\}mathsf{FM}=\mathsf{27.5}\,\mu\mathsf{s}$

 $⁻ MFM = 13.5 \,\mu s$

³⁾ Times double when CLK = 1MHz

Write Enable Timing

Symbol	Parameter Limit Values		Parameter		Units	Test Conditions
		Min.	Тур.	Max.	7	
TSET	Setup ADDR & CS to WE	50				
THLD	Hold ADDR & CS from WE	10	1			
TWE	WE Pulse Width	350	1	_	ns	
TDRR	DRQ Reset from WE		400	500	7 ''5	
TIRR	INTRQ Reset from WE		500	3000]	
TDS	Data Setup to WE	250			1	
TDH	Data Hold from WE	70	7			



¹⁾ CS may be permanently tied LOW if desired. When writing Data into Sector Track or Data Register User cannot read this Register until at least 4μs in MFM after the rising edge of WE when writing into the command Register Status is not valid until some 28μs in FM.14 μs in MFM later.

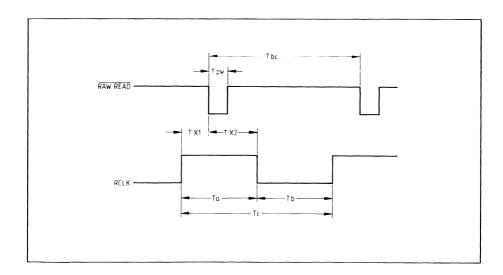
²⁾ T Service (worst case); FM = 23.5 μ s; MFM = 11.5 μ s

³⁾ Times double when CLK=1MHz

Input Data Timing

Symbol	Parameter	Limit Values		alues Units		its Test Conditions	
		Min.	Тур.	Max.]		
Tpw	RAW READ Pulse Width	100	200			1)	
Tbc	RAW READ Cycle Time ²⁾	1500	2000	1		1800 ns @ 70°C	
Тс	RCLK Cycle Time ³⁾	7 1500	2000	_	ns	1800 118 @ 70 C	
Tx1	RCLK hold to RAW READ	40		1		1)	
Tx2	RAW READ hold to RCLK	7 40				1)	

¹⁾ Pulse width on RAW READ (Pin 27) is normally 100 – 300ns. However, pulse may be any width if pulse is entirely within window. If pulse occurs in both windows, then pulse width must be less than 300ns for MFM at CLK = 2MHz and 600ns for FM at 2MHz. Times double for 1MHz.



				Nominal				
Diskette	Mode	DDEN	CLK	Ta	Tb	Tc		
8''	MFM	Ø	2 MHz	1 μs	1 μs	2 μs		
3′′	FM	1	2 MHz	2 μs	2 μs	4 μs		
ō''	MFM	Ø	1 MHz	2 μs	2 μs	4 μs		
5′′	FM	1	1 MHz	4 μs	4 μs	8 μs		

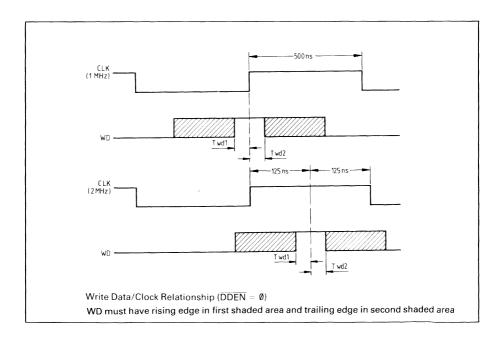
A PPL Data Separator is recommended for 8" MFM

 $^{^{2)}}$ tbc should be 2 μ s, nominal in MFM and 4 μ s nominal in FM. Times double when CLK = 1 MHz.

³⁾ RCLK may be high or low during RAW READ (Polarity is unimportant).

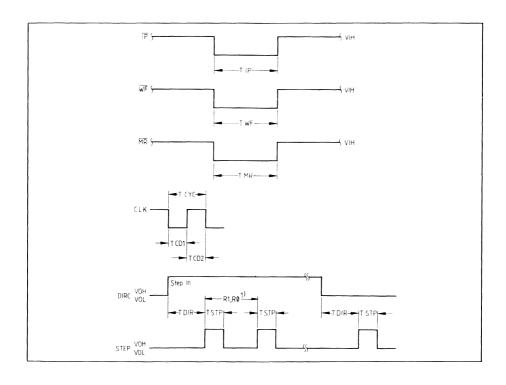
Write Data Timing (All Times Double when CLK = 1 MHz)

Symbol	Parameter		Limit Va	lues	Units	Test Conditions
		Min.	Тур.	Max.	1	
Twp	Write Data Pulse Width	450 150	500 200	550 250	ns	FM MFM
Twg	Write Gate to Write Data		2			FM MFM
Tbc	Write data cycle Time		2,3 or 4		μS	± CLK Error
Ts	Early (Late) to Write Data	125		1	ns	MFM
Th	Early (Late) from Write Data	125			1113	TVII IVI
Twf	Write Gate off from WD	-	2	_	μS	FM MFM
Twd1	WD Valid to CLK	100 50			ns	CLK = 1MHz CLK = 2MHz
Twd2	WD Valid after CLK	100 30	1 1 1		113	CLK = 1MHz CLK = 2MHz



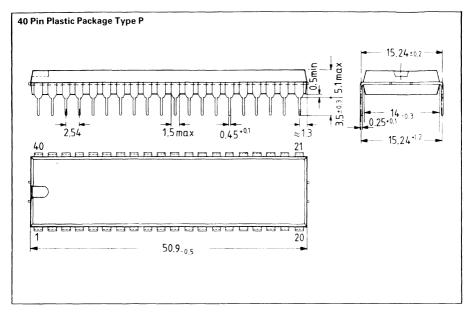
Miscellaneous Timing

Symbol	Parameter	Limit Values			Units	Test Conditions	
		Min.	Тур.	Max.			
TCD1	Clock Duty (LOW)	230		20000		2)	
TCD2	Clock Duty (HIGH)	200	1		ns		
TSTP	Step Pulse Output	2 or 4	-			1	
TDIR	Dir Setup to Step	-	12			+ CLK Error	
TMR	Master Reset Pulse Width	50		1-	μs	± CLK EffOf	
TIP	Index Pulse Width	10				2)	
TWF	Write Fault Pulse Width	20	_			2)	



¹⁾ From step rate table. ²⁾ Times double when CLK=1MHz

Package Outline



Ordering Information

Туре	Type Description	
SAB 1791-02-P	Floppy-Disk-Controller;	Q 67120-Y 39
	Inverted Data Bus, single-sided operation	
SAB 1793-02-P	Floppy-Disk-Controller;	Q 67120-Y 40
	True Data Bus, single-sided operation	
SAB 1795-02-P	Floppy-Disk-Controller;	Q 67120-Y 46
	Inverted Data Bus, double-sided operation	
SAB 1797-02-P	Floppy-Disk-Controller;	Q 67120-Y 47
	True Data Bus, double-sided operation	

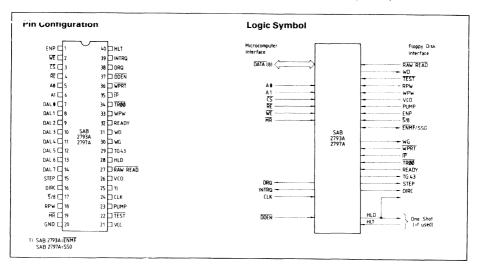
Preliminary

SAB 2793A/2797A Floppy Disk Formatter/ Controller Family

SAB 2793A	SAB 2797A
х	Х
X	Х
X	Х
	Х
Х	
	Х

- On-chip PLL data separator
- On-chip write precompensation logic

- Single +5V supply
- Accommodates single and double-density formats IBM 3740 single density (FM)
 IBM System 34 double density (MFM)
- · Automatic seek with verify
- Multiple sector read/write
- TTL-compatible
- Programmable control Selectable track-to-track access Head load timing
- Software-compatible with the SAB 179X floppy disk formatter/controller family
- Soft sector format compatibility



The SAB 2793A/2797A are floppy disk controllers in N-channel MOS LSI technology designed to interface with SAB 8080/8085/8051/8086/8088/80186/80188/80286 family processors. Its flexibility and ease of use makes it an ideal floppy disk interface between conventional floppy disks and all computer systems. Software-compatible with its predecessor, the SAB 179X, the device also contains a high-

performance phase-lock-loop data separator as well as write precompensation logic.

When operating in double density mode, write precompensation is automatically engaged to a value programmed via an external potentiometer. An on-chip VCO and phase comparator allows adjustable frequency range for 51/4 "-8" floppy disk and microfloppy disk interface.

Pin Definitions and Functions

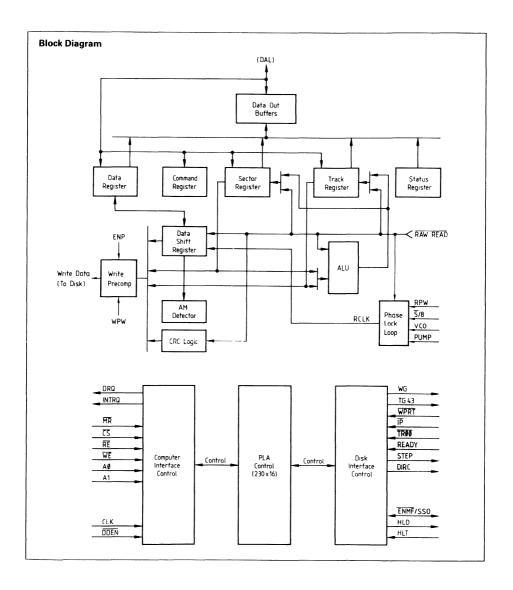
Symbol	Pin	Input (I) Output (O)	Function					
ENP	1	1	ENABLE PRECOMP A logic high on this input enables write precompensation to be performed on the write data output					
WE	2	I	WRITE ENABLE A logic low on this input gates data on the DAL into the selected register when CS is low					
CS	3	I	CHIP SELECT A logic low on this input selects the chip and enables comp communication with the device					
RE	4	I	READ ENABLE A logic low on this input controls the placement of data from a selected register on the DAL when CS is low					
A0, A1	5, 6	I	REGISTER SELECT LINES These inputs select the register to receive/transfer data on the DAL lines under RE and WE control: CS A1 A0 RE WE 0 0 0 Status register Command register 0 0 1 Track register Track register 0 1 0 Sector register Sector register 0 1 1 Data register Data register					
DALØ to DAL7	7-14	1/0	DATA ACCESS LINES 8-bit bidirectional bus used for transfer of commands, status and data					
STEP	15	0	STEP The step output contains a pulse for each step					
DIRC	16	0	DIRECTION Direction output is active high when stepping in, active low when stepping out					
5/8	17	1	$5^{1/4}$ ", 8" SELECT This input selects the internal VCO frequency for use with $5^{1/4}$ " drives or 8" drives					
RPW	18	ı	READ PULSE WIDTH An external potentiometer tied to this input controls the phase comparator within the data separator					
MR	19	I	MASTER RESET A logic low (50 µs min.) on this input resets the device and loads hex 03 into the command register. The "not ready bit" (status bit 7) is reset during MR active. When MR is brought to a logic high a restore command is executed, regardless of the state of the ready signal from the drive. Also hex 01 is loaded into sector register					
TEST	22	1	TEST A logic low on this input allows adjustment of external resistors by enabling internal signals to appear on selected pins					

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function				
PUMP	23	0	PUMP High-impedance output signal which is forced high or low to increase/decrease the VCO frequency				
CLK	24	1	CLOCK This input requires a free-running, 50% duty cycle square-wave clock for internal timing reference, 2 MHz \pm 1% for 8" drives, 1 MHz \pm 1% for minifloppies				
ENMF	25	ı	ENABLE MINIFLOPPY (SAB 2793A) A logic low on this input enables an internal divide by 2 of the master clock. This allows both 51/4" and 8" drive operation with a single 2 MHz clock. For a 1 MHz clock on pin 24, this line must be left open or tied to a logic 1				
SSO 25 O			SIDE SELECT OUTPUT (SAB 2797A) The logic level of the side select output is directly controlled by the U flag in type II or III commands. When U = 1, SSO is set to a logic 1. When U = 0, SSO is set to a logic 0. The SSO is compared with the side information in the sector ID field. If the do not correspond, status bit 4 (RNF) is set. The side select output is only updated at the beginning of a type II or III command. It is forced to a logic 0 upon a master reset condition				
VCO	26	-	VOLTAGE CONTROLLED OSCILLATOR An external capacitor tied to this pin adjusts the VCO center frequency				
RAW READ	27	1	RAW READ The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition				
HLD	28	0	HEAD LOAD The HLD output controls the loading of the read/write head against the media				
TG43	29	0	TRACK GREATER THAN 43 This output informs the drive that the read/write head is positioned between tracks 44 and 76. This output is valid only during read and write commands				
WG	30	0	WRITE GATE This output is made valid before writing is to be performed on the diskette				
WD	31	0	WRITE DATA MFM or FM output pulse per flux transition. WD contains the unique address marks as well as data and clock in both FM and MFM formats				
READY 32 I			READY This input indicates disk readiness and is sampled for a logic high before read or write commands are performed. If ready low the read or write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of ready. The ready input appears in inverted format as status register bit 7				

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function			
WPW	33	ı	WRITE PRECOMP WIDTH An external potentiometer tied to his input controls the amount of delay in write precompensation mode			
TR00	34	I	TRACK 00 This input informs the SAB 2793A/2797A that the read/write head is positioned over track 00			
ĪΡ	35	ı	INDEX PULSE This input informs the SAB 2793A/2797A when the index hole is encountered on the diskette			
WPRT	36	ı	WRITE PROTECT This input is sampled whenever a write command is received. A logic low terminates the command and sets the write protect status bit			
DDEN	37	I				
DRQ	38	0	DATA REQUEST This output indicates that the data register (DR) contains assembled data in read operations, or the DR is empty in write operations. This signal is reset when serviced by the computer through reading or loading the data register			
INTRQ	39	0	INTERRUPT REQUEST This output is set at the completion of any command and is reset when the status register is read or the command register is written to			
HLT	40	I	HEAD LOAD TIMING When a logic high is found on the HLT input the head is assumed to be engaged. It is typically derived from a single shot triggered by HLD			
VCC	21	-	POWER SUPPLY (+5V)			
VSS	20	-	GROUND (0 V)			



General Description

The SAB 2793A/2797A are N-channel MOS LSI devices performing the functions of a Floppy Disk Formatter/Controller in a single-chip implementation. The SAB 2793A/2797A is IBM 3740 compatible in single density mode (FM) and System 34 compatible in double density mode (MFM). The SAB 2793A/2797A contains all the features of its predecessor, the SAB 179X, plus a high-performance phase-lock-loop data separator as well as write precompensation logic. In double density mode, write precompensation is automatically engaged to a value programmed via an external potentiometer. In order to maintain compatibility, the SAB 179X and SAB 2793A/2797A designs were

made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load control is identical in each case, the actual pin assignments vary by only a few pins from any one to another.

The processor interface consists of an 8-bit bidirectional bus for data, status, and control word transfers. The SAB 2793A/2797A is set up to operate on a multiplexed bus with other bus-oriented devices. The SAB 2793A/2797A is TTL compatible on all inputs and outputs. The outputs will drive one TTL load or three LS loads.

The SAB 2797A has a side select output to control double sided drives.

Organization

The Floppy Disk Formatter block diagram is illustrated on page 5. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register (DSR) – This 8-bit register assembles serial data from the Read Data input (RAW READ) during read operations and transfers serial data to the Write Data output during write operations.

Data Register (DR) – This 8-bit register is used as a holding register during disk read and write operations. In disk read operations the assembled data byte is transferred in parallel from the Data Shift Register to the Data Register. In disk write operations information is transferred in parallel from the Data Register to the Data Shift Register. When executing the Seek command the Data Register holds the address of the desired track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register (TR) – This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk read, write and verify operations. The Track Register can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Sector Register (SR) – This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk read or write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) – This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a Force Interrupt command. The command register can be loaded from the DAL. but not read onto the DAL.

Status Register (STR) – This 8-bit register holds device status information. The meaning of the status bits depends on the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic – This logic is used to check or to generate the 16-bit Cycle Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$ The CRC includes all information starting with the address mark and up to the CRC character. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) – The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control – All computer and Floppy Disk interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

AM Detector – The address mark detector detects ID, data and index address marks during read and write operations.

Write Precompensation – Enables write precompensation to be performed on the Write Data output.

Data Separator – A high-performance phase-lock-loop data separator with on-chip VCO and phase comparator allows adjustable frequency range for 51/4" or 8" Floppy Disk interfacing.

Processor Interface

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer data, status, and control words out of or into the SAB 2793A/2797A. The DAL are three-state buffers that are enabled as output drivers when Chip Select ($\overline{\text{CS}}$) and Read Enable ($\overline{\text{RE}}$) are active (low logic state) or act as input receivers when $\overline{\text{CS}}$ and Write Enable ($\overline{\text{WE}}$) are active.

When data transfer with the Floppy Disk Controller is required by the host processor, the device address is decoded and \overline{CS} is made low. The address bits A1 and A0, combined with the signals \overline{RE} during a read operation or \overline{WE} during a write operation, are interpreted as selector for the following registers:

A1	A0	READ	WRITE
0	0	Status Register	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

During direct memory access (DMA) types of data transfers between the Data Register of the SAB 2793A/2797A and the processor, the Data Request (DRQ) output is used for data transfer control. This signal also appears as status bit 1 during read and write operations.

In disk read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters have been lost by having transferred new data into the register prior to processor readout, the Lost Data bit is set in the Status Register. The read operation continues until the end of sector is reached.

In disk write operations the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeros is written on the diskette and the Lost Data bit is set in the Status Register.

Upon completion of every command an INTRQ is generated. INTRQ is reset either by reading the Status Register or by loading the Command Register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

The SAB 2793A/2797A has two modes of operation depending on the state of \overline{DDEN} (Pin 37). When $\overline{DDEN}=1$, Single Density (FM) is selected. When $\overline{DDEN}=0$, Double Density (MFM) is selected. In either case, the CLK input (Pin 24) is set at 2 MHz for 8" drives or at 1 MHz for $5^1/4$ " drives. On the SAB 2793A the \overline{ENMF} input (Pin 25) can be used for controlling both, $5^1/4$ " and 8" drives with a single 2 MHz clock. When $\overline{ENMF}=0$, an internal divide by 2 of the CLK is performed. When $\overline{ENMF}=1$, no divide takes place. This allows the use of a 2 MHz clock for both, $5^1/4$ " and 8"

The internal VCO frequency must also be set to the proper value. The $\bar{5}/8$ input (Pin 17) is used to select data separator operation by internally dividing the read clock. When $\bar{5}/8=0$, $5^{1}/4^{\prime\prime}$ drive data separation is selected; when $\bar{5}/8=1$, $8^{\prime\prime}$ drive data separation is selected.

Clock (24)	ENMF (25)	5/8 (17)	Drive
2 MHz	1	1	8''
2 MHz	0	0	51/4"
1 MHz	1	0	51/4''

All other conditions are invalid.

configurations.

Functional Description

The SAB 2793A/2797A is software-compatible with the SAB 179X series of Floppy Disk Controllers. Commands, status, and data transfers are performed in the same way. Software generated for the SAB 179X can be transferred to a SAB 2793A/2797A system without modification.

In addition to the SAB 179X, the SAB 2793A/2797A contains an internal data separator and write precompensation circuit. The $\overline{\text{TEST}}$ (Pin 22) line is used to adjust both, data separator and precompensation. When $\overline{\text{TEST}}=0$, the WD (Pin 31) line is internally connected to the output of the write precomp single shot. Adjustment of the WPW (Pin 33) line can then be accomplished. A second single shot tracks the precomp setting at approximately 3:1 to ensure adequate Write Data pulse widths to meet drive specifications.

Similarly, data separation is also adjusted with $\overline{\text{TEST}} = 0$. The TG43 (Pin 29) line is internally connected to the output of the read data single shot, which is adjusted via the RPW (Pin 18) line. The DIRC (Pin 16) line contains the read clock output (500 kHz for 8" drives). The VCO trimming capacitor (Pin 26) is adjusted to center frequency.

Internal timing signals are used to generate pulses during the adjustment mode so that these adjustments can be made while the device is in operation. The TEST line also contains a pull-up resistor, so adjustments can be performed simply by grounding the TEST pin, overriding the pull-up. The TEST pin cannot be used to disable stepping rates during operation as its function is quite different from the SAB 179X.

Other pins on the device also include pull-up resistors and may be left open to satisfy a logic 1 condition. These are: ENP, 5/8, ENMF, WPRT, DDEN, HLT, TEST, and MR.

General Disk Read Operation

Sector lengths of 128, 256, 512 or 1024 are obtainable either in FM or MFM formats. For FM, DDEN should be placed to logic 1. For MFM formats, DDEN should be placed to a logic 0. Sector lengths are determined at format time by the fourth byte in the ID field.

Sector Length Table*						
Sector Length Field (hex)	Number of Bytes in Sector (decimal)					
00	128					
01	256					
02	512					
03	1024					

^{*} SAB 2797A may vary - see command summary.

The number of sectors per track as far as the SAB 2793A/2797A is concerned can vary between 1 and 255 sectors. The number of tracks as far as the SAB 2793A/2797A is concerned is from 0 to 255 tracks. For IBM 3740 compatibility, sector lengths are 128 byte with 26 sectors per track. For System 34 compatibility (MFM), sector lengths are 256 byte/sector with 26 sectors/track; or lengths of 1024 byte/sector with 8 sectors/track.

General Disk Write Operation

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the SAB 2793A/2797A before the Write Gate signal can be activated. Writing is inhibited when the Write Protect input is logic low, in which case any write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set.

For write operations, the SAB 2793A/2797A provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write Data consists of a series of pulses set to a width approximately three times greater than the precomp adjustment. Write Data provides the unique address marks in both formats.

Ready

Whenever a read or write command (Type II or III) is received the SAB 2793A/2797A samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated. TG43 may be tied to ENP to enable write precompensation on tracks 44–76.

Write Precompensation

When operating in double density mode (DDEN = 0), the SAB 2793A/2797A has the capability of providing a user-defined precompensation value for Write Data. An external potentiometer (10k) tied to the WPW signal (Pin 33) allows a setting of 100 to 300 ns from nominal.

Setting the write precomp value is accomplished by forcing the TEST line (Pin 22) to a logic 0. A stream of pulses can then be seen on the Write Data (Pin 31) line. Adjust the WPW Potentiometer for the desired pulse width. This adjustment may be performed incircuit since the Write Gate (Pin 30) is inactive while TEST = 0.

Data Separation

The SAB 2793A/2797A can operate with either an external data separator or its own internal recovery circuit. The condition of the $\overline{\text{TEST}}$ line (Pin 22) in conjunction with $\overline{\text{MR}}$ (Pin 19) will select internal or external mode.

To program the SAB 2793A/2797A for external VCO, a \overline{MR} pulse must be applied while $\overline{TEST}=0$. A clock equivalent to eight times the data rate (e.g. 4.0 MHz for 8" double density) is applied to the VCO input (Pin 26). The feedback reference voltage is available on the PUMP output (Pin 23) for external integration to control the VCO. \overline{TEST} is returned to a logic 1 for normal operation. Note: To maintain this mode, \overline{TEST} must be held low whenever \overline{MR} is applied.

For internal VCO operation, the TEST line must be high during the MR pulse, then set to a logic 0 for the adjustment procedure.

A 50 k Potentiometer tied to the RPW input (Pin 18) is used to set the internal Read Data pulse for proper phasing. With a scope on Pin 29 (TG43), adjust the RPW pulse for 1/8 of the data rate (250 ns for 8" Double Density). An external, variable capacitor of typically 5 to 60 pF is tied to the VCO input (Pin 26) for adjusting center frequency. With a frequency counter on Pin 16 (DIRC) adjust the trimmer cap to yield the appropriate data rate (500 kHz for 8" Double Density). The $\overline{\text{DDEN}}$ line must be low while the $\overline{\text{5}}/8$ line is held high or the adjustment times above will be doubled.

VCO Operation

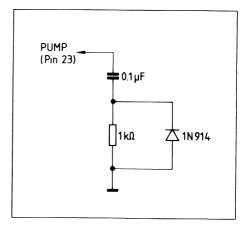
After adjustments have been made, the TEST pin is returned to a logic 1 and the device is ready for operation. Adjustments may be made in-circuit since the DIRC and TG43 lines may toggle without affecting the drive.

The PUMP output (Pin 23) consists of positive and negative pulses. Their duration is equivalent to the phase difference of incoming Data versus VCO frequency. This signal is internally connected to the VCO input, but a filter is needed to connect these pulses to a slow moving DC voltage.

The internal phase-detector is unsymmetrical for a random distribution of data pulses by a factor of two, in favor of a PUMP UP condition. Therefore it is desirable to have a PUMP DOWN twice as responsive to prevent run-away during a lock attempt.

A first-order lag-lead filter can be used at the PUMP output (Pin 23). This filter controls the instantaneous response of the VCO to bit-shifted data (jitter) as well as response to normal frequency shift i.e. the lock-up time. A balance must be accomplished between the two conditions to inhibit overresponsiveness to jitter and to prevent an extremely wide lock-up response leading to PUMP run-away. The filter affects these two reactions in mutually opposite directions.

The following Filter Circuit is recommended for 8" FM/MFM:



Since 51/4" Drives operate at exactly one-half the data rate (250 Kbyte/s) the above capacitor should be doubled to 0.2 or 0.22 μF .

Command Summary

	Commands for SAB 2793A								Com	man	ds fo	or SA	AB 27	797A				
						Bit	s							Bit	s			
Туре	Command		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1	Restore		0	0	0	0	h	٧	r ₁	r ₀	0	0	0	0	h	٧	r ₁	r ₀
1	Seek		0	0	0	1	h	V	\mathbf{r}_1	\mathbf{r}_0	0	0	0	1	h	V	\mathbf{r}_1	ro
i	Step		0	0	1	Τ	h	V	\mathbf{r}_1	r_0	0	0	1	Τ	h	V	r_1	r_0
1	Step-in		0	1	0	T	h	V	\mathbf{r}_1	\mathbf{r}_0	0	1	0	T	h	V	\mathbf{r}_{1}	r _o
1	Step-out		0	1	1	Τ	h	V	r_1	r_0	0	1	1	Τ	h	V	\mathbf{r}_1	\mathbf{r}_{0}
П	Read sector		1	0	0	m	S	Ε	С	0	1	0	0	m	L	Ε	U	0
П	Write Sector		1	0	1	m	S	Ε	С	a_0	1	0	1	m	L	Е	U	a_0
III	Read Address		1	1	0	0	0	Ε	0	0	1	1	0	0	0	Ε	U	0
111	Read Track		1	1	1	0	0	Ε	0	0	1	1	1	0	0	Ε	U	0
III	Write Track		1	1	1	1	0	Ε	0	0	1	1	1	1	0	Ε	U	0
IV	Force Interrupt		1	1	0	1	I_3	12	1,	I_0	1	1	0	1	I_3	12	1,	10

Flag Summary

Command Type	Bit	Description					
	r ₁ , r ₀ - Stepping Motor Rate V = Track Number Verify Flag	See page 13 for details V = 0, No verify V = 1, Verify on destination track					
1	h = Head Load Flag	h = 0, Unload head at beginning h = 1, Load head at beginning					
I	T = Track Update Flag	T = 0, No update T = 1, Update track register					
II & III	a ₀ = Data Address Mark	$egin{array}{ll} \mathbf{a_0} &= 0, FB (DAM) \\ \mathbf{a_0} &= 1, F8 (deleted DAM) \end{array}$					
II	C = Side Compare Flag	C = 0, Disable side compare C = 1, Enable side compare					
II & III	U = Update SSO	U = 0, Update SSO to 0 U = 1, Update SSO to 1					
II & III	E = 15 ms Delay	E = 0, No 15 ms delay E = 1, 15 ms delay (30 ms for 1 MHz clock)					
11	S = Side Compare Flag	S = 0, Compare for side 0 S = 1, Compare for side 1					
II	L = Sector Length Flag L = 1 (implicit) for SAB 2793A	LSB's Sector Length in ID Field 00 01 10 11 L = 0 256 512 1024 128 L = 1 128 256 512 1024					
II	m = Multiple Record Flag	m = 0, Single record m = 1, Multiple records					
IV	Ix = Interrupt Conditions Flags I0 = 1: Interrupt on Not Ready to Ready Transition I1 = 1: Interrupt on Ready to Not Ready Transition I2 = 1: Interrupt on Next Index Pulse I3 = 1: Immediate Interrupt Requires a Reset * I3-I0 = 0: Terminate with No interrupt (INTRQ)						

^{*} See Type IV command description for further information.

Status Register Summary

Bit	All Type I Commands	Read Address	Read Sector	Read Track	Write Sector	Write Track
S7 S6	NOT READY WRITE	NOT READY 0	NOT READY 0	NOT READY 0	NOT READY WRITE	NOT READY WRITE
	PROTECT	Ĭ	ľ	ľ	PROTECT	PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	0	0
S4	SEEK ERROR	RNF	RNF	0	RNF	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 00	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

Status for Type I Commands

Bit	Name	Meaning
S7	NOT READY	This bit, when set, indicates that the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically ORed with $\overline{\text{MR}}$.
S6	WRITE PROTECT	When set, indicates that Write Protect in activated. This bit is an inverted copy of WPRT input.
S5	HEAD LOADED	When set, it indicates that the head is loaded and engaged. This bit is a logical AND of HLD and HLT signals.
S4	SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3	CRC ERROR	CRC encountered in ID field.
S2	TRACK 00	When set, indicates that Read/Write head is positioned to Track 00. This bit is an inverted copy of the TR00 input.
S1	INDEX	When set, indicates that index mark is detected from drive. This bit is an inverted copy of the $\overline{\text{IP}}$ input.
S0	BUSY	When set, command is in progress. When reset, no command is in progress.

Status for Type II and III Commands

Bit	Name	Meaning
S7	NOT READY	This bit, when set, indicates that the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and ORed with $\overline{\text{MR}}$. The Type II and III Commands will not execute unless the drive is ready.
S6	WRITE PROTECT	For Read Record: not used. For Read Track: not used. On any Write: It indicates a Write Protect. This bit is reset, when updated.
S5	RECORD TYPE	For Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. For any Write: forced to a zero.
S4	RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3	CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2	LOST DATA	When set, it indicates that the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1	DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates that the DR is full on a read operation or the DR is empty on a write operation. This bit is reset to zero when updated.
S0	BUSY	When set, command is under execution. When reset, no command is under execution.

Summary of Adjustment Procedures

Write Precompensation

- 1) Set TEST (Pin 22) to a logic high.
- 2) Strobe MR (Pin 19).
- 3) Set TEST (Pin 22) to a logic low.
- 4) Observe pulse width on WD (Pin 31).
- 5) Adjust WPW (Pin 33) for desired pulse width (Precomp Value).
- 6) Set TEST (Pin 22) to a logic high.

Data Separator

- 1) Set TEST (Pin 22) to a logic high.
- 2) Strobe \overline{MR} (Pin 19). Ensure that $\overline{5}/8$, and \overline{DDEN} are set properly.
- 3) Set TEST (Pin 22) to a logic low.4) Observe pulse width on TG43 (Pin 29).
- 5) Adjust RPW (Pin 18) for 1/8 of the read clock (250 ns for 8" DD, 500 ns for 51/4" DD, etc.).
- 6) Observe frequency on DIRC (Pin 16).
- 7) Adjust variable capacitor on VCO pin for data rate (500 kHz for 8" DD, 250 kHz for 51/4" DD, etc.).
- 8) Set TEST (Pin 22) to a logic high.
- NOTE: To maintain internal VCO operation, insure that $\overline{\text{TEST}} = 1$ whenever a master reset pulse is applied.

Status Register

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits is updated or cleared for the new command. If the Force Interrupt command is received while a current command is under execution, the Busy status bit is reset, and the rest of the status bits is left unchanged. If the Force Interrupt command is received while there is no current command under execution, the Busy Status bit is reset and the rest of the status bits is updated or cleared as after a Type I command.

The user can optionally read the Status Register through program control or by using the DRQ line with DMA or interrupt methods. When the Data Register is read, the DRQ bit in the Status Register and the DRQ line are automatically reset. A write to the Data Register also causes the reset of both DRQs. The Busy bit in the status may be monitored by a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a busy status check is not recommended because reading the Status Register to determine the condition of Busy will reset the INTRQ line.

The format of the Status Register is shown below:

(BITS)											
7	6	5	4	3	2	1	0				
S7	S6	S5	S4	S3	S2	S1	S0				

Status varies according to the type of command executed as shown on page 11.

Because of internal sync cycles, certain time delays must be observed when operating under programmed I/O. They are:

Operation	Next Operation	Delay Req'd.	
		FM	MFM
Write to Command Reg.	Read Busy Bit (Status Bit 0)	12 μs	6 μs
Write to Command Reg.	Read Status Bits 1-7	28 μs	14 μs
Write to Any Register	Read from Diff. Register	0	0

Times double when clock = 1 MHz

Command Description

The SAB 2793A/2797A will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The only exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a

command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault-free. For ease of discussion, commands are divided into four types. Commands and types are summarized on page 10.

Type I Commands

The Type I commands include the Restore, Seek, Step, Step-In and Step-Out commands. Each of the Type I commands contains a rate field $(r_0,\,r_1)$ which determines the stepping motor rate. A 2 μs (MFM) or 4 μs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the Direction output. The chip steps the drive in the same direction it has been stepped previously, unless the command changes direction. The Direction signal is active high when stepping in and low when stepping out. The Direction signal has been valid 12 μs before the first stepping pulse is generated. The rates can be applied to a Step-Direction motor through the device interface.

Stepping Rates

CLK		2 MHz	1 MHz
r1	r0	TEST = 1	TEST = 1
0	0	3 ms	6 ms
0	1	6 ms	12 ms
1	0	10 ms	20 ms
1	1	15 ms	30 ms

After the last directional step, additional 15 milliseconds of head settling time are generated if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock. There is also a 15 ms head setting time if the E flag is set in any Type II or III command.

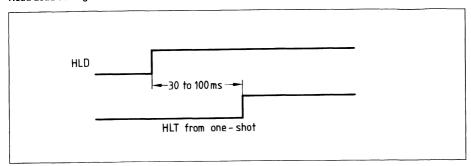
When a Seek, Step or Restore command is executed an optional verification of Read/Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification

operation begins at the end of the 15 millisecond setting time after the head is loaded against the media. The track number from the first encountered ID field is compared against the contents of the Track Register, If the track numbers correspond and the ID field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. If there is a match but not a valid CRC, the CRC Error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation. The SAB 2793A/2797A must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the Seek Error is set and an INTRQ is generated. If V = 0, no verification is performed. The Head Load (HLD) output controls the movement of the Read/Write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the Verify flag is set (V = 1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with h = 0 and V = 0, or if the SAB 2793A/2797A is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load timing (HLT) is an input to the SAB 2793A/2797A which is used for the head engage time.

When HLT= 1, the SAB 2793A/2797A assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a single shot. The output of the single shot is then used for HLT and supplied as an input to the SAB 2793A/2797A.

Head Load Timing



When both HLD and HLT are true, the SAB 2793A/2797A will read from or write to the media. The "AND" of HLD and HLT appears as status bit 5 in Type I status.

Summary of the Type I commands:

If h = 0 and V = 0, HLD is reset.

If h = 1 and V = 0, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay.

If h=0 and V=1, HLD is set near the end of the command, an internal 15 ms delay occurs, and the SAB 2793A/2797A waits for HLT to be true. If h=1 and V=1, HLD is set at the beginning of the

Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the SAB 2793A/2797A waits for HLT to occur. For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

Restore (Seek Track 0)

Upon receipt of this command the Track 00 (TR00) input is sampled. If TR00 is active low indicating the Read/Write head is positioned over track 0, the Track Register is loaded with zeros and an interrupt is generated. If TR00 is not active low, stepping pulses at a rate specified by the r₁ r₀ field are issued until the TR00 input is activated. At this time the Track Register is loaded with zeros and an interrupt is generated. If the TR00 input does not go active low after 255 stepping pulses, the SAB 2793A/2797A terminates operation, interrupts and sets the Seek error status bit. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is always executed when MR goes from an active to an inactive state.

Seek

This command assumes that the Track Register contains the track number of the current position of the Read/Write head and the Data Register contains the desired track number. The SAB 2793A/2797A will update the Track Register and issue stepping pulses in the appropriate direction until the contents of the Track Register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the termination of the command. Note: When using multiple

drives, the Track Register must be updated for the drive selected before seek commands are issued.

Step

Upon receipt of this command, the SAB 2793A/2797A issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous Step command. After a delay determined by the $r_1\,r_0\,$ field, a verification takes place if the V flag is on. If the T flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the termination of the command.

Step-In

Upon receipt of this command, the SAB 2793A/2797A issues one stepping pulse towards track 76. If the T flag is on, the Track Register is incremented by one. After a delay determined by the $r_1\,r_0$ field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the termination of the command.

Step-Out

Upon receipt of this command, the SAB 2793A/ 2797A issues one stepping pulse towards track 0. If the T flag is on, the Track Register is decremented by one. After a delay determined by the r_1 r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the termination of the command.

Exceptions

On the SAB 2797A, the SSO output is not affected during Type I commands, and an internal side compare does not take place when the Verify flag V is on.

Type II Commands

The Type II Commands are the Read Sector and Write Sector commands. Prior to loading a Type II command into the Command Register the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the Busy status bit is set. If the E flag is 1 (this is the normal case) HLD is made active and HLT is sampled after a 15 ms delay. If the E flag is 0, the head is loaded and HLT is sampled without a 15 ms delay.

When an ID field is located on the disk, the SAB 2793A/2797A compares the track number on the ID field with the Track Register. If they do not match, the next encountered ID field is read and a comparison is again made. If there has been a match, the Sector Number of the ID field is compared with the Sector Register. If there is no sector match, the next encountered ID field is read off the disk and again compared. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The SAB 2793A/2797A must find an ID field with a track number, sector number, side number, and CRC within 5 revolutions of the disk; otherwise, the Record-Not-Found status bit is set (Status bit 4) and the command is terminated with an interrupt. Each of the Type II commands contains an m flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the termination of the command. If m = 1, multiple records are read or written with the Sector Register internally updated so that an address verification can occur on the next record. The SAB 2793A/ 2797A will continue to read or write multiple records and update the Sector Register in numerical ascending sequence until the Sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

For example: If the SAB 2793A/2797A is instructed to read sector 27 and there are only 26 sectors on the track, the Sector Register exceeds the number available. The SAB 2793A/2797A will search for 5 disk revolutions, interrupt out, reset Busy, and set the Record-Not-Found status bit.

The Type II commands for the SAB 2793A also contain Side Select Compare flags. When C=0 (bit 1) no side comparison is made. When C=1, the LSB of the side number is read off the ID field of the disk and compared with the contents of the S flag (bit 3). If the S flag corresponds to the side number recorded in the ID field, the SAB 2793A/2797A continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record-Not-Found status bit is set.

The Type II and III commands for the SAB 2797A contains a Side Select flag (bit 1). When U = 0, SSO is updated to 0. Similary, U = 1 updates SSO to 1. The chip compares the SSO to the ID field. If they do not correspond within 5 revolutions the interrupt line is made active and the RNF status bit is set. The SAB 2797A Read Sector and Write Sector commands include an L flag. The L flag, in conjunction with the sector length byte of the ID Field, allows different byte lengths to be implemented in each sector. For IBM compatibility, the L flag should be set to a one.

Read Sector

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 byte in single density and 43 byte in double density after the last ID field CRC byte; if not, the ID field search is repeated. When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data status bit is set. This sequence continues until the complete data field has been input to the computer. If there is a CRC error at the end of the data field, the CRC Error status bit is set, and the command is terminated (even if it is a multiple sector command).

At the end of the read operation, the type of Data Address Mark encountered in the field is recorded in the Status Register (bit 5) as shown:

Status Bit 5		_
1	Deleted Data Mark	
0	Data Mark	

disk. At this time the Data Address Mark is written on the disk as determined by the a_0 field of the command as shown below:

a ₀	Data Address Mark (Bit 0)
1	Deleted Data Mark
	Data Mark

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The SAB 2793A/2797A counts off 11 bytes in single

side number, and correct CRC, a DRQ is generated. The SAB 2793A/2797A counts off 11 bytes in single density and 22 bytes in double density from the CRC field, and the Write Gate (WG) output is made active if the DRQ is serviced (i.e. the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros in single density and 12 bytes in double density are then written on the

The SAB 2793A/2797A then writes the data field and generates DRQs to the computer. If the DRQ is not serviced in time for continuous writing, the Lost Data status bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of hex FE in FM or in MFM. The WG output is then deactivated. For a 2 MHz clock the INTRQ is set between 8 and 12 µs after the last CRC byte has been written. For partial sector writing, the proper method is to write the data and fill the balance with zeros. By letting the chip fill the zeros, errors may be masked by the Lost Data status and improper CRC bytes.

Types III Commands

Read Address

Write Sector

Upon receipt of the Read Address command, the head is loaded and the Busy status bit is set. The next encountered ID field is then read from the disk, and the six data bytes of the ID field are assembled and transferred to the DR. And DRQ is generated for each byte. The six bytes of the ID field are shown below:

Track	Side	Sector	Sector	CRC	CRC
Address	number	address	length	1	2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the SAB 2793A/2797A checks for validity and the CRC Error status bit is set if there is a CRC error. The track address of the ID field is written into the Sector Register so that a comparison can be made by the host. At the end of the operation an interrupt is generated and the Busy status bit is reset.

Read Track

Upon receipt of the Read Track command, the head is loaded, and the Busy status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse.

All gap, header, and data bytes are assembled and transferred to the Data Register. DRQs are generated for each byte. The accumulation of bytes is synchronized to each address mark encountered. An interrupt is generated at the termination of the command.

This command has several characteristics which make it suitable for diagnostic purposes. They are: no CRC checking is performed; gap information is included in the data stream; the internal side compare is not performed; and the address mark detector is on for the duration of the command. Because the AM detector is always on, write splices or noise may cause the chip to look for an AM. If an address mark does not appear on schedule with the Lost Data status flag being set, the ID AM, ID field, ID CRC bytes, DAM, data and data CRC bytes for each sector will be correct. The gap bytes may be read incorrectly during write splice time because of synchronization.

Write Track Formatting the Disk

Formatting the disk is a comparatively simple task when operating programmed I/O or when operating under DMA with a large amount of memory. Data and gap information must be provided at the computer interface. Formatting the disk is accomplished

by positioning the R/W head over the desired track number and issuing the Write Track command. Upon receipt of the Write Track command, the head is loaded and the Busy status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The data request is activated immediately upon receipt of command, but writing will not start before the first byte is loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated by making the device not busy. The Lost Data status bit is set, and the interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted.

This sequence continues from one index mark to the next. Normally, whatever data pattern appears in the Data Register, it is written on the disk with a normal clock pattern. However, if the SAB 2793A/ 2797A detects a data pattern of F5 thru FE in the Data Register, this is interpreted as Data Address Marks with missing clocks or CRC generation. The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR or by receipt of F5 in MFM. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRCs must be generated by an F7 pattern. Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 byte.

Control Bytes for Initialization

Data Pattern in DR (hex)	SAB 2793A/2797A Interpretation in FM (DDEN = 1)	SAB 2793A/2797A Interpretation in MFM (DDEN = 0)
FE	Write 00 thru F4 with CLK = FF Not Allowed Not Allowed Generate 2 CRC Bytes Write F8 thru FB, CLK = C7, Preset CRC Write FC with CLK = D7 Write FD with CLK = FF Write FE, CLK = C7, Preset CRC Write FF with CLK - FF	Write 00 thru F4, in MFM Write A1 ¹¹ in MFM, Preset CRC Write C2 ²¹ in MFM Generate 2 CRC Bytes Write F8 thru FB, in MFM Write FC in MFM Write FD in MFM Write FE in MFM Write FF in MFM

¹⁾ Missing clock transition between bits 4 and 5

Type IV Commands

The Force Interrupt command is generally used to terminate a multiple sector Read or Write command or to ensure Type I status in the Status Register. This command can be loaded into the Command Register at any time. If there is a current command under execution (Busy status bit set) the command will be terminated and the Busy status bit reset. The lower four bits of the command determine the conditional interrupt as follows:

- 10: Not-Ready to Ready Transition
- 11: Ready to Not-Ready Transition
- 12: Every Index Pulse
- 13: Immediate Interrupt

The conditional interrupt is enabled when the corresponding bit positions of the command (I3–I0) are set to a1. Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred. If I3–I0 are all set to zero (hex D0), no interrupt will occur but any command presently under execution will be immediately terminated. When using the immediate interrupt condition (I3 = 1), an interrupt will be immediately generated and the current

command terminated. Reading the status register or writing to the Command Register will not automatically clear the interrupt. The hex D0 is the only command that will enable the immediate interrupt (hex D8) to clear on a subsequent load Command Register or read Status Register operation, Follow a hex D8 with a D0 command. Wait 8 us (double density) or 16 µs (single density) before issuing a new command after a Force Interrupt command has been issued (times double when clock = 1 MHz). Loading a new command sooner than this will nullify the forced interrupt. Forced interrupt stops any command at the end of an internal microinstruction and generates INTRQ when the specified condition is met. Forced interrupt will wait until ALU operations in progress are completed (CRC calculations, comparisons, etc.). More than one condition may be set at a time. If, for example, the Ready to Not-Ready condition (I1 = 1) and the Every Index Pulse (I2 = 1) are both set, the resultant command will be hex DA. The OR function is performed so that either a Ready to Not-Ready or the next Index Pulse will cause an interrupt condition.

²⁾ Missing clock transition between bits 3 and 4

Formats

IBM 3740 Format - 128 Byte/Sector (8")

Shown below is the IBM single-density format with 128 byte/sector. In order to format a diskette, the user must issue the Write Track command, and load the Data Register with the following values. For every byte to be written, there is one data request.

	T
Number	Hex Value of
of Bytes	Byte Written
40	FF (or 00) ³⁾
6	00
1	FC (Index Mark)
26	FF (or 00)
1) 6	00
1	FE (ID Address Mark)
1	Track Number
1	Side Number (00 or 01)
1	Sector Number (1 thru 1A)
1	00
1	F7 (2 CRCs Written)
11	FF (or 00)
6	00
1	FB (Data Address Mark)
128	Data (E5)
1	F7 (2 CRCs Written)
27	FF (or 00)
247 ²⁾	FF (or 00)

IBM System 34 Format - 256 Byte/Sector (8")

Shown in the following table is the IBM double-density format with 256 byte/sector. In order to format a diskette the user must issue the Write Track command and load the Data Register with the following values. For every byte to be written, there is one data request.

Number	Hex Value of
of Bytes	Byte Written
80	4E
12	00
3	F6 (Writes C2)
1	FC (Index Mark)
50	4E
1) 12	00
3	F5 (Writes A1)
1	FE (ID Address Mark)
1	Track Number (0 through 4C)
1	Side Number (0 or 1)
1	Sector Number (1 through 1A)
1	01 (Sector Length)
1	F7 (2 CRCs Written)
22	4E
12	00
3	F5 (Writes A1)
1	FB (Data Address Mark)
256	Data (E5)
1	F7 (2 CRCs Written)
54	4E
598 ²⁾	4E

¹⁾ Write bracketed field 26 times.

²⁾ Continue writing until SAB 2793A/2797A interrupts out. Approx. 247 (598) byte.

³⁾ Optional '00' on SAB 2797A only is allowed.

Recommended - 128 Byte/Sector (Minidiskette)

Shown below is the recommended single-density format with 128 byte/sector. In order to format a diskette, the user must issue the Write Track command, and load the Data Register with the following values. For every byte to be written, there is one data request.

Syte Section Syte Written A0	Number	Hex Value of
1) 6 00 1 FE (ID Address Mark) 1 Track Number 1 Side Number (00 or 01) 1 Sector Number (1 through 10) 1 00 (Sector Length) 1 F7 (2 CRCs Written) 11 FF (or 00) 6 00 1 FB (Data Address Mark) 128 Data (E5) 1 F7 (2 CRCs Written) FF (or 00) 10 FF (or 00)	of Bytes	Byte Written
1 FE (ID Address Mark) 1 Track Number 1 Side Number (00 or 01) 1 Sector Number (1 through 10) 1 00 (Sector Length) 1 F7 (2 CRCs Written) FF (or 00) 6 00 1 FB (Data Address Mark) 128 Data (E5) 1 F7 (2 CRCs Written) FF (or 00)	40	FF (or 00)
1 Track Number 1 Side Number (00 or 01) 1 Sector Number (1 through 10) 1 00 (Sector Length) 1 F7 (2 CRCs Written) 11 FF (or 00) 6 00 1 FB (Data Address Mark) 128 Data (E5) 1 F7 (2 CRCs Written) 10 FF (or 00)	1) 6	00
1 Side Number (00 or 01) 1 Sector Number (1 through 10) 1 00 (Sector Length) 1 F7 (2 CRCs Written) FF (or 00) 6 00 1 FB (Data Address Mark) 128 Data (E5) 1 F7 (2 CRCs Written) FF (or 00)	1	FE (ID Address Mark)
1 Sector Number (1 through 10) 1 00 (Sector Length) 1 F7 (2 CRCs Written) 11 FF (or 00) 6 00 1 FB (Data Address Mark) 128 Data (E5) 1 F7 (2 CRCs Written) 10 FF (or 00)	1	Track Number
1 00 (Sector Length) 1 F7 (2 CRCs Written) 11 FF (or 00) 6 00 1 FB (Data Address Mark) 128 Data (E5) 1 F7 (2 CRCs Written) 10 FF (or 00)	1	Side Number (00 or 01)
1 F7 (2 CRCs Written) 11 FF (or 00) 6 00 1 FB (Data Address Mark) 128 Data (E5) 1 F7 (2 CRCs Written) 10 FF (or 00)	1	Sector Number (1 through 10)
11	1	00 (Sector Length)
6 00 1 FB (Data Address Mark) 128 Data (E5) 1 F7 (2 CRCs Written) 10 FF (or 00)	1	F7 (2 CRCs Written)
1 FB (Data Address Mark) 128 Data (E5) 1 F7 (2 CRCs Written) 10 FF (or 00)	11	FF (or 00)
128 Data (E5) 1 F7 (2 CRCs Written) 10 FF (or 00)	6	00
1 F7 (2 CRCs Written) 10 FF (or 00)	1	FB (Data Address Mark)
10 FF (or 00)	128	Data (E5)
, , , , , , , , , , , , , , , , , , ,	1	F7 (2 CRCs Written)
349 ²⁾ FF (or 00)	10	FF (or 00)
	349 ²⁾	FF (or 00)

Recommended – 256 Byte/Sector (Minidiskette)

Shown below is the recommended double-density format with 256 byte/sector. In order to format a diskette the user must issue the Write Track command and load the Data Register with the following values. For every byte to be written, there is one data request.

Number	Hex Value of
of Bytes	Byte Written
60	4E
1) 12	00
3	F5 (Writes A1)
1	FE (ID Address Mark)
1	Track Number (0 through 4C)
1	Side Number (0 or 1)
1	Sector Number (1 through 10)
1	01 (Sector Length)
1	F7 (2 CRCs Written)
22	4E
12	00
3	F5 (Write A1)
1	FB (Data Address Mark)
256	Data (E5)
1	F7 (2 CRCs Written)
24	4E
718 ²⁾	4E

Non-Standard Formats

Variations in the IBM formats are possible to a limited extent if the following requirements are met:

- 1. Sector size must be 128, 256, 512 or 1024 byte.
- Gap 2 cannot be varied from the recommended format.
- 3. 3 bytes of A1 must be used in MFM. In addition, the Index Address Mark is not required for operation by the SAB 2793A/2797A. Gap 1, 3, and 4 lengths can be as short as 2 bytes for SAB 2793A/2797A operation, however, PLL lock-up time, motor speed variation, write-splice area, etc., will add more bytes to each gap to achieve proper operation. It is recommended that the IBM format should be used for highest system reliability.

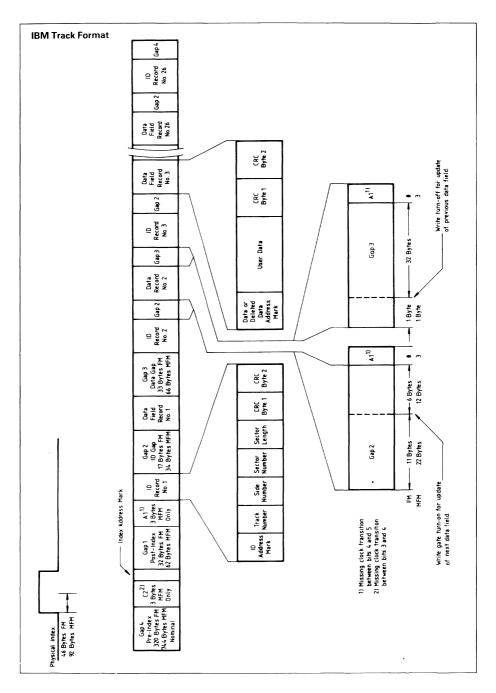
	FM	MFM
Gap I	16 Byte FF	32 Byte 4E
Gap II	11 Byte FF	22 Byte 4E
3)	6 Byte 00	12 Byte 00
		3 Byte A1
Gap III	10 Byte FF	24 Byte 4E
4)	4 Byte 00	8 Byte 00
		3 Byte A1
Gap IV	16 Byte FF	16 Byte 4E

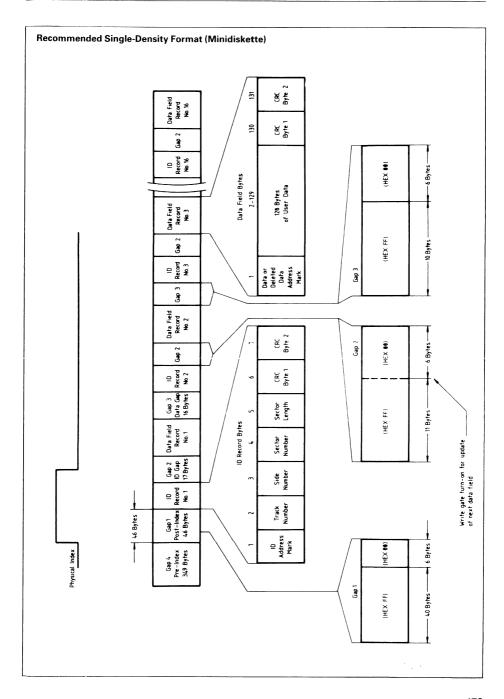
¹⁾ Write bracketed field 16 times.

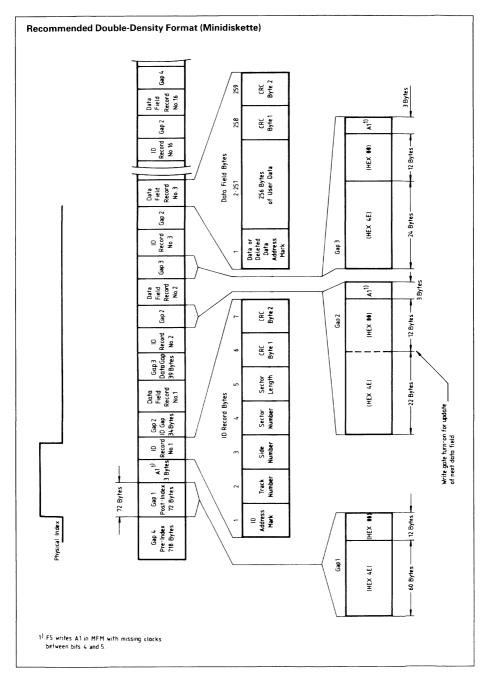
²⁾ Continue writing until SAB 2793A/2797A interrupts out. Approx. 349 (718) byte.

³⁾ Byte counts must be exact.

⁴⁾ Byte counts are minimum, except exactly 3 bytes of A1 must be written in MFM.







Absolut Maximum Ratings¹⁾

Ambient Temperature Under Bias

0 to + 70°C

Storage Temperature Voltage on Any Pin with -65 to +150°C

Respect to Ground (VSS)

Power Dissipation

-0.5 to +7V 2W

DC Characteristics

 $TA = 0 \text{ to } 70^{\circ}\text{C}; VCC = +5\%; VSS = 0V$

Symbol	Parameter	L	Limit Values			Test Condition
		Min.	Тур.	Max.		
IIL 1	Input Leakage Current 2)	-		10		VIN = VCC
IIL 2	Internal Leakage Current 2)	100	1	1700	ļιA	VIN = 0V
IOL	Output Leakage Current	_	1	10	7	VOUT = VCC
VIH	Input High Voltage	2.0	7	_		
VIL	Input Low Voltage	-	1	0.8	1	
VOH	Output High Voltage	2.4	1	-	\rfloor_{v}	$IOH = -100 \mu A$
VOL	Output Low Voltage	_	7	0.45	7 "	IOL = 1.6 mA
VOHP	Output High PUMP	2.2		_	1	IOHP = -1.0 mA
VOLP	Output Low PUMP	_	1	0.2	7	IOLP = +1.0 mA
ICC	Supply Current	-	70	150	mA	All outputs open

Capacitance³⁾

Symbol	Parameter	Limit Value (max.)	Unit	Test Condition
CIN	Input Capacitance	15	pF	Unmeasured pins
COUT	Output Capacitance	15	Pi	returned to GND

¹⁾ Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

²⁾ IIL 1 applies to normal inputs, IIL 2 to inputs with internal pull-up resistors on pins 1, 17, 19, 22, 36, 37, and 40. Also pin 25 on SAB 2793A.

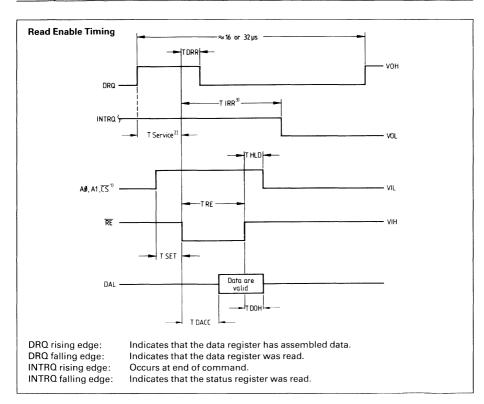
³⁾ This parameter is periodically sampled and not 100% tested.

AC Characteristics

TA = 0 to 70°C; VCC = +5V $\pm 5\%$; VSS = 0V. All timing readings at VOL = 0.8 V and VOH = 2.0 V.

Read Enable Timing

Symbol	Parameter	Limit Values			Unit	Test Condition
		Min.	Тур.	Max.		
TSET	Setup Addr. and CS to RE	50				
THLD	Hold Addr. and CS from RE	10]_	-		_
TRE	RE Pulse Width	200	7	1	CL = 50 pF	
TDRR	DRQ Reset from RE		100	200	ns	
TIRR	INTRO Reset from RE	-	500	3000		
TDACC	Data Valid from RE		100	200	7	
TDOH	Data Hold from RE	20	-	150	7	CL = 50 pF



¹⁾ $\overline{\text{CS}}$ may be permanently tied low if desired.

²⁾ T Service (worst case)

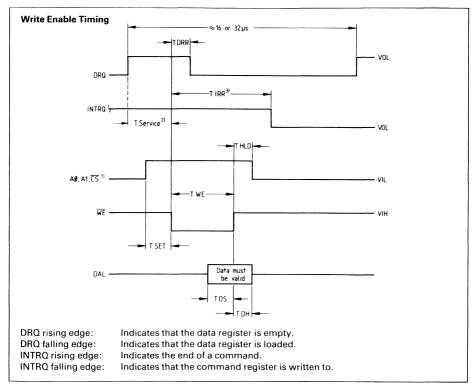
 $⁻FM = 27.5 \,\mu s$

 $^{^{3)}}$ Time doubles when CLK = 1 MHz.

 $⁻MFM = 13.5 \,\mu s$

Write Enable Timing

Symbol	Parameter	Limit Values			Unit	Test Condition
		Min.	Тур.	Max.		
TSET	Setup Addr. and CS to WE	50				
THLD	Hold Addr. and CS from WE	10]_	1- -		
TWE	WE Pulse Width	200	7			
TDRR	DRQ Reset from WE		100	200	ns	_
TIRR	INTRQ Reset from WE		500	3000	1	
TDS	Data Setup to WE	150				
TDH	Data Hold from WE	50	7	-		



¹⁾ CS may be permanently tied low if desired. When writing Data into Sector, Track or Data Register, the User cannot read this register until at least 4 μ s in MFM after the rising edge of WE. When writing into the Command Register status is not valid until some 28 μ s in FM/14 μ s in MFM later. These times double when CLK = 1 MHz.

 $^{^{2)}}$ T Service (worst case); FM = 23.5 $\mu s;$ MFM = 11.5 $\mu s.$

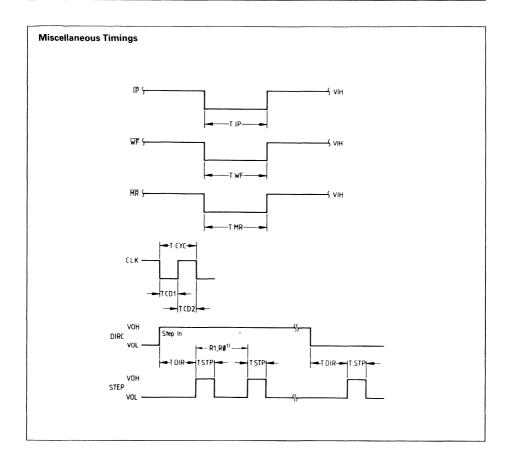
 $^{^{3)}}$ Time doubles when CLK = 1 MHz.

SAB 2793A/2797A

Miscellaneous Timings

Symbol	Parameter	L	imit Va	lues	Unit	Test Condition	
		Min.	Тур.	Max.			
TCD 1	Clock Duty (low)	230	250	20000	ns		
TCD 2	Clock Duty (high)	1230	250	20000	"	_	
TSTP 1)	Step Pulse Output	2 or 4	_				
TDIR	DIRC Setup to Step	I -	12]_	μS	±CLK Error	
TMR	Master Reset Pulse Width	50			μο		
TIP	Index Pulse Width	10					
RPW	Read Window Pulse Width	120 240	_	700 1400		MFM FM ±15% Input 0-5V	
	Precomp Adjust	100		300	ns	MFM Input 0 3V	
WPW	Write Data Pulse Width	200	300	400		Precomp = 100 ns MFM	
		600	900	1200		Precomp = 300 ns MFM	
vco	Free-Running Voltage-Controlled Oscillator	6.0	-			Cext = 0	
	Adjustable by Ext. Capacitor on Pin 26	_	4.0]-		Cext = 35 pF	
	PUMP Up +25%	5.0		1	MHz	PU = 2.2 V, Cext = 35 pF	
	PUMP Down -25%	-	1_	3.0	IVIDZ	$\overline{PD} \approx 0.2 \text{ V, Cext} = 35 \text{ pl}$	
	5% Change VCC	3.8	1	4.2		Cext = 35 pF	
		3.5		_		TA = 75°C, Cext = 35 pF	
	Adjustable External Capacitor	20	35	100	pF	VCO = 4.0 MHz rated	
RCLK	Derived Read Clock = VCO: 8, 16, 32		500			DDEN = 0 5/8 = 1	
			250		kHz	$ \begin{array}{ c c c c c } \hline DDEN = 0 \\ \hline 5/8 = 0 \end{array} $ VCO = 4.0	
			250			DDEN = 1 5/8 = 1	
			125			DDEN = 1 5/8 = 0	
PU/	PU/PD Time On (Pulse Width)		_	250	ns	MFM	
DON				500		FM	

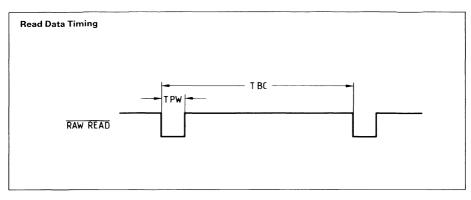
¹⁾ See stepping rates on page 13



SAB 2793A/2797A

Read Data Timing

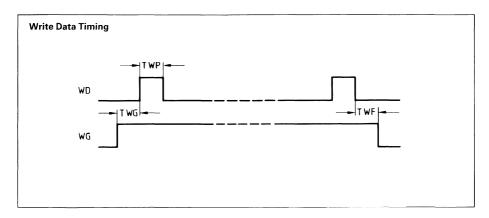
Symbol	Parameter	Limit Values		ues	Unit	Test Condition
		Min.	Тур.	Max.		
TPW	RAW READ Pulse Width	100	200		ns	_
TBC	RAW READ Cycle Time	1500	2000	<u> </u>	113	



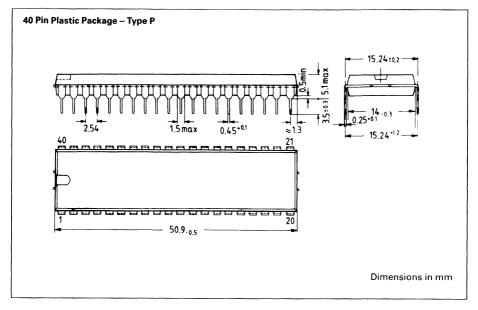
Write Data Timing

Symbol	Parameter	L	Limit Values			Test Condition
		Min.	Тур.	Max.		
TWP Write Data Pulse Width	Write Data Pulse Width	400	500	600	ns	FM
	Write Data i dise Width	200	250	300] '''3	MFM
TWG Write Gate to Write Data	Write Gate to Write Date	-	2			FM
	Write date to Write Data		1]	แร	MFM
TWF	Write Gate from WD	-	2	-	7	FM
			1			MFM

All times double when CLK = 1 MHz; no Write precompensation.



Package Outline



SAB 2793A/2797A

Ordering Information

Type	Description	Ordering Code
SAB 2793A-02-P	Floppy disk controller; true data bus, single-sided operation	Q67120-Y82
SAB 2797A-02-P	Floppy disk controller; true data bus, double-sided operation	Q67120-Y84

Advance Information

SAB 7201A Multi-Protocol Serial Communications Controller

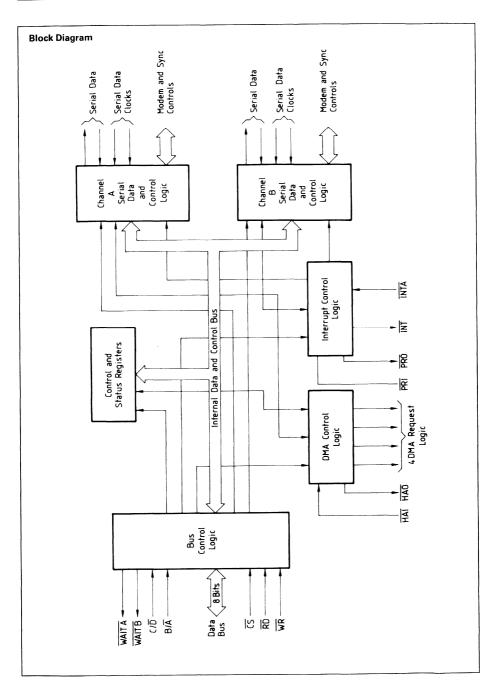
- Two independent full duplex serial channels
- Four independent DMA channels for transmitted/ received data for both serial inputs/outputs
- Programmable interrupt vectors and interrupt priorities
- Modem controls signals
- Variable software programmable data rate, up to 1.25 Mbaud at 5 MHz clock
- Double buffered transmitter data and quadruply buffered received data
- Programmable CRC algorithm
- Selection of interrupt, DMA or polling mode of operation
- Asynchronous operation
 - character length: 5, 6, 7, or 8 bits
 - stop bits: 1, 11/2, 2
 - Transmission speed: x1, x16, x32 or x64 clock frequency
 - parity: odd, even, or disable

- break generation and detection
- interrupt on parity, overrun or framing errors
- Monosync, bisync, and external sync operations
 - software selectable sync characters
 - automatic sync insertion
 - CRC generation and checking
- HDLC ans SDLC operations
 - abort sequence generation and detection
 - automatic zero insertion and detection
 - address field recognition
 - CRC generation and checking
 - I-field residue handling
- High-performance MYMOS technology
- Single +5V power supply; interfaces to most microprocessors including SAB 8080, 8085, 8086, and others
- Single-phase TTL clock
- Available in plastic dual-in line packages

Pin configuration	Pin names		
CLK 1	TxDA Transmit Data, Channel A and B	WAITA WAITB DO-D7 WR RD CS C/D B/A HAI HAO DTRA DTRB INT INTA PRI PRO	Wait Channel, A and B Data Bus Write Read Chip Select Control/Data Select Channel Select Hold Acknowledge In Hold Acknowledge Out Data Terminal Ready, Channel A and B Interrupt Request Interrupt Acknowledge Interrupt Priority In Interrupt Priority Out

The Siemens SAB 7201A Multi-Protocol Serial Communications Controller (MPSC) is designed to interface high-speed communications lines using asynchronous, IBM Bisync or HDLC/SDLC protocol. It can be interfaced with all Siemens

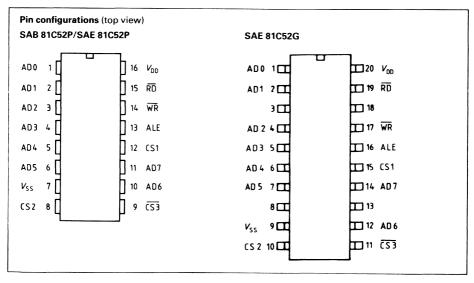
microcontrollers, 8 and 16-bit microprocessors and the SAB 8237 DMA controller in polled, interruptdriven, or DMA-driven modes of operation. The MPSC is a 40-pin device fabricated using Siemens high-performance MYMOS technology.



Preliminary

SAB 81C52, SAE 81C52 256×8-Bit static CMOS RAM NMOS-compatible

- 256 × 8-bit organization
- standby mode
- compatible with the μC/μP families SAB 8085, SAB 8088, SAB 8084, SAB 8051, the new SAB 80515, etc.
- very low power dissipation
- data retention up to VDD = 1V
- three different chip select inputs for two chip select modes
- no increasing power consumption in standby mode if the control inputs are on undefined potential
- Temperature range:
 SAB 81C52 0°C to 70°C
 SAE 81C52 -40°C to +85°C *¹
- Package DIP 16 or SO-20



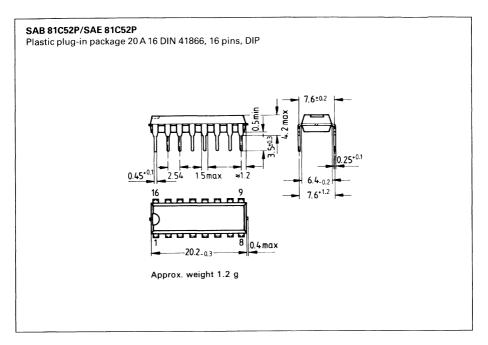
The SAB 81C52P is a CMOS silicon gate, static random access memory (RAM), organized as 256 words by 8 bits. The multiplexed address and data bus allows to interface directly to 8-bit NMOS microprocessors/microcomputers without any timing or level problems, e.g. the families SAB 8085, SAB 8088, SAB 8048, SAB 8051, and SAB 80515.

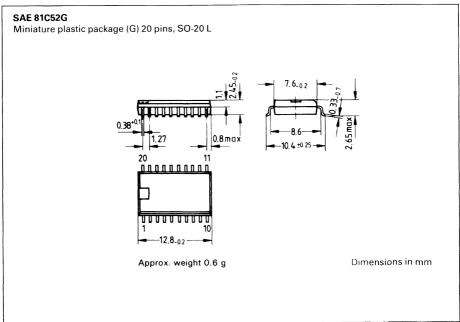
All inputs and outputs are fully compatible with NMOS circuits, except CS1. Data retention is given

to VDD \geq 1.0 V. The SAB 81C52P has three different inputs for two chip select modes which allow to inhibit either the address/data lines (AD0...AD7) and the control lines (\overline{WR} , \overline{RD} , ALE, CS2, $\overline{CS3}$), or only the control lines \overline{RD} , \overline{WR} .

The power consumption is max. $5.5\,\mu W$ in standby mode and max. $2.75\,mW$ in operation. In standby mode, the power consumption will not increase if the control inputs are on undefined potential.

^{*)} Values for applications up to -40°C to $+110^{\circ}\text{C}$ upon request.





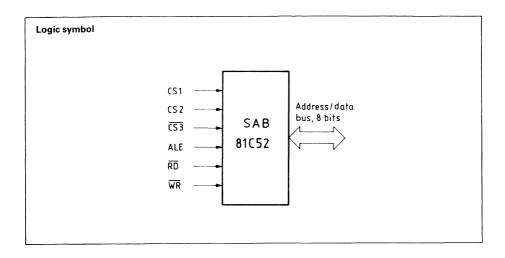
Preliminary data

Type	Ordering code	Package
SAB 81C52P	Q67100-Q486	DIP 16
SAE 81C52P	Q67100-H8003	DIP 16
SAE 81C52G	Q67100-H8004	SO-20

Pin designation

Pin No.		Symbol	Function
SAE 81C52G	SAB 81C52P SAE 81C52P		
1, 2, 4, 5, 6 7, 12, 14	16	AD0 7	Address/data lines
15	12	CS 1	Chip select 1 (standby) active low; inhibits all lines including control lines
16	13	ALE	Address latch enable
17	14	WR	Write enable
19	15	RD	Read enable
20	16	VDD	Power supply
9	7	VSS	GND
10	8	CS 2	Chip select 2; inhibits control inputs RD, WR
11	9	CS 3	Counterpart to CS 2

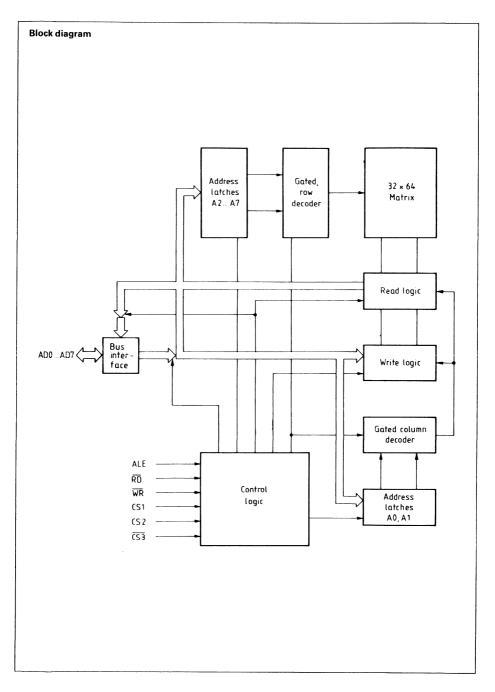
SAB 81C52/SAE 81C52



Truth table

CS 1	CS 2	CS 3	ALE	RD	WR	AD 0 AD 7	Function
L	*	*	*	*	*	floating (tristate) address to memory	standby store address
H H	X H	Ĺ	L	H	H	data from memory	read
H H	H	L X	L	H X	L X	data to memory floating (tristate)	write none
Н	X	Н	L	ĺχ	x	floating (tristate)	none

*: Level = VSS...VDD X: Level = LOW or HIGH



Maximum ratings

Maximum ratings are absolute limits. The integrated circuit may be destroyed if only a single value is exceeded.

Symbol	Parameter	Lin	Limit values		
		min.	max.		
VDD	Supply voltage reffered to GND (VSS)		-0.3 to 6	V	
VIM	All input and output voltages		VSS -0.3 VDD +0.3	V	
Ptot	Total power dissipation	-	250	mW	
PQ	Power dissipation for each output		50]	
Tj	Junction temperature		125	°C	
Tstg	Storage temperature		-55 to 125		
Rth SA	Thermal resistance		70	K/W	

Operating range

In the operating range, the functions shown in the circuit description will be fulfilled. Deviations from the electrical characteristics may be possible.

Symbol	Parameter	Li	mit value	Unit
		min.	max.	
VS	Supply voltage		4.5 to 5.5	V
Tamb	Ambient temperature: SAE 81C52		-40 to 85 *)	°C
	Ambient temperature: SAB 81C52		0 to 70	

^{*)} Values for applications up to 110 °C upon request

Electrical Characteristics

The electrical characteristics include the guaranteed tolerance of the values which the IC stays within for the specified operating range.

The typical characteristics are average values which can be expected from production. Unless otherwise specified, the typical characteristics apply to T_{amb} and the specified supply voltage.

DC Characteristics

SAE 81C52: Tamb = $-40\,^{\circ}\text{C}$ to $+85\,^{\circ}\text{C}$; **SAB 81C52:** Tamb = $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$; VDD = $4.5\,\text{V}$ to $5.5\,\text{V}$, VSS = $0\,\text{V}$

Symbol	Parameter	Limit	values	Unit	Test Condition
		min.	max.		
IDD	Standby supply current		1	цA	
IDD	Supply current		500]	f = 1 MHz
VDD	Standby voltage for data retention	1.0		V	
IIL	L input current (for each input)	1.0	1	μА	VI = 0 to VDD
IQIK	Output leakage current				VQ = 0 to VDD tri.
VIL	L input voltage	2.2	0.8		except CS1
VIH	H input voltage				
VQL	L output voltage		0.4		IQL = 1 mA
VQH	H output voltage	2.6	0.4	V	IQH = 1 mA
VIL	L input voltage CS1		1		
VIH	H input voltage CS1	VDD -1			

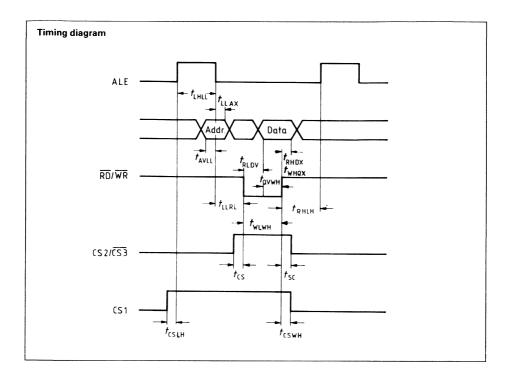
SAB 81C52/SAE 81C52

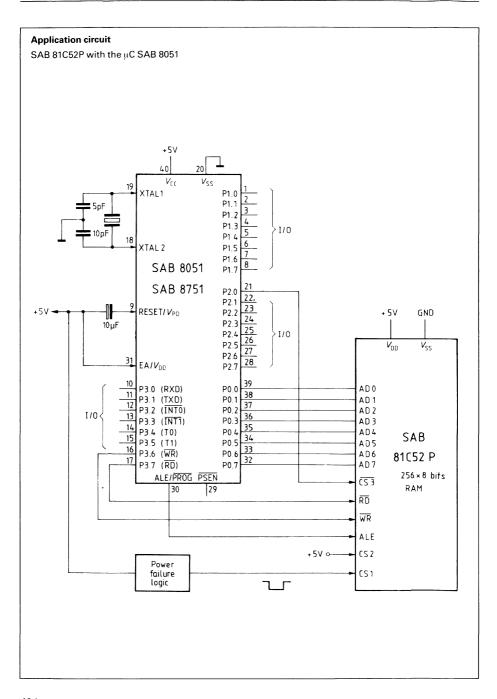
AC Characteristics

 $\begin{array}{ll} \textbf{SAE 81C52:} \;\; Tamb = -40\,^{\circ}\text{C to } +85\,^{\circ}\text{C *}); \\ \textbf{SAB 81C52:} \;\; Tamb = & 50\,^{\circ}\text{C to } & 70\,^{\circ}\text{C}; \\ \end{array} \right\} \hspace{0.5cm} VDD = 4.5\,\text{V to } 5.5\,\text{V; VSS} = 0\,\text{V}$

Symbol	Parameter	Li	mit values	Unit
		min.	max.	
TLHLL	ALE pulse width	100		
TLLRL	Ale low to RD low	50		
TRHLH	RD high to ALE high	30		
TLLWL	ALE low to WR low	50		
TWHLH	WR high to ALE high	30		
TAVLL	Address setup before ALE	25	_	
TLLAX	Address hold after ALE	20		
TWLWH	WR or RD pulse width	250		ns
TQVWH	Data setup before WR	100		
TWHQX	Data hold after WR	30		
TRHDX	Data hold after RD	-	90	
TCS	Chip select (2, 3) before \overline{RD} , \overline{WR}	50		
TSC	Chip select (2, 3) after RD, WR	50		:
TCSLH	Chip select 1 before ALE	20		
TCSWH	Chip select 1 after RD, WR	50		
TRLDV	Output delay time		200	
CI	Input capacitance against VSS (for each input)		10	pF

^{*)} Values for applications up to 110°C upon request

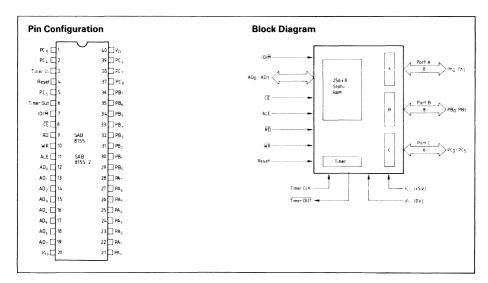




SAB 8155, 8155-2 2048 Bit Static MOS RAM with I/O Ports and Timer

- 256 Word × 8 Bits
- Single +5V Power Supply
- Completely Static Operation
- Internal Address Latch
- 2 Programmable 8-Bit I/O Ports
- 1 Programmable 6-Bit I/O Port

- Programmable 14-Bit Binary Counter/Timer
- Compatible with SAB 8085A and SAB 8088 CPU
- Multiplexed Address and Data Bus
- 40 Pin DIP



The SAB 8155 is a RAM and I/O chip to be used in the SAB 8085A and SAB 8088 microprocessor systems. The RAM portion is designed with 2048 static cells organized as 256×8. They have a maximum access time of 400ns to permit use with no wait states in SAB 8085A CPU. The SAB 8155-2 has a maximum access time of 330ns for use with the SAB 8085A-2 and the full speed 5MHz SAB 8088 CPU.

The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed to be status pins, thus allowing the other two ports to operate in handshake mode.

A 14-bit programmable counter/timer is also included on chip to provide either a square wave or terminal count pulse for the CPU system depending on timer mode. 5.82

Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function
PCØ-PC5	1, 2, 5, 37–39	1/0	PORT C – These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the command register. When PCØ-PC5 are used as control signals, they will provide the following: PCØ – A INTR (Port A Interrupt) PC1 – ABF (Port A Buffer Full) PC2 – A STB (Port A Strobe) PC3 – B INTR (Port B Interrupt) PC4 – B BF (Port B Buffer Full) PC5 – B STB (Port B Strobe)
TIMER IN	3	1	TIMER INPUT – Input to the counter/timer.
RESET	4	ı	RESET – Pulse provided by the SAB 8085A to initialize the system (connect to SAB 8085A RESET OUT). Input high on this line resets the chip and initializes the three I/O ports in input mode. The width of RESET pulse should typically be two SAB 8085A clock cycle times.
TIMER OUT	6	0	TIMER OUTPUT – This output can be either a square wave or a pulse, depending on the timer mode.
IO/M	7	I	I/O MEMORY – Selects memory if low and I/O and command/status registers if high.
CE	8	I	CHIP ENABLE – On this SAB 8155, this pin is $\overline{\text{CE}}$ and is ACTIVE LOW.
RD	9	I	READ CONTROL – Input low on this line with the Chip Enable active enables and AD0 – AD7 buffers. If IO/M pin is low, the RAM contents will be read out to the AD bus. Otherwise the contents of the selected I/O port or command/status registers will be read to the AD bus.
WR	10	I	WRITE CONTROL – Input low on this line with the Chip Enable active causes the data on the Address/Data bus to be written to the RAM or I/O ports and command/status register, depending on IO/\overline{M} .
ALE	11	I	ADDRESS LATCH ENABLE – This control signal latches both the address on the ADØ – AD7 lines and the state of the Chip Enable and IO/M into the chip at the falling edge of ALE.
ADØ-AD7	12-19	1/0	ADDRESS/DATA – 3-state Address/Data lines that interface with the CPU lower 8-bit Address-Data Bus. The 8-bit address is latched into the address latch inside the SAB 8155 on the falling edge of ALE. The address can be either for the memory section or the I/O section depending on the IO/ $\overline{\rm M}$ input. The 8-bit data is either written into the chip or read from the chip, depending on the $\overline{\rm WR}$ or $\overline{\rm RD}$ input signal.

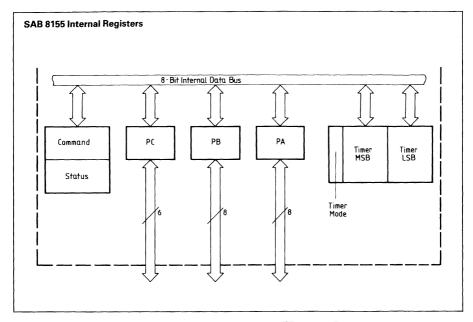
Symbol	Number	Input (I) Output (O)	Function
PAØ-PA7	21-28	1/0	PORT A – These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PBØ-PB7	29-36	1/0	PORT B – These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
· V _{cc}	40		POWER SUPPLY (+5V)
V_{SS}	20		GROUND (0 V)

Functional Description

The SAB 8155 contains the following:

- 2Kbit Static RAM organized as 256×8
- Two 8-bit I/O ports (PA & PB) and one 6-bit I/O port (PC)
- 14-bit timer-counter

The IO/ \overline{M} (IO/Memory Select) pin selects either the five registers (Command, Status, PA \emptyset -PA7, PB \emptyset -PB7, PC \emptyset -PC5) or the memory (RAM) portion.



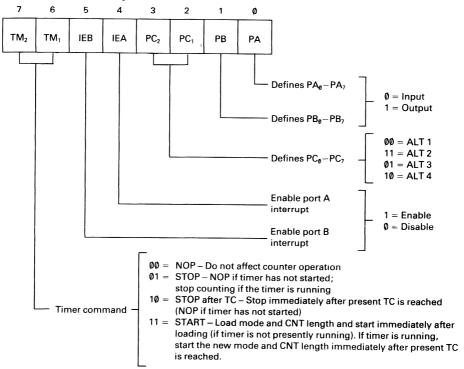
The 8-bit address on the Address/Data lines, Chip Enable input $\overline{\text{CE}}$, and $\text{IO}/\overline{\text{M}}$ are all latched on-chip at the falling edge of ALE.

Programming of the Command Register

The command register consists of eight latches. Four bits $(\emptyset-3)$ define the mode of the ports, two bits (4-5) enable or disable the interrupt from port C when it acts as control port, and the last two bits (6-7) are for the timer.

The command register contents can be altered at any time by using the I/O address XXXXX000 during a WRITE operation with the Chip Enable active and $10/\overline{M} = 1$. The meaning of each bit of the command byte is defined in the following figure. The contents of the command register may never be read.

Command Register Bit Assignment

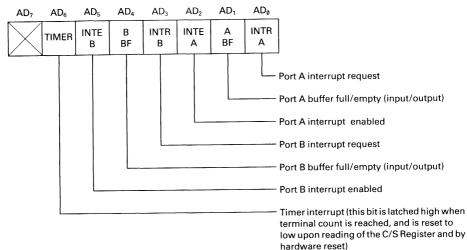


Reading the Status Register

The status register consists of seven latches, one for each bit; six $(\emptyset-5)$ for the status of the ports and one (6) for the status of the timer.

The status of the timer and the I/O section can be by reading the Status Register (Address XXXXX000). Status word format is shown in the following figure. Note that you may never write to the status register since the command register shares the same I/O address and the command register is selected when a write to that address is issued.

Status Register Bit Assignment Polled



Input/Output Section

The I/O section of the SAB 8155 consists of five registers (see following figure):

 Command/Status Register (C/S) – Both registers are assigned the address XXXXX000. The C/S address serves the dual purpose.

When the C/S registers are selected during WRITE operation, a command is written into the command register. The contents of this register are **not** accessible through the pins.

When the C/S (XXXXX000) is selected during a READ operation, the status information of the I/O ports and the timer becomes available on the AD0-AD7 lines.

• PA Register – This register can be programmed to be either input or – output ports depending on the status of the contents of the C/S Register. Also depending on the command, this port can operate in either the basic mode or the strobed mode (see timing diagram). The I/O pins assigned in relation to this register are PAØ–PA7. The address of this register is XXXXXX001.

- PB Register This register functions the same as PA Register. The I/O pins assigned are PBØ – PB7. The address of this register is XXXXXØ1Ø.
- PC Register This register has the address XXXXX011 and contains only 6 bits. The 6 bits can be programmed to be either input ports, output ports or as control signals for PA und PB by properly programming the AD2 and AD3 bits of the C/S register.

When PCO – PC5 is used as a control port, 3 bits are assigned for Port A and 3 for Port B. The first bit is an interrupt that the SAB 8155 sends out. The second is an output signal indicating whether the buffer is full or empty, and the third is an input pin to accept a strobe for the strobed input mode (see table Port Control Assignment).

When the 'C' port is programmed to either ALT3 or ALT4, the control signals for PA and PB are initialized as follows:

Control	Input Mode	Output Mode
BF	Low	Low
INTR	Low	High
STB	Input Control	Input Control

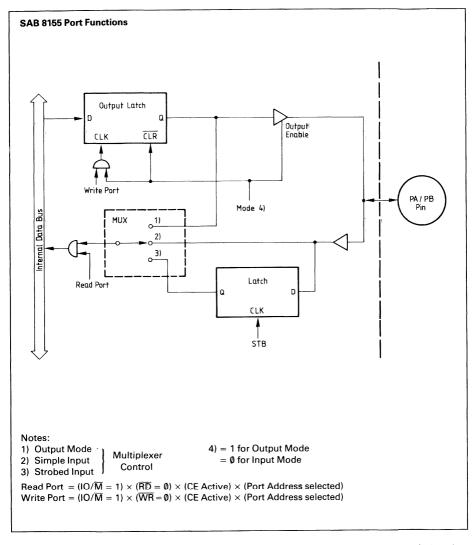
I/O Port and Timer Addressing Scheme

I/O Address *							Selection	
A7	A6	A5	A4	А3	A2	A1	AØ	
Х	х	х	х	Х	Ø	Ø	Ø	Interval Command/Status Register
X	×	х	×	×	ø	Ø	1	General Purpose I/O Port A
Х	Х	х	х	х	Ø	1	Ø	General Purpose I/O Port B
Х	х	х	х	Х	Ø	1	1	Port C – General Purpose I/O or Control
Х	х	х	х	х	1	Ø	Ø	Low-Order 8 bits of Timer Count
Х	х	х	х	х	1	Ø	1	High 6 bits of Timer Count and 2 bits of Timer Mode

X: Don't Care.

^{*:} I/O Address must be qualified by $\overline{CE} = \emptyset$ and $IO/\overline{M} = 1$ in order to select the appropriate register.





Note in the diagram that when the I/O ports are programmed to be output ports, the contents of the output ports can still be read by a READ operation when appropriately addressed.

The outputs of the SAB 8155 are "glitch-free" meaning that you can write a "1" to a bit position that was previously "1" and the level at the output pin will not change.

Note also that the output latch is cleared when the port enters the input mode. The output latch cannot be loaded by writing to the port if the port is in the input mode. The result is that each time a port mode is changed from input to output, the output pins will go low. When the SAB 8155 is RESET, the output latches are all cleared and all 3 ports enter the input mode.

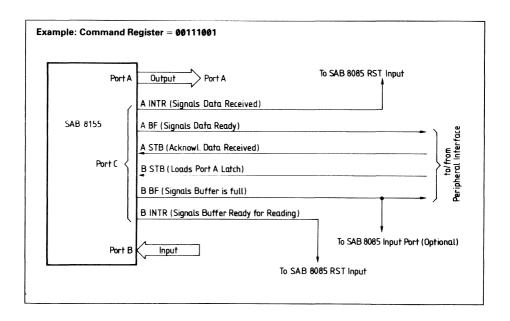
Port Control Assignment

nput Port	Output Port	A INTR (Port A Interrupt)	A INTR (Port A Interrupt)
nput Port	Output Port	A BF (Port A Buffer Full)	A BF (Port A Buffer Full)
nput Port	Output Port	A STB (Port A Strobe)	A STB (Port A Strobe)
nput Port	Output Port	Output Port	B INTR (Port B Interrupt)
nput Port	Output Port	Output Port	B BF (Port B Buffer Full)
nput Port	Output Port	Output Port	B STB (Port B Strobe)
r	pput Port pput Port pput Port pput Port	put Port Output Port	put Port Output Port A BF (Port A Buffer Full) put Port Output Port A STB (Port A Strobe) put Port Output Port Output Port put Port Output Port Output Port

When in the ALT1 or ALT2 modes, the bits of PORTC are structured like the diagram above in the simple input or output mode, respectively.

Next figure shows how the SAB 8155 I/O ports might be configured in a typical SAB 8085 system.

Reading from an input port with nothing connected to the pins will provide unpredictable results.

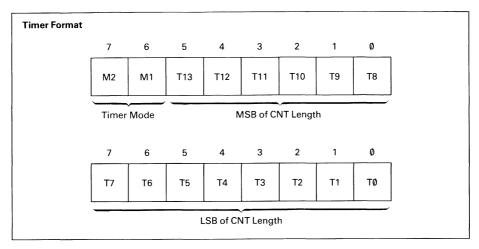


Timer Section

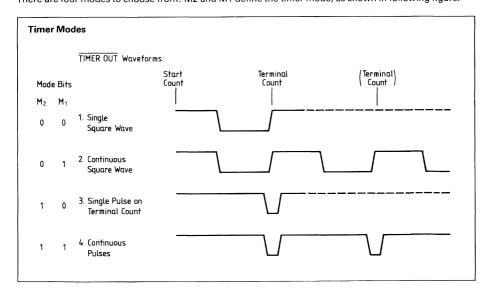
The timer is a 14-bit down-counter that counts the TIMER IN pulses and provides either a square wave or pulse when terminal count (TC) is reached.

The timer has the I/O address XXXXX100 for the low order byte of the register and the I/O address XXXXX101 for the high order byte of the register (see figure I/O Port and Timer Addressing Scheme).

To program the timer, the COUNT LENGTH REG is loaded first, one byte at a time, by selecting the timer addresses. Bits $\emptyset-13$ of the high order count register will specify the length of the next count and bits 14-15 of the high order register will specify the timer output mode (see next figure). The value loaded into the count length register can have any value from 2H through 3FFH in Bits $\emptyset-13$.



There are four modes to choose from: M2 and M1 define the timer mode, as shown in following figure.

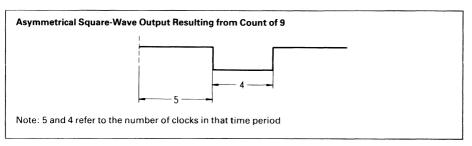


Bits 6–7 (TM2 and TM1) of command register contents are used to start and stop the counter. There are four commands to choose from:

TM2	TM1	Function NOP – Do not affect counter operation				
Ø	Ø					
Ø	1	STOP – NOP if timer has not startet; stop counting if the timer is running				
1	Ø	STOP AFTER TC – Stop immediately after present TC is reached (NOP if timer has n startet)				
, ,		START – Load mode and CNT length and start immediately after loading (if timer is not presently running). If timer is running, start the new mode and CNT length immediately after present TC is reached				

Note that while the counter is counting, you may load a new count and mode into the count length registers. Before the new count and mode will be used by the counter, you **must** issue a START command to the counter. This applies even though you may only want to change the count and use the previous mode.

In case of an odd-numbered count, the first halfcycle of the squarewave output, which is high, is one count longer than the second (low) half-cycle, as shown in next figure.



The counter in the SAB 8155 is not initialized to any particular mode or count when hardware RESET occurs, but RESET does stop the counting. Therefore, counting cannot begin following RESET until a START command is issued via the C/S register.

Please note that the timer circuit on the SAB 8155 chip is designed to be a square-wave timer, not an event counter. To achieve this, it counts down by twos twice in completing one cycle. Thus, its registers do not contain values directly representing the number of TIMER IN pulses received. You cannot load an initial value of 1 into the count register and cause the timer to operate, as its terminal count value is 10 (binary) or 2 (decimal). (For the detection of single pulses, it is suggested that one of the hardware interrupt pins on the SAB 8085A be used.) After the timer has started counting down, the values residing in the count registers can be used to calculate the actual number of TIMER IN pulses

required to complete the timer cycle if desired. To abtain the remaining count, perform the following operations in order:

- 1. Stop the count
- 2. Read in the 16-bit value from the count length registers
- 3. Reset the upper two mode bits
- Reset the carry and rotate right one position all 16 bits through carry
- 5. If carry is set. add 1/2 of the full original count (1/2 full count 1 if full count is odd)

Note:

If you started with an odd count and you read the count length register before the third count pulse occurs, you will not be able to discern whether one or two counts have occured. Regardless of this, the SAB 8155 always counts out the right number of pulses in generating the TIMER OUT waveforms.

SAB 8155

Absolute maximum ratings *)

Temperature Under Bias $0 \text{ to } +70^{\circ}\text{C}$ Storage Temperature $-65 \text{ to } +150^{\circ}\text{C}$ Voltage on any Pin with Respect to Ground Power Dissipation -0.5 to +7 V

D.C. Characteristics

 $T_A = 0$ to 70°C; $V_{CC} = 5 \text{ V } \pm 5\%$

Symbol	Parameter	Limit Values		Units	Test Conditions
		Min.	Max.		
V _{IL}	Input Low Voltage	-0.5	0.8		-
V _{iH}	Input High Voltage	2.0	V _{CC} +0.5	v	
V _{OL}	Output Low Voltage	-	0.45		$I_{OL} = 2 \text{ mA}$
V _{OH}	Output High Voltage	2.4	_		$I_{\text{OH}} = -400 \mu\text{A}$
I _{IL}	Input Leakage		±10	μА	$V_{\rm IN} = V_{\rm CC}$ to 0 V
I _{LO}	Output Leakage		1 - 10	μΑ	$0.45 \mathrm{V} \leq V_{\mathrm{OUT}} \leq V_{\mathrm{CC}}$
I _{CC}	V _{cc} Supply Current		180	mA	-
I _{IL} (CE)	Chip Enable Leakage		+100	μА	$V_{\rm IN} = V_{\rm CC}$ to 0 V

^{*)} Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

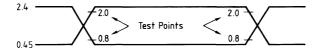
A.C. Characteristics

 $T_{\rm A} = 0$ to 70°C; $V_{\rm CC} = 5 \, \text{V} \pm 5\%$

Symbol	Parameter		Lim	it Values		Units
		SAB 8155		SA	SAB 8155-2	
		Min.	Max.	Min.	Max.	
t _{AL}	Address to Latch Set Up Time	50				
t _{LA}	Address Hold Time after Latch	80	_	30	_	
t _{LC}	Latch to READ/WRITE Control	100		40		
t _{RD}	Valid Data Out Delay from READ Control		170		140	
t _{AD}	Address Stable to Data Out Valid		400		330	
t _{LL}	Latch Enable Width	100	-	70	_	
t _{RDF}	Data Bus Float After READ	0	100	0	80	
t _{CL}	READ/WRITE Control to Latch Enable	20		10		
t _{cc}	READ/WRITE Control Width	250		200		
t _{DW}	Data In to WRITE Set Up Time	150	_	100	_	
t _{wD}	Data In Hold Time After WRITE	0		0		
t _{RV}	Recovery Time Between Controls	300		200		
t _{wP}	WRITE to Port Output	-	400	_	300	ns
t _{PR}	Port Input Setup Time	70	-	50	_	
t _{RP}	Port Input Hold Time	50	-	10	_	
t _{SBF}	Strobe to Buffer Full	-	400	-	300	
t _{ss}	Strobe Width	200	-	150	_	7
t _{RBE}	READ to Buffer Empty					
t _{sı}	Strobe to INTR ON]-	400	-	300	
t _{RDI}	READ to INTR Off					
t _{PSS}	Port Setup Time to Strobe Strobe	50	_	0		
t _{PHS}	Port Hold Time After Strobe	120		100		
t _{sbe}	Strobe to Buffer Empty					7
t _{wBF}	WRITE to Buffer Full					
t _{wi}	WRITE to INTR Off]-	400	-	300	
t _{TL}	TIMER-IN to TIMER-OUT Low					
t _{TH}	TIMER-IN to TIMER-OUT High					
t _{RDE}	Data Bus Enable from READ Control	10		10		
t ₁	TIMER-IN Low Time	80]_	40	7-	
t ₂	TIMER-IN High Time	120		70		

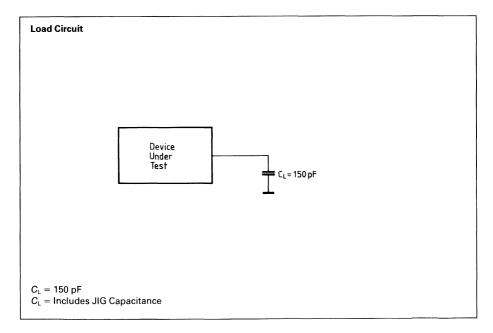
A.C. Testing

Input/Output Waveform

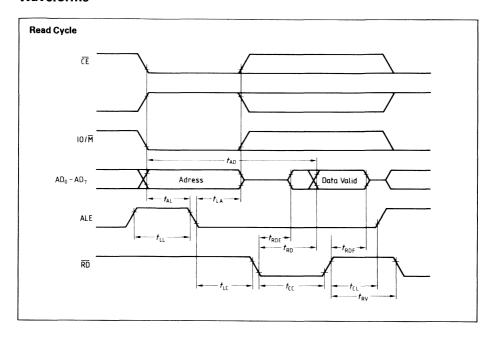


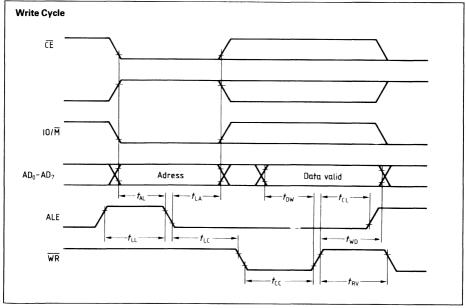
A.C. Testing: Inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0".

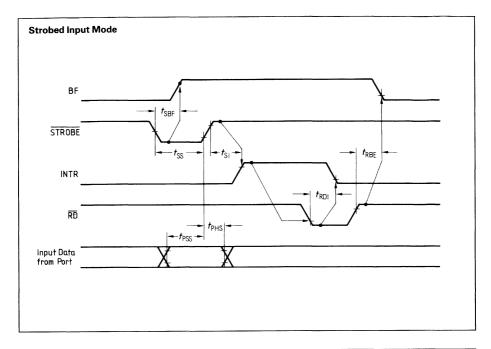
Timing Measurements are made at 2.0V for Both a Logic "1" and 0.8V for a Logic "0".

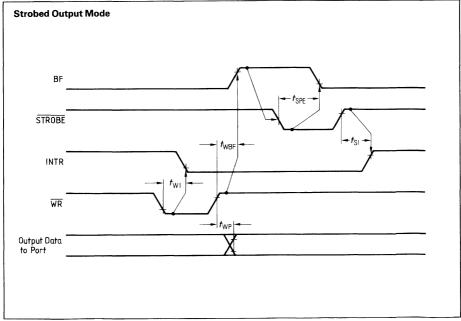


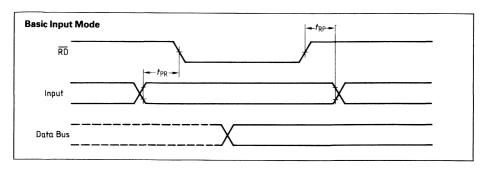
Waveforms

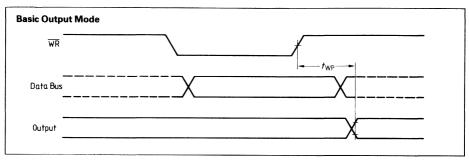


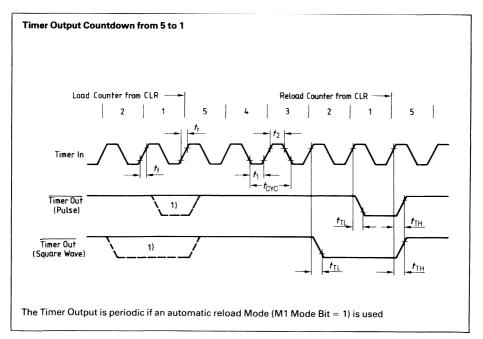




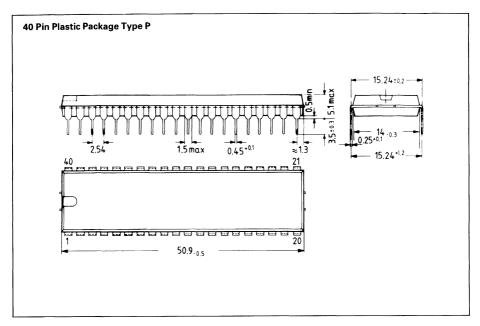








Package Outline



Ordering Information

Туре	Description	Ordering code
	RAM with I/O Port and Timer	
SAB 8155-P	Plastic	Q 67120-Q 42
SAB 8155-2-P	Plastic	Q 67120-Q 86

P_{reliminary} 87A-5

SAB 8237A, SAB 8237A-5 High Performance Programmable DMA Controller

- Four Independent DMA Channels
- Enable/Disable Control of Individual DMA Requests
- Memory-to-Memory Transfers
- Memory Block Initialization
- Address Increment or Decrement
- Independent Autoinitialization of all Channels
- High performance: Transfers up to 1.6
 MBytes/Second with 5 MHz SAB 8237A-5

- Directly Expandable to any Number of Channels
- End of Process Input for Terminating Transfers
- Software DMA Requests
- Independent Polarity Control for DREQ and DACK Signals
- Single +5V Power Supply
- 40 Pin Dual-In-Line Package
- Fully compatible with the Industry Standard 9517A/8237A

Pin Configuration		Pin Names	
IOR 0	40 A7	DB7-DBØ	Data Bus (bidirectional)
ĬŌ₩ ☐ 2	39 A6	IOR, IOW	I/O Read and Write Input/Output
ΜΕΜΆ □ 3 ΜΕΜ ₩ □ 4	38 A5	MEMR, MEMW	Memory Read and Write Output
(Note1) 5	36 E E O P	AØ-A3	Address Input/Output
READY 6	35 A3	A4-A7	Adress Output
HLDA 7	34 A 2 33 A 1	CS	Chip Select Input
AEN 3 SAB	32 A0	CLK	Clock Input
HRQ 10 8237A	_5 31	READY	Ready Input
₹ ☐ 11 € LK ☐ 12	30 DB0 29 DB1	HRQ	Hold Request Output
RESET 13	28 DB2	HLDA	Hold Acknowledge Input
DACK 2 14 DACK 3 15	27 DB3 26 D 084	RESET	Reset Input
DREQ3 16	25 DACKO	DREQØ-DREQ3	DMA Request Input
DREQ 2 17	24 DACK1	DACKØ-DACK3	DMA Acknowledge Output
DREQ.1 18	23 DB5 22 DB6	AEN	Address Enable Output
GND 20	21 087	ADSTB	Address Strobe Output
1) Pin always tied high		EOP	End of Process Input/Output

The SAB 8237A Multimode Direct Memory Access (DMA) Controller is designed to improve system performance by allowing external devices to directly transfer information to or from system memory. Memory-to-memory transfer capability is also provided.

The SAB 8237A contains four independent channels, each with a separate register set, and may be expanded to any number of channels by cascading additional controller chips. The three basic transfer modes allow programmability of the types of

DMA service by the user. Each channel can be individually programmed to Autoinitialize to its original state following an End of Process (EOP). Each channel has a full 64K address and word count capability.

The SAB 8237A is fabricated in $+5\,\text{V}$ advanced N-channel, silicon gate Siemens MYMOS technology and packaged in a 40-pin DIP. The SAB 8237A-5 is the 5 MHz version of the standard 3 MHz SAB 8237A respectively.

3.85

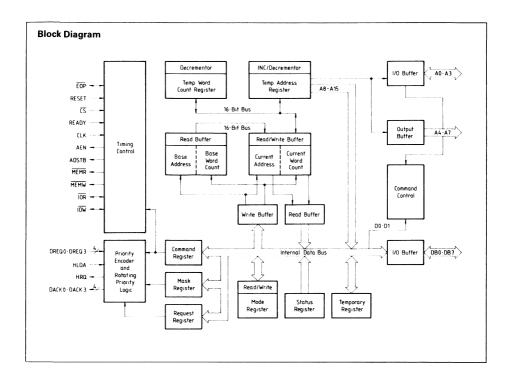
Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function	
IOR	1	1/0	I/O READ I/O Read is a bidirectional active low three-state line. In the idle cycle, it is an input control signal used by the CPU to read the control registers. In the Active cycle, it is an output control signal used by the SAB 8237A to access data from a peripheral device during a DMA Write transfer.	
ĪÓW	2	I/O	I/O WRITE I/O Write is a bidirectional active low three-state line. In the idle cycle it is an input control signal used by the CPU to load information into the SAB 8237A. In the Active cycle it is an output control signal used by the SAB 8237A to load data to a peripheral device during a DMA Read transfer. Write operations by the CPU to the SAB 8237A require a rising IOW edge following each data byte transfer. It is not sufficient to hold the IOW pin low and toggle CS.	
MEMR	3	0	MEMORY READ The Memory Read signal is an active low three-state output used to access data from the selected memory location during a memory-to-peripheral or a memory-to-memory transfer.	
MEMW	4	0	MEMORY WRITE The Memory Write signal is an active low three-state output used to write data to the selected memory location during a peripheral-to-memory or a memory-to-memory transfer.	
_	5	1	Pin 5 must be tied high.	
READY	6	1	READY Ready is an input used to extend the memory read and write pulses from the SAB 8237A to accommodate slow memories or I/O peripheral devices. Ready must not make transitions during its specified setup/hold time.	
HLDA	7	1	HOLD ACKNOWLEDGE The active high Hold Acknowledge from the CPU indicates that control of the system busses has been relinquished.	
ADSTB	8	0	ADDRESS STROBE The active high Address Strobe is used to strobe the upper address byte from DBØ-DB7 into an external latch.	
AEN	9	0	ADDRESS ENABLE Address Enable is an active high signal used to disable the system bus during DMA cycles and to enable the output of the external latch which holds the upper byte of the address. Note that during DMA transfers HLDA and AEN should be used to deselect all other I/O peripherals which may erroneously be accessed as programmed I/O during the DMA operation. The SAB 8237A automatically deselects itself by disabling the CS input during DMA transfers.	

Symbol	Number	Input (I) Output (O)	Function	
HRQ	10	0	HOLD REQUEST The Hold Request to the CPU is used by the DMA to request control of the system bus. Software requests or unmasked DREQs cause the SAB 8237A to issue HRQ.	
CS	11	1	CHIP SELECT Chip Select is an active low input used to select the SAB 8237A as an I/O device during an I/O Read or I/O Write by the host CPU. This allows CPU communication on the data bus. During multiple transfers to or from the SAB 8237A by the host CPU CS may be held low providing IOR or IOW is toggled following each transfer.	
CLK	12	I	CLOCK This input controls the internal operations of the SAB 8237A and its rate of data transfers. The input may be driven at up to 3 MHZ for the standard SAB8237A and up to 5 MHz for the SAB 8237A-5.	
RESET	13	ı	RESET Reset is an asynchronous active high input which clears the Command, Status, Request and Temporary register. It also clears the First/Last Flip/Flop and sets the Mask register. Following a Reset the device is in the idle cycle.	
DACKØ DACK1 DACK2 DACK3	25 24 14 15	0 0 0 0	DMA ACKNOWLEDGE The DMA Acknowledge lines indicate that a channel is active. In many systems they will be used to select a peripheral. Only one DACK will be active at a time and none will be active unless the DMA is in control of the bus. The polarity of these lines is programmable. Reset initializes them to active-low.	
DREQØ DREQ1 DREQ2 DREQ3	19 18 17 16	 	DMA REQUEST The DMA Request lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service in Fixed Priority, DREQØ has the highest priority and and DREQØ has the highest priority and and DREQØ has the howest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of DREQ signal. The Polarity of DREQ is programmable. Reset initializes these lines to active high.	
DBØ-DB7	30-26, 23-21	1/0	DATA BUS The Data Bus lines are bidirectional three-state signals connected to the system data bus. The outputs are enabled during the I/O Read by the host CPU, permitting the CPU to examine the contents of an Address register, the Status register, the Temporary register or a Word Count register. The Data Bus is enabled to input data during a host CPU I/O write, allowing the CPU to program the SAB 8237A control registers. During DMA cycles the most significant eight bits of the address are output onto the data bus to be strobed into an external latch by ADSTB. In memory-to-memory operations data from the source memory location comes into the SAB 8237A's Temporary register on the read-from-memory half of the operation. On the write-to-memory half of the operation, the data bus outputs the Temporary register data into the destination memory location.	

SAB 8237A

Symbol	Number	Input (I) Output (O)	Function	
A0-A3	32–35	1/0	ADDRESS Ø-3 The four least significant address lines are bidirectional 3-state signals. During DMA idle cycles they are inputs and allow the host CPU to load or read control registers. When the DMA is active, they are outputs and provide the lower 4-bits of the output address.	
A4-A7	37–40	0	ADDRESS 4–7 The four most significant address lines are three-state outp and provide four bits of address. These lines are enabled oduring DMA service.	
ЕОР	36	1/0	END OF PROCESS $\overline{\text{EOP}}$ is an active low bidirectional open-drain signal providing information concerning the completion of DMA service. When a channel's Word Count goes to zero, the SAB 8237A pulses $\overline{\text{EOP}}$ low to provide the peripheral with a completion signal. $\overline{\text{EOP}}$ may also be pulled low by the peripheral to cause premature completion. The reception of $\overline{\text{EOP}}$, either internal or external, causes the currently active channel to terminate the service, to set its TC bit in the Status register and to reset its request bit. If Autoinitialization is selected for the channel, the current registers will be updated from the base registers. Otherwise the channel's mask bit will be set and the register contents will remain unaltered. During memory-to-memory transfers, $\overline{\text{EOP}}$ will be output when the TC for channel 1 occurs. $\overline{\text{EOP}}$ always applies to the channel with an active DACK; external $\overline{\text{EOP}}$ s are disregarded when DACK0-DACK3 are all inactive if the DMA is in state SI. In situations where two or more SAB 8237A DMAs are cascaded, the $\overline{\text{EOP}}$ pins should be logically OR'ed (not wire-OR'ed). Because $\overline{\text{EOP}}$ is an open-drain signal, an external pullup resistor is required. Values of 3.3 k Ω or 4.7 k Ω are recommanded; the $\overline{\text{EOP}}$ pin cannot sink the current passed by a 1 k Ω pullup.	
VCC	31	_	POWER SUPPLY (+5V)	
GND	20	-	GROUND (0 V)	
			the state of the s	



Register Description

Current Address Register

Each channel has a 16-bit Current Address register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the intermediate values of the address are stored in the Current Address register during the transfer.

Current Word Count Register

Each channel has a 16-bit Current Word Count register. This register should be programmed with, and will return on a CPU read, a value one less than the number of words to be transferred. The word count is decremented after each transfer. The intermediate value of the word count is stored in the register during the transfer. When the value

in the register goes to zero, a TC will be generated.

Base Address and Base Word Count Registers

Each channel has a pair of Base Address and Base Word Count registers. These 16-bit registers store the original values of their associated current registers. During Autoinitialize these values are used to restore the current registers to their original values. The base registers are written simultaneously with their corresponding current register in 8-bit bytes during DMA programming by the microprocessor.

Command Register

This 8-bit register controls the operation of the SAB 8237A. It is programmed by the microprocessor in the Program Condition and is cleared by Reset.

Mode Registers

Each channel has a 6-bit Mode register associated with it. When the register is being written to by the microprocessor in the Program Condition, bits 0 and 1 determine which channel Mode register is to be written.

Request Register

The SAB 8237A can respond to requests for DMA service which are initiated by software as well as by a DREO. Each channel has a request bit associated with it in the 4-bit Request register. These are nonmaskable and subject to prioritization by the Priority Encoder network. Each register bit is set or reset separately under software control or is cleared upon generation of a TC or external EOP. The entire register is cleared by a Reset.

Mask Register

Each channel has associated with it a mask bit which can be set to disable the incoming DREQ. Each mask bit is set when its associated channel produces an EOP if the channel is not programmed for Autoinitialize. Each bit of the 4-bit Mask register may also be set or cleared separately under software control. The entire register is also set by a Reset.

Status Register

The Status registers may be read out of the SAB 8237A by the microprocessor. It indicates which channels have reached a terminal count and which channels have pending DMA requests.

Temporary Register

The Temporary register is used to hold data during memory-to-memory transfers. Following the completion of the transfers, the last word moved can be read by the microprocessor in the Program Condition.

Functional Description

DMA Operation

The SAB 8237A is designed to operate in two major cycles. These are called Idle and Activa cycles. Each device cycle is made up of a number of states. State I (SI)is the inactive state. It is entered when the SAB 8237A has no valid DMA requests pending. While in SI, the DMA controller is inactive but may be in the Program Condition, being programmed by the processor. State Ø (SØ) is the first state of a DMA service. The SAB 8237A has requested a hold but the processor has not yet returned an acknowledge. An acknowledge from the CPU will signal that transfers may begin, S1, S2, S3 and S4 are the working states of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wait states (SW) can be inserted before S4 by the use of the Ready line on the SAB 8237A.

Memory-to-memory transfers require a read-from and a write-to-memory to complete each transfer. The states, which resemble the normal working states, use two digit numbers for identification. Eight states are required for each complete transfer. The first four states (S11, S12, S13, S14) are used for the read-from-memory half and the last four states (S21, S22, S23 and S24) for the write-to-memory half of the transfer.

Idle Cycle

When no channel is requesting service, the SAB 8237A will enter the Idle cycle and perform "SI" states. In this cycle the SAB 8237A will sample the DREQ lines every clock cycle to determine if any channel is requesting a DMA service. The device will also sample $\overline{\text{CS}}$, looking for an attempt by the microprocessor to write or read the internal registers of the SAB 8237A.

Active Cycle

When the SAB 8237A is in the Idle cycle and a channel requests a DMA service, the device will output a HRQ to the microprocessor and enter the Active cycle. It is in this cycle that the DMA service will take place, in one of four modes:

Single Transfer Mode

In Single Transfer mode, the SAB 8237A will make a one-byte transfer during each HRQ/HLDA handshake. When DREQ goes active, HRQ will go active. After the CPU responds by driving HRQ active, a one-byte transfer will take place. Following the transfer, HRQ will go inactive, the word count will be decremented and the address will be either incremented or decremented.

Block Transfer Mode

In Block Transfer mode, the SAB 8237A will continue making transfers until a TC (caused by the word count going to zero) or an external End of Process (EOP) is encountered.

Demand Transfer Mode

In Demand Transfer mode the device will continue making transfers until a TC or external $\overline{\text{EOP}}$ is encountered or until DREQ goes inactive. Thus, the device requesting service may discontinue transfers by bringing DREQ inactive. Service may be resumed by asserting an active DREQ once again.

Cascade Mode

This mode is used to cascade more than one SAB 8237A together for simple system expansion. The HRQ and HLDA signals from the additional SAB 8237A are connected to the DREQ and DACK signals of a channel of the initial SAB 8237A.

TRANSFER TYPES

Each of the three active transfer modes can perform three different types of transfers. These are Read, Write and Verify. Write transfers move data from an I/O device to the memory by activating $\overline{\text{IOR}}$ and $\overline{\text{MEMW}}$. Read transfers move data from memory to an I/O device by activating $\overline{\text{MEMR}}$ and $\overline{\text{IOW}}$. Verify transfers are pseudo transfers; the SAB8237A operates as in Read or Write transfers generating addresses, responding to $\overline{\text{EOP}}$, etc., however, the memory and I/O control lines remain inactive.

Memory-to-Memory

The SAB8237A includes a block move capability that allows blocks of data to be moved from one memory adress space to another. Channel 0 forms the source address and channel 1 forms the destination address. The channel 1 word count is used. A memory-to-memory transfer is initiated by setting a software DMA request for channel 0.

Autoinitialize

By programming a bit in the Mode register a channel may be set up for an Autoinitialize operation. During Autoinitialization, the original values of the Current Address and Current Word Count registers are automatically restored from the Base Address and Base Word Count registers of that channel following EOP.

Extended Write

For Flyby Transactions late write is normally used, as this allows sufficient time for the \overline{IOR} signal to get data from the peripheral onto the bus before \overline{MEMW} is activated. In some systems, performance can be improved by starting the write cycle earlier.

Address Generation

In order to reduce pin count, the SAB 8237A multiplexes the eight higher order address bits on the data lines. State S1 is used to output the higher order address bits to an external latch from which they may be placed on the address bus. The falling edge of Address Strobe (ADSTB) is used to load these bits from the data lines to the latch. Address Enable (AEN) is used to enable the bits onto the address bus through the 3-state enable control signal of the latch. The lower order address bits are output by the SAB 8237A directly. To save time and speed transfers, the SAB 8237A executes S1 states only when updating of A8–A15 in the latch is necessary.

Compressed Timing

In order to achieve even greater throughput where system characteristics permit, the SAB 8237A can compress the transfer time to two clock cycles. By removing state S3 the read pulse width is made equal to the write pulse width and a transfer consists only of state S2 to change the address and state S4 to perform the read/write.

Priority

The SAB 8237A has two types of priority encoding available as software selectable options. The first is Fixed Priority which fixes the channels in priority order based upon the descending value of their number. The channel with the lowest priority is 3 followed by 2, 1 and the highest priority channel Ø. The second schema is Rotating Priority. The last channel to get service becomes the lowest priority channel with the others rotating accordingly.

Software Commands

There are two special software commands which can be executed in the Program Condition.
Clear First/Last Flip/Flop: This command may be issued prior to writing or reading SAB 8237A address or word count information. This initializes the Flip/Flop to a known state so that subsequent accesses to register contents by the microprocessor will address lower and upper bytes in the correct sequence.

Master Clear: This software instruction has the same effect as the hardware Reset. The Command, Status, Request, Temporary and Internal First/Last Flip/Flop registers are cleared and the Mask register is set.

Absolute Maximum Ratings 1)

Ambient Temperature Under Bias	0 to	70°C
Storage Temperature	-65 to + 1	50°C
Voltage on Any Pin with Respect to Ground (VSS)	-0.5 to $+$	7 V
Power Dissipation		2 W

D.C. Characteristics

TA = 0 to 70°C; VCC = $5V \pm 5\%$; VSS = 0V

Symbol	Parameter		Limit Valu	ies	Unit	Test Condition	ND.	
	Turumeter	Min.	Typ. 2)	Max.	Oint	rest condition		
VOH	Output High Voltage	2.4				/OH = -200	μΑ	
		3.3				/OH = -100 µ	A (HRQ only)	
VOL	Output Low Voltage	_		0.40	v	IOL = 3.2 m/	4	
VIH	Input High Voltage	2.0	_	VCC+0.5				
VIL	Input Low Voltage	-0.5		0.8				
/LI	Input Load Current			±10	uА	0 V ≤ VIN ≤ V	/CC	
/LO	Output Leakage Current			10	μA	$0.4 \text{V} \leq V \text{OUT} < V \text{CC}$		
/CC	VCC Supply Current		110	130	mA	$TA = +25^{\circ}C$	All outputs	
			130	150		TA = 0°C	discon- nected	
со	Output Capacitance		4	8				
CI	Input Capacitance		8	15	рF	fc = 1.0 MHz,	Inputs = 0 V	
CIO	I/O Capacitance		10	18				

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

²⁾ Typical values are for $TA = 25^{\circ}C$, nominal supply voltage and nominal processing parameters.

A.C. Characteristics

TA = 0 to $70^{\circ}C$; $VCC \approx 5 V \pm 5\%$; VSS = 0 V

DMA (Master) Mode

Symbol	Parameter		Limit	Values		Unit
		823	37A	823	7A-5	
		Min.	Max.	Min.	Max.	
TAEL	AEN High from CLK Low (S1) Delay Time		300		200	
TAET	AEN Low from CLK High (S1) Delay Time		200		130	
TAFAB	ADR Active to Float Delay from CLK High	_	150	_	90	
TAFC	READ or WRITE Float from CLK High		150		120	
TAFDB	DB Active to Float Delay from CLK High		250		170	
TAHR	ADR from READ High Hold Time	TCY-100		TCY-100		
TAHS	DB from ADSTB Low Hold Time	50	-	40	-	
TAHW	ADR from WRITE High Hold Time	TCY -50		TCY -50		
	DACK Valid from CLK Low Delay Time 1)		250		170	
TAK	EOP High from CLK High Delay Time 2)	_	250]_	170	
	EOP Low to CLK High Delay Time		250		170	
TASM	ADR Stable from CLK High		250		170	
TASS	DB to ADSTB Low Setup Time	100		100	ns	ns
TCH	CLK High Time (transitions ≤ 10 ns)	120	_	80	_	
TCL	CLK Low Time (transitions ≤ 10 ns)	150		68		
TCY	CLK Cycle Time	320		200		
TDCL	CLK High to READ or WRITE Low Delay 3)		270		190	
TDCTR	READ High from CLK High (S4) Delay Time ³⁾		270		190	
TDCTW	WRITE High from CLK High (S4) Delay Time ³⁾	_	200	_	130	
TDQ1	HRQ Valid from CLK High Delay Time 4		160		120	
TDQ2	Time valid from CER riight belay Time		250		120	
TEPS	EOP Low from CLK Low Setup Time	60		40		
TEPW	EOP Pulse Width	300	-	220		
TFAAB	ADR Float to Active Delay from CLK High		250		170	
TFAC	READ or WRITE Active from CLK High		200		150	
TFADB	DB Float to Active Delay from CLK High		300		200	

Notes see next page.

Symbol	Parameter		Lim	nit Values		Unit	
		8237A		823	8237A-5		
		Min.	Max.	Min.	Max.		
THS	HLDA Valid to CLK High Setup Time	100		75			
TIDH	Input Data from MEMR High Hold Time	0	1	0			
TIDS	Input Data to MEMR High Setup Time	250	7	170			
TODH	Output Data from MEMW High Hold Time	20		10		ns	
TODV	Output Data Valid to MEMW High 5)	200]_	125]	115	
TQS	DREQ to CLK Low (S1, S4) Setup Time 1)	0		0			
TRH	CLK to READY Low Hold Time	20		20			
TRS	READY to CLK Low Setup Time	100	1	60			
TSTL	ADSTB High from CLK High Delay Time		200		130		
TSTT	ADSTB Low from CLK High Delay Time	_	140		90		
ТОН	DREQ from DACK Valid Hold Time	0		0			
TRQHA	HRQ to HLDA Delay Time	1	1	1	7	clk	

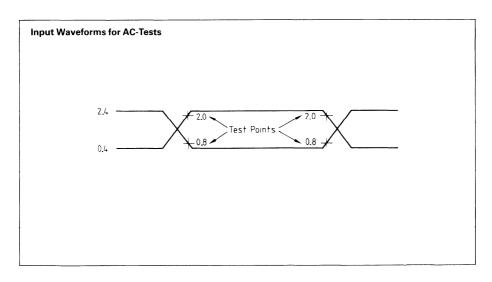
- 1) DREQ and DACK signals may be active high or low. Timing diagrams assume the active high mode.
- 2) EOP is an open collector output. This parameter assumes the presence of a 2.2 k Ω pullup to VCC.
- 3) The net IOW or MEMW pulse width for normal write will be TCY -100 ns and for extended write will be 2TCY -100 ns. The net IOR or MEMR pulse width for normal read will be 2TCY -50 ns and for compressed read will be TCY -50 ns.
- 4) TDQ is specified for two different output high levels. TDQ1 is measured at 2.0 V. TDQ2 is measured a 3.3 V. The value for TDQ2 assumes an external 3.3 k Ω pull-up resistor connected from HRQ to VCC.
- 5) If N wait states are added during the write-to-memory half of a memory-to-memory transfer, this parameter will increase by N (TCY).

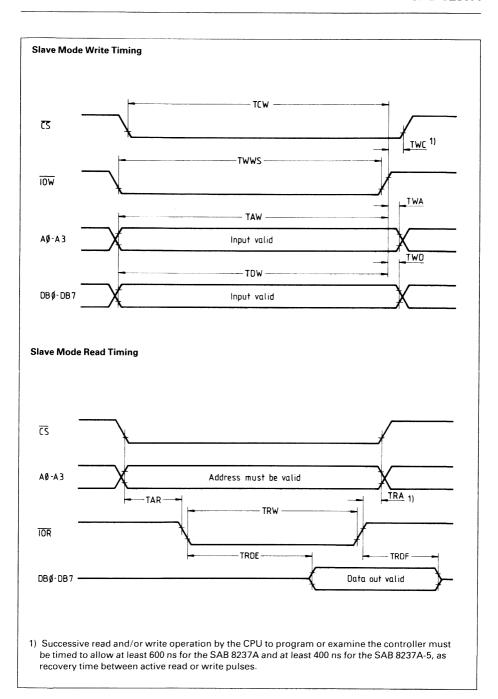
SAB 8237A

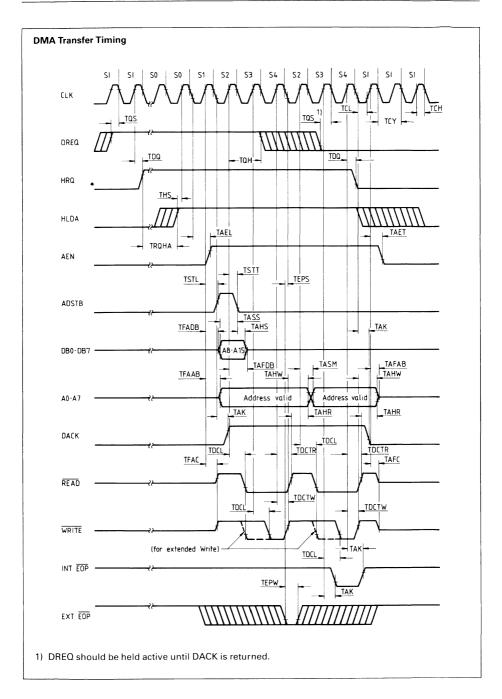
Peripheral (Slave) Mode

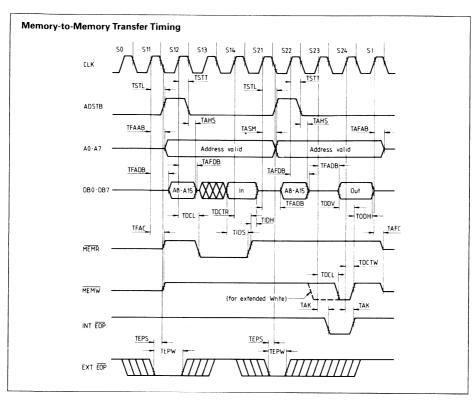
Symbol	Parameter		Lim	it Values		Unit
		82	237A	8237A-5		
		Min.	Max.	Min.	Max.	
TAR	ADR Valid or CS Low to READ Low	50		50		
TAW	ADR Valid to WRITE High Setup Time	200		130		
TCW	CS Low to WRITE High Setup Time	200	_	130	_	
TDW	Data Valid to WRITE High Setup Time	200		130		
TRA	ADR or CS Hold from READ High	0		0		
TRDE	Data Access from READ Low 1)	-	200	-	140	
TRDF	DB Float Delay from READ High	20	100	0	70	ns
TRSTD	Power Supply High to RESET Low Setup Time	500		500		
TRSTS	RESET to First IOWR	2 TCY		2 TCY		
TRSTW	RESET Pulse Width	300		300		
TRW	READ Width	300]_	200	_	
TWA	ADR from WRITE High Hold Time	20		20		
TWC	CS High from WRITE High Hold Time	20		20		
TWD	Data from WRITE High Hold Time	30		30		
TWWS	WRITE Width	200		160		

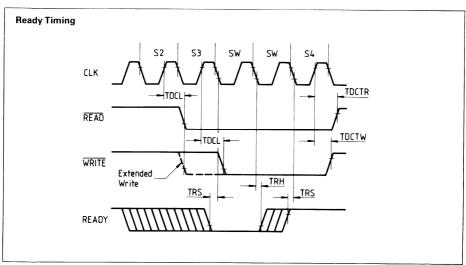
1) Output loading is 1 TTL gate plus 150 pF capacitance, unless otherwise noted.

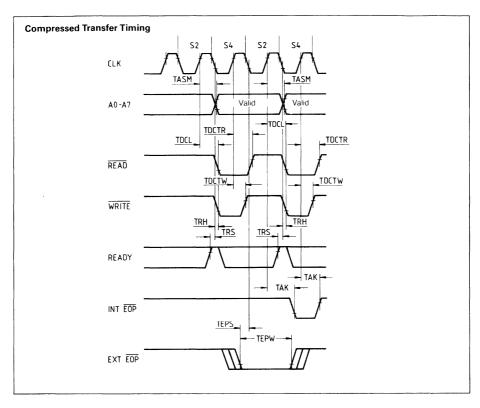


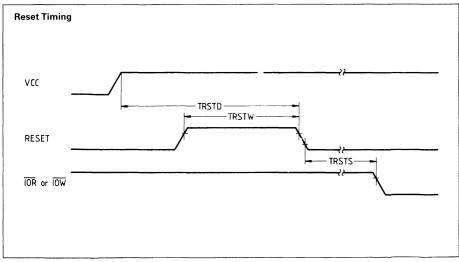




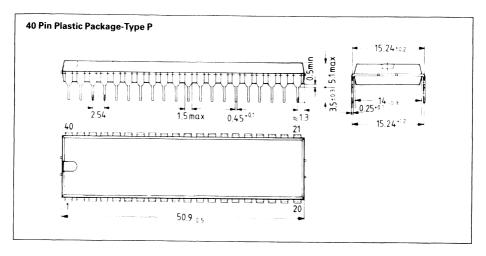








Package Outline



SAB 8237A

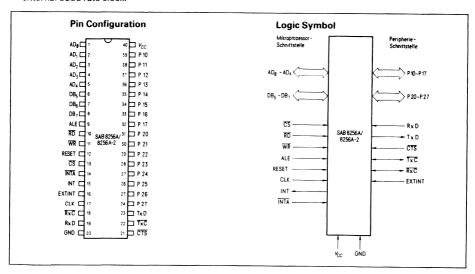
Ordering Information

Description	Ordering code
Programmable DMA Controller 3 MHz (Plastic)	Q 67120-Y49
Programmable DMA Controller 5 MHz (Plastic)	Q 67120-Y72
	Programmable DMA Controller 3 MHz (Plastic)



SAB 8256A, SAB 8256A-2 Programmable Multifunction UART (MUART)

- SAB 8256A compatible with processors up to 3 MHz system clock (e. g. SAB 8085A, SAB 8048, SAB 8051).
 - SAB 8256A-2 compatible with processors up to 8 MHz system clock (e.g. SAB 8085A-2, SAB 8086 minimum mode, SAB 80186).
- Full-Duplex asynchronous serial interface with programmable 5–8 data bits, 0.75–2 stop bits, parity generation and checking.
- Internal baud rate generator programmable for 50-19200 Baud; 0-1 Megabaud possible with external baud rate clock.
- Interrupt Controller with 8 priority levels; each level independently maskable, programmable for normal and fully nested operation with SAB 8085 and SAB 8086 processor families.
- Five programmable 8-bit counter/timers, internal or external clock, four are cascadable to two 16-bit counter/timers.
- Two 8-bit I/O ports, bit programmable for input/output, hand-shake mode supported.



SAB 8256A integrates four of the most used peripheral functions in a microcomputer system into a 40 pin package: serial interface, parallel interface, timer/counter and interrupt controller. It is primarily suited for system like SAB 8048, SAB 8085, SAB 8086, SAB 8088, SAB 80186 and

SAB 80188 which have a multiplexed bus. With some additional circuitry, it can also be used with other processors. All the functions of SAB 8256A are programmable by software, leading to a great flexibility in system design.

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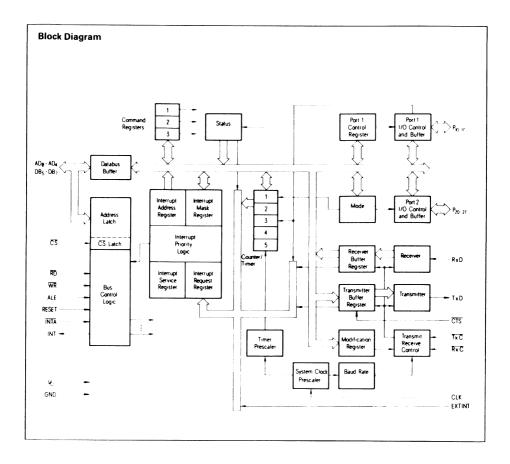
Pin Description and Functions

Symbol	Pin No.	Input (I) Output (O)	Function
ADØ-AD4, DB5-DB7	1-8	I/O	Interface to Multiplexed Bus Bidirectional lines to 8 data bits and 5 least significant address bits which are latched internally on the falling edge of ALE.
ALE	9	I	Adress Latch Enable The five least significant address bits and $\overline{\text{CS}}$ are latched on the falling edge of ALE into an internal register.
RD	10	I	Read Control The microprocessor reads data from the chip when this signal is low.
WR	11	1	Write Control The microprocessor writes data into the chip with a low on this pin.
RESET	12	1	Reset A high on this pin forces the chip to its initial state. The chip remains in this state till control information is written into the chip.
CS	13	ı	Chip Select A low on this pin during ALE enables the bus interface of the chip. Neither read nor write operations are possible without this enable. The signal has no effect on the internal operation of the chip.
INTA	14	I	Interrupt Acknowledge The microprocessor informs the chip a low on this pin that an interrupt request is being serviced, if this functions has been enabled.
INT	15	0	Interrupt Request The chip demands interrupt service from the microprocessor with a high on this output.
EXTINT	16	I	External Interrupt An external source can request interrupt service through this input. The source can be either a peripheral or another SAB 8256A with its INT pin as the signal source. The input is level sensitive (high). The request must be held high until the processor acknowledges it.
CLK	17	I	System Clock Clock on this input is the reference clock for various function like timers, baud rate generator etc.

Symbol	Pin No.	Input (I) Output (O)	Function
R×C	18	I/O	Receiver Clock If this pin is programmed as an output, it provides a low-to-high transition at the sampling point of each received data bit (excluding the framing bits). When programmed as an input, an externally generated receiver clock must be connected to this pin. At DC, its frequency can range up to 1.024 MHz matching the receiver baud rate. The internal baud rate generator is disabled if this pin is used as input.
R×D	19	l	Receiver Data Input for serial data, which is converted to parallel format while discarding the framing bits and then is made available for the processor.
CTS	21		Clear to Send This input enables the serial transmitter. If 1, 1.5 or 2 stop bits are selected, CTS is level sensitive. As long as CTS is low, any character loaded into the transmitter buffer register will be transmitted serially. For continuous transmission, this input must be tied to low. A single negative going pulse causes the transmission of a single character previously loaded into the transmister buffer register. If the transmitter buffer is empty, this pulse will be ignored. If this pulse occurs during the transmission of a character upto the time where 0.5 of the first (or the only) stop bit is sent out, it will be ignored. If it occurs afterwards, but before the end of the stop bits the next character will be transmitted immediatly following the current one. If CTS is still high when the transmitter register is sending the last stop bit, the transmitter will enter its idle state until the next high-to-low transition on CTS occurs. If 0.75 stop bits is chosen, CTS input is edge sensitive. A negative edge on CTS results in the immediate transmission of the next character. The length of the stop bits is determined by the time interval between the beginning of the first stop bit and the next negative edge on CTS. A high-to-low transition has no effect if the transmitter buffer is empty or if the time interval between the beginning of the stop bit and next negative edge is less than 0.75 bit. A high or a low level or a low-to-high transition has no effect on the transmitter for the 0.75 stop bit mode.
T×c	22	1/0	Transmitter Clock The function of this pin can be programmed in 3 configurations. As an output it delivers the transmitter clock corresponding to the baud rate. If programmed as an input, an external clock of 32 or 64 times the baud rate that is common to transmitter and receiver, or a $1\times$ clock matching the baud rate which is used for the transmitter only, can be tied to this pin. The maximum frequency is 1.024 MHz. Thus, baud rates ranging from 0 to 16 Kbaud $(64\times)$ or from 0 to 32 Kbaud $(32\times)$ or from 0 to 1.024 Mbaud $(1\times)$ are possible. The internal baud rate generator is disabled if $\overline{1\times}C$ is selected as input.

SAB 8256A

Symbol	Pin No.	Input (I) Output (O)	Function
T×D	23	0	Transmitter Data Serial data output. The parallel data received from the processor and the framing bits added by the SAB 8256A are sent out serially over this output when the transmitter is enabled by the CTS signal.
P27-P20	24-31	1/0	Parallel I/O Port 2 The eight general purpose I/O pins of parallel port 2 can be configured in sets of four pins (nibbles) as inputs or outputs or 8 bit I/O with handshake (control-signals at port 1). In the nibble mode the output signals are latched whereas the input signals are not. In the handshake mode both inputs and outputs are latched.
P17-P10	32-39	1/0	Parallel I/O Port 1 Each one of these 8 pins can be programmed as input or output. Alternatively these pins can serve as control pins which extends considerably the functional spectrum of the chip. The pins are assigned special functions implicitly by programming. All outputs are latched whereas inputs are not.
V _{cc}	40	_	Power Supply (+5V)
GND	20	_	Ground (0 V)



Functional Description

Bus Interface

The bus interface unit, consisting of bus drivers, address latches and bus control logic, interfaces the SAB 8256A to the data, address and control busses of a microcomputer system. The chip is selected by the $\overline{\text{CS}}$ signal, which is latched into the chip along with address lines AD0 – AD4 by the ALE signal. $\overline{\text{WR}}$ and $\overline{\text{RD}}$ signals are used to write data into and read data from SAB 8256A.

Signals INT und INTA are used to handle interrupt protocol with the processor.

RESET signal resets the chip to its initial state.

Counter/Timer

Five programmable counter/timers can be used in several modes. Each can be used as an 8-bit timer while two can alternatively serve as counters. Counter/timer 2 and timer 4 as well as 3 counter/timers. All counter/timers function as binary down-counters with a programmable initial value and generate an interrupt request on their 1 to 0 transition. An internal register is provided for the initial count of timer 5 and with an external trigger pulse it is possible to reload the initial value into timer 5 (also for cascaded counter/timer 3 and timer 5).

A common clock source with a frequency of either 1 KHz or 16 KHz is available for the timers. In addition, for counters, 2, 3 and the cascaded counters, an external clock source can be provided through two pins of part 1.

Asynchronous Serial Interface

For double buffered full-duplex operations both transmitter and receiver have two registers. The received data (5 to 8 data bits, programmable) is assembled to parallel format in the receiver register, the framing bits (Start, Stop, and Parity) are stripped off and stored into the receiver buffer register. The data to be transmitted is first loaded into the transmitter buffer register and then sent out through the transmitter register.

Controlling the CTS signal, single characters on character strings can be transmitted. Baud rate clock (50 to 19,200 Baud) is generated on the chip which is common to both the receiver and the transmitter. It is also possible to provide an external baud rate clock (common or separate for receiver and transmitter) to provide baud rates from 0 to 1.024 Mbaud.

Parallel Interface

The parallel interface consists of two 8-bit ports programmable as inputs or outputs. Each pin of port 1 can be programmed separately as an input or an output. They can also be used as control pins. Ports 2 can be programmed as input our output in two 4-bit groups. Port 2 can also be used as an 8-bit input or output port with handshake signals.

Assignment of Control Signals to Port 1

Pins Port 1	P17	P16	P15	P14	P13	P12	P11	P10
Control Function	External interrupt input	Break-In detect input	Trigger input for timer 5 (cascaded counter/ timer 3+5)	Output of the clock of the internal baudrate- generator	Clock input for counter 3	Clock input for counter 2	Handshak Signals fo	

Interrupt Controller

The interrupt controller manages 12 interrupt sources (10 internal and 2 external) on 8 priority levels. Normal (every interrupt request immediately recognized) and "fully nested" (recognition based on priority) modes are supported.

The interrupt controller supports various methods of connecting SAB 8256A to the processor. Firstly, the true interrupt mode (using INT and INTA signals for interrupt protocol), secondly, a combination of polling and interrupt (using INT and interrupt address registers). The interrupt protocols of SAB 8048, SAB 8085A, SAB 8086, SAB 8088, SAB 80186 and SAB 80188 are directly supported.

Programming the SAB 8256A

The functional characteristics of SAB 8256A can be programmed by writing appropriate control information into it. It is specially designed for ease of programming. It is hence possible to alter individual bits in certain registers like e.g. the Interrupt Mask Register and Command Register 3. All functions of SAB 8256A can be easily used because each unit (e.g. counter/timer, serial interface) has specially assigned registers which can be directly read or written.

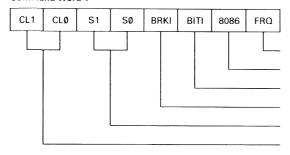
Registe	r Sel	lect										
	FRO		BØ		0		P2CØ		P10		Γĝ	
	9808	Command Register 1	18	Command Register 2	TBRK		P2C1		P11	ter	17	Interrupt Mask Register
gisters	BITI		B2		SBRK	ဗု	P2C2		P12		77	
	BRKI		B3		0	Register	CT2	Mode Register	P13	ol Regis	ខ	
Read Registers	ØS	mmand	Ø	nmand	Ä	Command Register 3	CT3		P14	Port 1 Control Register	4	
	S1	Ŝ	٦	Ö	IAE	Ö	T5C		P15		L5	
	CLØ		9		R×E		T24		P16		P. P.	
	CL1		PEN		0		T35		P17		77	
ADØ AD1	0	-	-		0	-	-	•	6	•	-	•
ress AD1 AD2	0		9		-		-		0		0	
Address AD2 AD3 AD3 AD3	0		0		0		0		-		_	
AD3 AD4	0		0		0		0		0		0	
SAB 8085 Mode: AD3 SAB 8086 Mode: AD4	FRO		BØ		SRES		P2CØ		P10		ΓØ	
AB 8085 AB 8086	9808		18		TBRK		P2C1		P11		11	i i
	BITI	_	B2	2	SBRK	e .	P2C2		P12	p	77	Word
egisters	BRKI	d Word	B3	d Word	END	d Word	CT2	Word	P13	1 Control Word	L3	Enable
Write Registers	SØ	Command Word 1	80	Command Word 2	NE NE	Command Word 3	СТЗ	Mode Word	P14	Port 1 Con	L4	Interrupt-Level Enable Word
	S1	٥	5	O	IAE	O	TEC		P15	Po	. L5	Interru
	CLØ		д		R × E		T24		P16		PT PT	
538	CL1		PEN		SET		T35		P17		[17	

		8		ΘΩ		©		ρQ		<u>0</u>		Ø	
gisters	10		10		10		D1		10		10		
	D2	Interrupt Address Register	02		05		D2	ort 2	D2	imer 1	D2	er 2	
	D3		D3		23	Port 1	D3		D3		D3	/Count	
Read Registers		D4	upt Add	40	Receiver Buffer	42	Read Port 1	D4	Read Port 2	40	Read Timer 1	D4	Read Timer/Counter 2
	DS	Interr	50		50		D5		DS		DS	Rea	
		90		90		90		90		90		D6	
		D7		10		10		D7		10		D7	
	ADØ AD1	6		_		6		_		6		_	
ess	AD1 AD2	-		-		0		0		-		-	
Address	AD2 AD1 AD0 AD3 AD2 AD1	-		-		0		0		0		0	
	AD3 AD4	0		0		-		-		-		-	
	SAB 8085 Mode: AD3 SAB 8086 Mode: AD4	ΓØ	vel Disable Word	ρQ		Õ		ρØ		ΘĞ		ρQ	
	AB 8085 AB 8086	۲1		5		10		10		10		D1	
	SS	17		D2	<u>_</u>	D2		D2		D2		D2	11.2
gisters		F.3		23	Transmitter Buffer	63	Port 1	D3	Write Port 2	D3	imer 1	D3	/Counte
Write Registers		L4		D4	ansmitt	7	Write Port 1	D4	Write	70	Write Timer 1	D4	Write Timer/Counter 2
		L5	Interru	Interrup D5	Ë	90		D5		D5		D5	
		97		90		90		De		90		9Q	
		7.7		D7		07		D7		70		D7	
					-		•						

		80		00		ØΩ		Ⅱ	
		D1	Read Timer/Counter 3	10		10		OE	
		D2		D2		D2		PE	
gisters		D3		D3	imer 4	D3	imer 5	BD	Status Register
Read Registers		D4	d Timer	D4	Read Timer 4	D4	Read Timer 5	TRE	
_		D2	Rea	DS		DS		TBE	
		9G		90		90		RBF	
		D7		70		D7		TNI	
	ADØ AD1	6		_	İ	6	ŀ	_	
SS	VD1 /	0		0		-		-	
Address	(D2 /	-		-		-		-	
	D3 A	-		_		_		-	
	de: A	DØ		ρĝ		ρĝ		ာ့	
	85 Mc 86 Mc			٥		_		DSC	
	SAB 8085 Mode: AD3 AD2 AD1 AD0 SAB 8086 Mode: AD4 AD3 AD2 AD1	D1		D1		D1	Write Timer 5	TME	
	o o	D2	er 3	D2		D2		RSØ	р
gisters		D3	/Counte	D3	imer 4	D3		RS1	ion Wor
Write Registers		D4	Write Timer/Counter 3	D4	Write Timer 4	D4		RS2	Modification Word
		D5 Write		DS		DS		RS3	Š
		9Q		9Q		9Q		RS4	
		D7		D7		D7		0	

Programming

Command Word 1



Timer Input Frequency

Processor Type Select

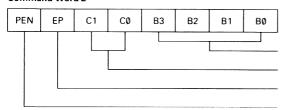
Source for Interrupt Level 1

Break-In Detect Enable

Stop Bit Length

Character Length

Command Word 2



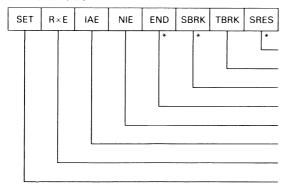
Baud Rate Select

System Clock Prescaler

Odd/Even Parity

Parity Enable

Command Word 3



Software Reset

Transmit Continous BREAK

Transmit Single Character BREAK

End of Interrupt

Nested Interrupt Enable

Interrupt Acknowledge Enable

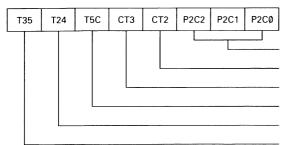
Receive Enable

Bit Set/Reset in Register 3

^{*)} These bits can only be set, they are reset at the end of the operation.

SAB 8256A

Mode Word



Port 2 Control

Timer/Counter 2 Mode

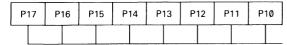
Timer/Counter 3 Mode

Timer 5 Mode

Cascade Counter/Timer 2 and Timer 4

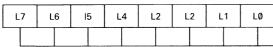
Cascade Counter/Timer 3 and Timer 5

Port 1 Control World



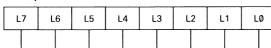
Input/Output Mode of Ports 1 Pins

Interrupt-Level Enable Word



Enable Interrupt Levels

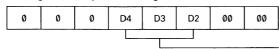
Interrupt-Level Disable Word



Disable Interrupt Levels

Determination of Interrupt Level

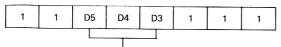
Reading the Interrupt Address Register



Interrupt Level

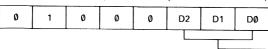
Response to INTA

SAB 8085-Mode (RST-instruction in response to INTA)



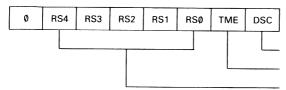
Interrupt Level

SAB 8086-Mode (Interrupt Vector in response to second INTA)



Interrupt Level

Modification Word

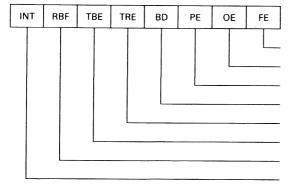


Disable Start Bit Check

Transmission Mode Enable

Receiver Sampling Point

Status Register



Framing Error/Transmission Mode Indication

Overrun Error

Parity Error

Break Detect or Break-in Detect

Transmitter Register Empty

Transmitter Buffer Empty

Receiver Buffer Full

Interrupt Pending

SAB 8256A

Absolute Maximum Ratings 1)

Ambient Temperature Under Bias $0 \text{ to } 70^{\circ}\text{C}$ Storage Temperature $-65 \text{ to } +150^{\circ}\text{C}$

Voltage on Any Pin With Respect to Ground -0.5 to +7 V

Power Dissipation 1W

D.C. Characteristics

 $T_A = 0$ to 70°C, $V_{CC} = 5 \text{ V} \pm 5\%$, $V_{SS} = 0 \text{ V}$ (when not otherwise specified)

0 1 1	B	Limi	t Values	1.1	T . O . III.	
Symbol	Parameter	Min. Max.		Unit	Test Condition	
V _{IL}	Input Low Voltage	-0.5	0.8		_	
V _{IH}	Input High Voltage	2.0	V _{CC} +0.5	v		
V _{OL}	Output Low Voltage	-	0.45	*	$I_{OL} = 2.5 \text{mA}$	
V _{OH}	Output High Voltage	2.4	-		$I_{\rm OH} = -400 \mu {\rm A}$	
I_{IL}	Input Leakage		±10	uА	$V_{\rm IN}=0{ m V}$ to $V_{\rm CC}$	
I _{LO}	Output Leakage Current	_	190		$V_{\text{OUT}} = 0 \text{ V to } V_{\text{CC}}$	
I _{CC}	V _{CC} Supply Current				_	

Capacitance 2)

Symbol	Parameter	Limit Value (Max.)	Unit	Test Condition		
C _{IN}	Input Capacitance	10	pF	f _C = 1 MHz Unmeasured pins		
C _{I/O}	I/O Capacitance 20]"	returned to GND		

¹⁾ Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

²⁾ This parameter is periodically sampled and not 100% tested.

A.C. Characteristics

 $T_{\rm A}=0$ to 70°C; $V_{\rm CC}=+5\,{
m V}\pm5\%$; $V_{\rm SS}=0\,{
m V}$

Test Conditions

Capacitive load $C_{\rm L} = 150~{\rm pF}$

The timings are with respect to the following levels:

H-level: 2.0 V L-level: 0.8 V

Rise and fall times: 20 ns

The timings are valid for an internal clock of 1.024 MHz.

			Limit				
Symbol	Parameter	SAB 825	56A	SAB 8256A-2		Unit	Test Condition
		Min.	Max.	Min.	Max.		
t AC	STB ↓ to ÎBF ↓	_	300	_	300	ns	
t ACK	ACK Pulse Width	t ADP	-	t ADP	_	_	
t AD	Address Stable to Data Valid		400		230		
t ADP	ACK ↓ to OBF ↑		300	_	300	ns	
t AED	OBF ↓ to ACK ↓	0	_	0	-		
t Al	ACK ↑ to INT ↑	_	1.5 t CY	-	1.5 t CY	-	
t AL	Address Stable to ALE ↓	50		30			
t CC	RD and WR Pulse widths	300		200]	ns	
t CL	RD ↑ or WR ↑ to Next ALE ↑	50		25			
t CPI	Counter input Cycle Time (P12, P13,)	2.2]_	2.2		μs	
t CSL	CS Stable to ALE ↓	60		10		ns	
t CTS	CTS Pulse Width for Single Character Transmission	1)		1)		_	
t CY	System Clock Period	300		195	1	ns	1
t DEI	STB ↑ to INT ↑		1.5 t CY		1.5 t CY	_	
t DEX	EXTINT ↑ to INT ↑		200	_	200		1
t DH	STB ↑ to P2 Data Stable	10	-	10	-	ns	
t DPI	Interrupt Request on P17 to INT↑	_	1.5 t CY	_	1.5 t CY	_	1
t DSI	P2 Data Stable before STB ↓	10	-	10	_		
t DTX	T×C ↓ to T×D Data Valid	_	300	_	300		
t DW	Data Valid before WR↑	250		150]	
t HEA	EXTINT ↓ after INTA ↑ or RD ↑	30]_	30	}_		
t HIA	INT ↓ after INTA ↑ or RD ↑	_	300	_	300	ns	
t LA	CS and Address valid after ALE ↓	50		20			
t LC	ALE ↓ to RD ↓ or WR ↓	60]-	20	1-		
t LL	ALE Pulse width	100		50	1		

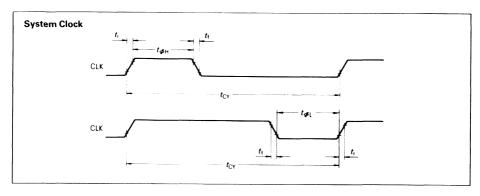
Notes see next page.

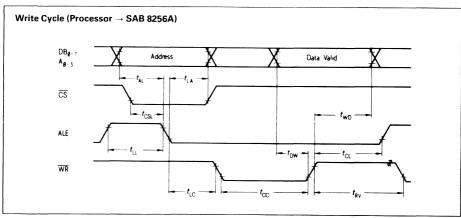
			Lim				
Symbol	Parameter	SAB 8256A		SAB 82	256A-2	Unit	Test Condition
		Min.	Max.	Min.	Max.		Johnson
t PI	Pulse Width of Interrupt Request on P17	1.1		1.1		แร	
t PP	Counter 5 Load (P15↓) before Next Clock Pulse on P13 ↑	1	_			,113	
t PR	P1, P2 Data Stable before RD ↓	300		300			
t RD	Data Valid after RD ↓	_	200	_	150		_
t RDE	RD ↓ to Data Drivers Active	10	100	10	50		
t RDF	Data Bus Float After RD ↑	10	100		30		
t RES	RESET Pulse Width	300	_	300	-		
t RI	RD ↑ to IBF ↑	-	300	-	300		
t RP	P1, P2 Data Hold after RD↑	50	_	50	1-	ns	
t RRD	Data Bit Start to R×C ↓		2)		2)	7	3)
t RV	RD ↑ or WR ↑ to Next RD ↓ or WR ↓	300		150			CS =Low
t SCY	Serial Clock Period (32×, 64×)	975		975			
t SPD	Serial Clock High (32×, 64×)	250		350			
t SPW	Serial Clock Low (32×, 64×)	350		350			
t STB	Strobe Pulse Width	t AC	7	t AC		_	
t TCY	Serial Clock Period (1×)	975		975		ns	٦
t TPD	Serial Clock High (1×)	350		350			
t TIH	Load Pulse for Counter 5 (P15)-High	1.1		1.1			
t TIL	Load Pulse for Counter 5 (P15)-Low] '. '		'.'			
t TPI	Counter Input ↑ (P12, P13) to INT ↑ at Terminal Count	-	2.5	-	2.5		
t TPW	Serial Clock Low (1)	350		350		ns	
t TRV	Time between 2 readcycles onto the same counter/timer	1.1	_	1.1]-	μs	
t WD	Data Hold after WR ↑	40		30			
t WP	P1, P2 Data Valid after WR↑	-	300	_	300	ns	1
t WPH	Count Clock (P12, P13) High			1.			7
t WPL	Count Clock (P12, P13) Low	1.1	-	1.1	-	μs	
t WPO	OBF ↑ after WR ↓		300		300		7
t f	Clock Fall Time	1-	30		30		
t ΦH	Clock High	105		C.E.		ns	
t ΦL	Clock Low	105	-	65	-		
tr	Clock Rise Time	1-	30	_	30		

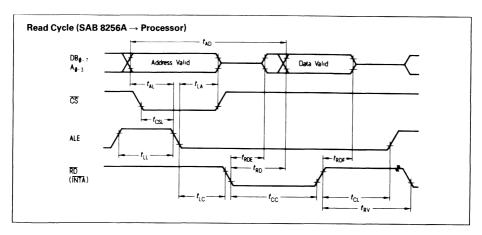
^{1) 1/32} bit length with transmitter clock with a baud rate factor of 32 or 64 100 ns when baud rate factor = 1

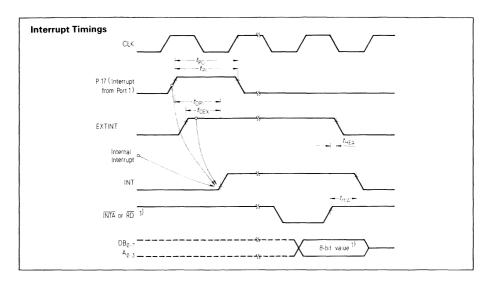
 ³⁰⁰ ns + (1/32 bit length)
 Sampling time at bit center

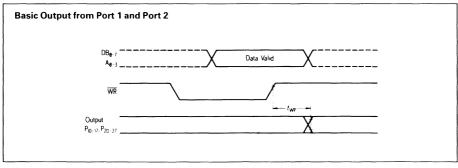
Waveforms

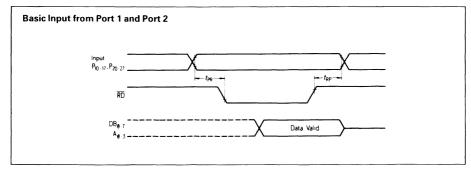






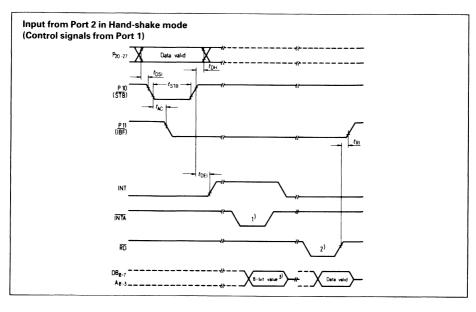


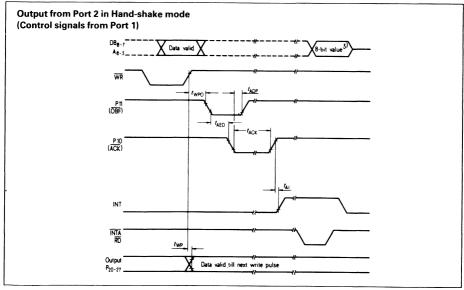




If INTA is enabled, RSTn instruction is output on INTA (SAB 8085 mode) or interrupt vector is output on second INTA (SAB 8086 mode) other-

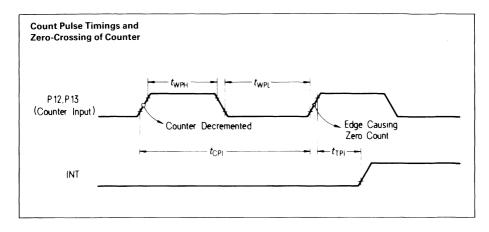
wise, interrupt address is output on a read address register operation.

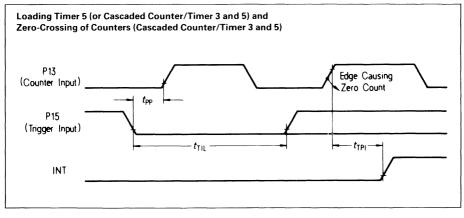


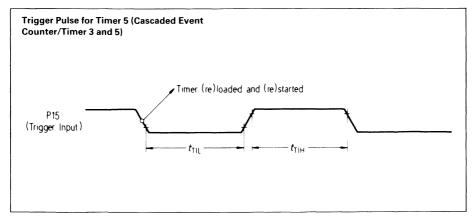


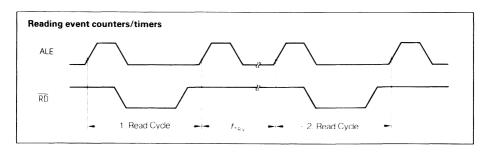
- Instead of INTA, RD can serve as interrupt acknowledge (reading the interrupt address register).
- 2) Read from channel 2.

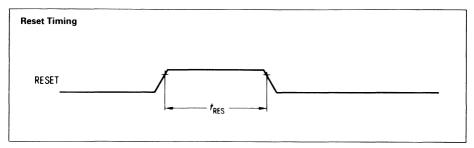
If INTA is enabled, RSTn instruction is output on INTA (SAB 8085 mode) or interrupt vector is output on second INTA (8086 mode) otherwise, interrupt address is output on a read address register operation.

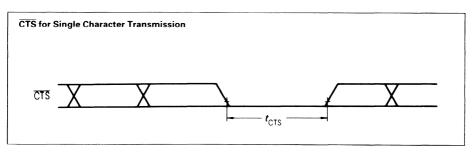


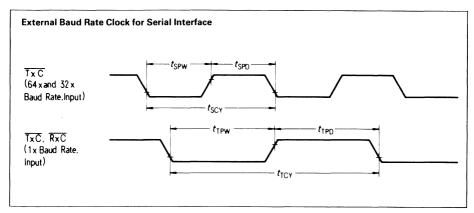


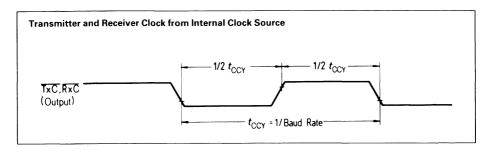


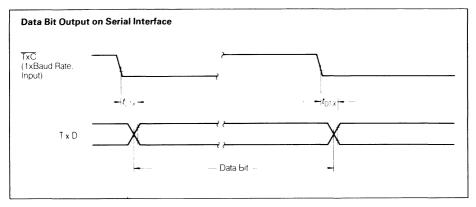


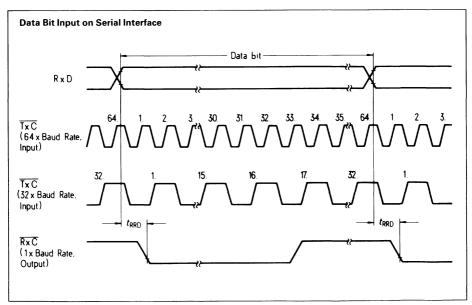


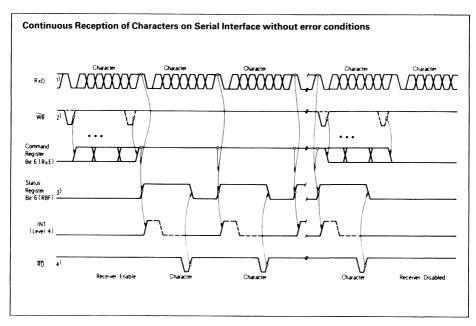






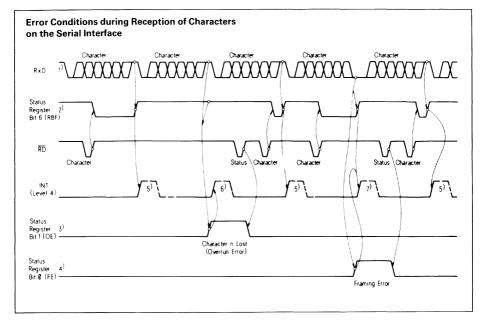






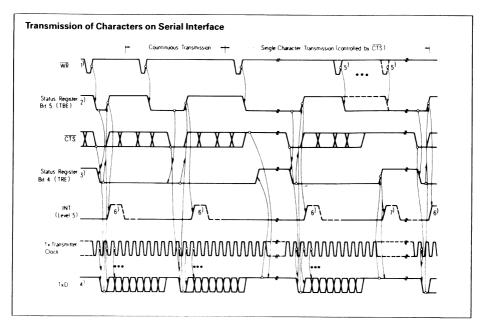
- 1) Character format for this example: 6 Data bits with Parity bit and one Stop bit.
- 2) Set or Reset bit 6 of Command Register 3 (Enable Receiver)
- 3) Receiver Buffer Loaded
- 4) Read Receiver Buffer Register
- 5) Receiver is active even though no data is sent or Status bit set.

No Status bits are altered when RD is active.



- 1) Character format for this example: 6 Data bits without Parity and one Stop bit
- 2) Receiver Buffer Register Loaded
- 3) Overrun error
- 4) Framing error
- 5) Interrupt from receiver buffer register loading
- 6) Interrupt from Overrun error
- 7) Interrupt from framing error and loading receiver buffer register

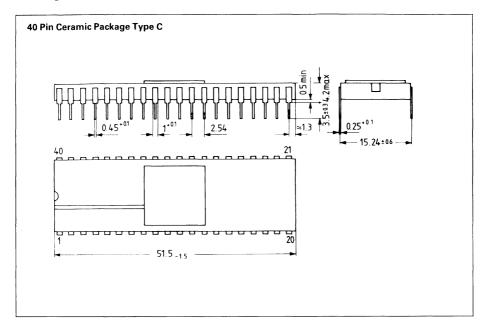
No Status bits are altered when \overline{RD} is active.

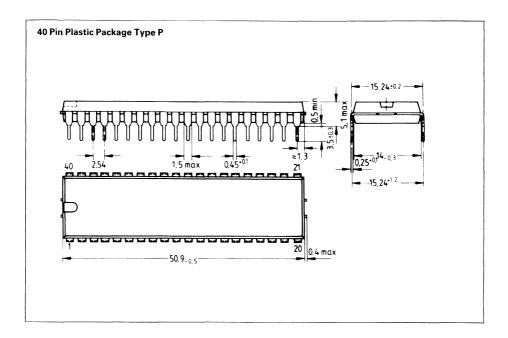


- 1) Load Transmitter buffer register
- 2) Transmitter buffer register is empty
- 3) Transmitter register is empty
- 4) Character format for this example: 7 Data bits with Parity bit and 2 Stop bits
- 5) Loading of transmitter buffer register must be completed before $\overline{\text{CTS}}$ goes low
- 6) Interrupt due to transmitter buffer register empty
- 7) Interrupt due to transmitter register empty

No Status bits are altered when RD is active.

Package Outline





Ordering Information

Туре	Description	Ordering code
	Programmable Multifunction Chip MUART	
SAB 8256A-C	3 MHz system clock (ceramic)	Q 67120-Y55
SAB 8256A-P	3 MHz system clock (plastic)	Q 67120-Y43
SAB 8256A-2-C	5 MHz system clock (ceramic)	Q 67120-Y58
SAB 8256A-2-P 5 MHz system clock (plastic)		Q 67120-Y59



SAB 8259A, SAB 8259A-2 Programmable Interrupt Controller

- Compatible with SAB 8086/88, SAB 80186/188 and SAB 80286 processor families
- · Eight-level priority controller
- Expandable to 64 levels

- Programmable interrupt modes
- Individual request mask capability
- Single +5 V supply (no clocks)
- 28-pin dual-in-line package

in Configuration		Pin Names	
	28 7 VCC	D7-D0	Data Bus (Bidirectional)
₩R ☐ 2	27 A 0	RD	Read Input
RD [3	26 TINTA	WR	Write Input
07 🗆 4	25 IR7	A0	Command Select Address
D6 5	24 IR6	 CS	Chip Select
D5	23	CAS2-CAS0	Cascade Lines
D3 8 8259A	21	SP/EN	Slave Programm/Enable Buffer
D2 🗖 9	20 IR2	INT	Interrupt Output
D1	19 IR1	ĪNTA	Interrupt Acknowledge Input
D0	18 IR 0 17 INT	IR0-IR7	Interrupt Request Inputs
AS1 13	16 SP/EN		
GND 14	15 CAS2		

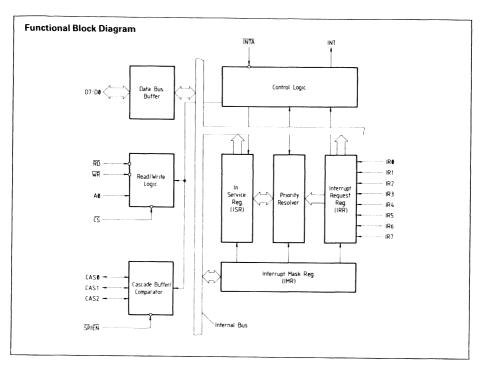
The SAB 8259A programmable interrupt controller handles up to eight vectored priority interrupts for the CPU. It is cascadable for up to 64 vectored priority interrupts without requiring additional circuitry. The SAB 8259A is fabricated in +5V advanced N-channel, silicon gate Siemens MYMOS technology and packaged in a 28-pin DIP. The circuitry is static, requiring no clock input.

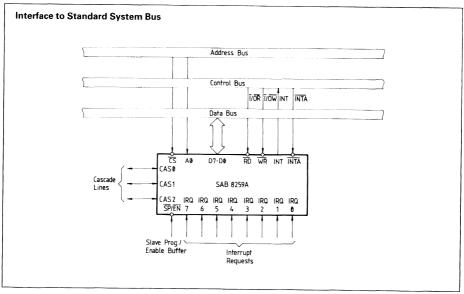
The SAB 8259A is designed to minimize the software and real-time overhead in handling multi-level priority interrupts. It has several modes, permitting optimization for a variety of system requirements.

Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
CS	1	l	CHIP SELECT A low on this pin enables $\overline{\text{RD}}$ and $\overline{\text{WR}}$ communication between the CPU and the SAB 8259A. $\overline{\text{INTA}}$ functions are independent of $\overline{\text{CS}}$.
WR	2	1	WRITE A low on this pin when $\overline{\text{CS}}$ is low, enables the SAB 8259A to accept command words from the CPU.
RD	3	1	READ A low on this pin when $\overline{\text{CS}}$ is low, enables the SAB 8259A to release status onto the data bus for the CPU.
D7-D0	4-11	I/O	BIDIRECTIONAL DATA BUS Control, status and interrupt vector information is transferred via this bus.
CAS0-CAS1	12, 13, 15	1/0	CASCADE LINES The CAS lines form a private SAB 8259A bus to control a multiple SAB 8259A structure. These pins are outputs for a master SAB 8259A and inputs for a slave SAB 8259A.
SP/EN	16	1/0	SLAVE PROGRAM/ENABLE BUFFER This is a dual function pin. When in buffered mode it can be used as an output to control buffer transceivers (EN). When not in buffered mode it is used as an input to designate a master (SP = 1) or slave (SP = 0).
INT	17	0	INTERRUPT ¹⁾ This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin.
IR0-IR7	18-25	1	INTERRUPT REQUESTS Asynchronous inputs. An interrupt request can be generated by raising an IR input (low to high) and holding it high until it is acknowledged (edge triggered mode), or just by a high level on an IR input (level triggered mode).
INTA	26	I	INTERRUPT ACKNOWLEDGE This pin is used to enable SAB 8259A interrupt-vector data onto the data bus. This is done by a sequence of interrupt acknowledge pulses issued by the CPU.
A0	27	I	A0 ADDRESS LINE This pin acts in conjunction with the $\overline{\text{CS}}$, $\overline{\text{WR}}$ and $\overline{\text{RD}}$ pins. It is used by the SAB 8259A to destinguish between various command words the CPU writes and status the CPU wishes to read. It is typically connected to the CPU A0 address line (A1 for SAB 8086/80186/80286).
VCC	28	1	POWER SUPPLY (+5V)
GND	14	1	GROUND (0 V)

 $^{^{1)}}$ An active low signal on $\overline{\rm WR}$ during an INT high signal may force INT to low.





Functional Description

General

The SAB 8259A is a device specifically designed for use in real-time, interrupt-driven microcomputer systems. It manages eight levels or requests and has built-in features for expandability to other SAB 8259A's (up to 64 levels). It is programmed by the system's software as an I/O peripheral. A selection of priority modes is available to the programmer so that the manner in which the requests are processed by the SAB 8259A can be configured to match his system requirements. The priority modes can be changed or reconfigured dynamically at any time during the main program. This means that the complete interrupt structure can be defined as required, based on the total system environment.

Interrupt Request Register (IRR) and In-Service Register (ISR)

The interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In-Service Register (ISR). The IRR is used to store all the interrupt levels which are requesting service, and the ISR is used to store all the interrupt levels which are being serviced.

Priority Resolver

This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during an INTA pulse.

Interrupt Mask Register (IMR)

The IMR stores the bits which mask the interrupt lines to be masked. The IMR operates on the IRR. Masking of a higher priority input will not affect the interrupt request lines of lower priority.

INT (Interrupt)

This output goes directly to the CPU interrupt input. The VOH level on this line is designed to be fully compatible with the SAB 8080A/8085A/8086/8088/80186/80188/80286.

INTA (Interrupt Acknowledge)

INTA pulses will cause the SAB 8259A to release vectoring information onto the data bus. The format of this data depends on the system mode (µPM) of the SAB 8259A.

Data Bus Buffer

This tristate, bidirectional 8-bit buffer is used to interface the SAB 8259A to the system data bus. Control words and status information are transferred through the data bus buffer.

Read/Write Control Logic

The function of this block is to accept output commands from CPU. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store the various control formats for device operation. This function block also allows the status of the SAB 8259A to be transferred onto the data bus.

CS (Chip Select)

A low on this input enables the SAB 8259A. No reading or writing of the chip will occur unless the device is selected.

WR (Write)

A low on this input enables the CPU to write control words (ICWs and OCWs) to the SAB 8259A.

RD (Read)

A low on this input enables the SAB 8259A to send the status of the Interrupt Request Register (IRR), In-Service Register (ISR), the Interrupt Mask Register (IMR), or the interrupt level onto the data hus.

ΑO

This input signal is used in conjunction with \overline{WR} and \overline{RD} signals to write commands into the various command registers, as well as reading the various status registers of the chip. This line can be tied directly to one of the address lines.

The Cascade Buffer/Comparator

This function block stores and compares the IDs of all SAB 8259As used in the system. The associated three I/O pins (CAS0-2) are outputs when the SAB 8259A is used as a master and are inputs when the SAB 8259A is used as a slave. As a master, the SAB 8259A sends the ID of the interrupting slave device onto the CAS0-2 lines. The slave thus selected will send its preprogrammed subroutine address onto the data bus during the next one or two consecutive INTA pulses.

Interrupt Sequence

The powerful features of the SAB 8259A in a microcomputer system are its programmability and the interrupt routine addressing capability. The latter allows direct or indirect jumping to the specific interrupt routine requested without any polling of the interrupting devices. The normal sequence of events during an interrupt depends on the type of CPU being used.

The events occur as follows in an SAB 8080/85 system:

- One or more of the INTERRUPT REQUEST lines (IR7-0) are raised high, setting the corresponding IRR bit(s).
- 2. The SAB 8259A evaluates these requests, and sends an INT to the CPU, if appropriate.
- 3. The CPU acknowledges the INT and responds with an INTA pulse.
- 4. Upon receiving an INTA from the CPU group, the highest priority ISR bit is set, and the corresponding IRR bit is reset. The SAB 8259A will also release a CALL instruction code (11001101) onto the 8-bit data bus through its D7-0 pins.
- This CALL instruction will initiate two more INTA pulses to be sent to the SAB 8259A from the CPU group.
- These two INTA pulses allow the SAB 8259A to release its preprogrammed subroutine address onto the data bus. The lower 8-bit address is

- released at the first INTA pulse and the higher 8-bit address is released at the second INTA pulse.
- 7. This completes the 3-byte CALL instruction released by the SAB 8259A. In the AEOI¹⁾ mode the ISR bit is reset at the end of the third INTA pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt sequence.

The events occurring in an SAB 8086/8088/80186/80188/80286 system are the same until step 4.

- 4. Upon receiving an INTA from the CPU group, the highest priority ISR bit is set and the corresponding IRR bit is reset. The SAB 8259A does not drive the data bus during this cycle.
- The CPU will initiate a second INTA pulse.
 During this pulse, the SAB 8259A releases an 8-bit pointer onto the data bus where it is read by the CPU.
- 6. This completes the interrupt cycle. In the AEOI mode the ISR bit is reset at the end of the second INTA pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

If no interrupt request is present at step 4 of either sequence (i.e. the request was too short in duration) the SAB 8259A will issue an interrupt level 7. Both the vectoring bytes and the CAS lines will look like an interrupt level 7 was requested.

¹⁾ Automatic End of Interrupt

SAB 8259A

Absolute Maximum Ratings 1)

DC Characteristics

TA = 0 to 70°C; VCC = $5V \pm 10\%$

C	Danamatas	Limi	t values	Unit	Test conditions
Symbol	Parameter	min.	max.	Unit	rest conditions
VIL	Input low voltage	-0.5	0.8		
VIH	Input high voltage	2.0	VCC +0.5 V		-
VOL	Output low voltage	_	0.45	v	IOL = 2.2 mA
VOH	Output high voltage	2.4			$IOH = -400 \mu A$
VOLUMET.		3.5]_		IOH = -100 μA
VOH (INT)	Interrupt output high voltage	2.4			IOH = -400 μA
ILI	Input load current		110		$0V \le VIN \le VCC$
ILOL	Output leakage current		± 10	μΑ	$0.45\text{V} \leq \text{VOUT} \leq \text{VCC}$
ICC	VCC supply current	_	85	mA	All outputs open
	18:		-300		VIN = 0V
ILIR	IR input load current		10	μA	VIN = VCC

Capacitance

 $TA = 25^{\circ}C$; VCC = GND = 0V

Cumbal	Parameter	Limit	values	Unit	Test conditions	
Symbol	Farameter	min.	max.	Onit		
CIN	Input capacitance		10		fC = 1 MHz	
CI/O	I/O capacitance	_	20	pF	Unmeasured pins returned to GND	

¹⁾ Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC Characteristics

 $TA = 0 \text{ to } 70^{\circ}\text{C}; VCC = 5 \text{ V} \pm 10\%$

Timing Requirements

			Limi		Test		
Symbol	Parameter	SAE	8259A	SAB 8259A-2		Unit	condi-
		min.	max.	min.	max.		tions
TAHRL	A0/CS setup to RD/INTA↓	0		0			
TRHAX	A0/CS hold after RD/INTA↑] ້					
TRLRH	RD pulse width	235		160			
TAHWL	A0/CS setup to WR↓	0	7	0			_
TWHAX	A0/ CS hold after WR ↑	1					
TWLWH	WR pulse width	290	7	190			
TDVWH	Data setup to WR↑	240	7	160			
TWHDX	Data hold after WR↑	0		0			
TJLJH	Interrupt request width (low)	100	7	100			1)
TCVIAL	Cascade setup to second or third INTA (slave only)	55]-	40	_	ns	
TRHRL	End of RD to next RD End of INTA to next INTA within an INTA sequence only	160		160			_
TWHRL	End of WR to next WR	190		190			
TCUCL 2)	End of command to next command (not same command type)		500				
TCHCL ²)	End of INTA sequence to next INTA sequence	500		500			

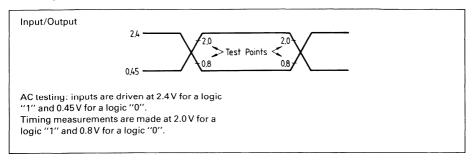
Timing Responses

			Limi		Test		
Symbol	Parameter	SAE	8259A	SAB	SAB 8259A-2		condi-
		min.	max.	min.	max.	1	tions
TRLDV	Data valid from RD/INTA↓	-	200	_	120		C of data bus
TRHDZ	Data float after RD/INTA↑	10	100	10	85	1	max. test C
TJHIH	Interrupt output delay		350		300	1	100 pF
TIALCV	Cascade valid from first INTA↓ (master only)		565		360		min. test C
TRLEL	Enable active from RD↓ or INTA↓	-	125	_	100	ns	CINT = 100 p
TRHEH	Enable inactive from RD↑ or INTA↑		150		150		C cascade =
TAHDV	Data valid from stable address		200		000		
TCVDV	Cascade valid to valid data		300		200		

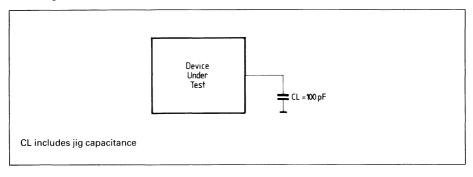
¹⁾ This is the low time required to clear the input latch in the edge-triggered mode.

²) Worst-case timing for TCHCL in an actual microprocessor system is typically much greater than 500 ns.

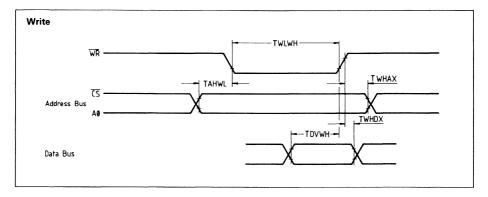
AC Testing Input, Output Waveform

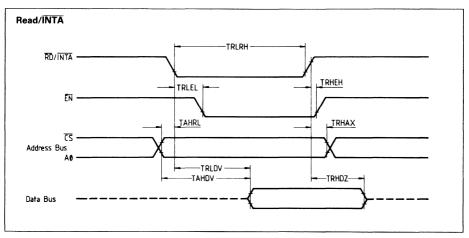


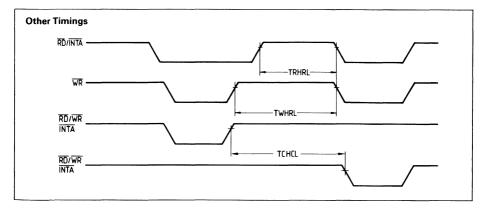
AC Testing Load Circuit

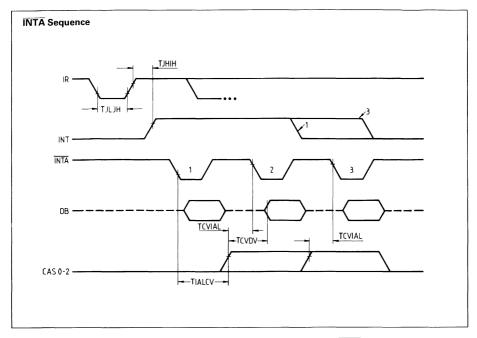


Waveforms





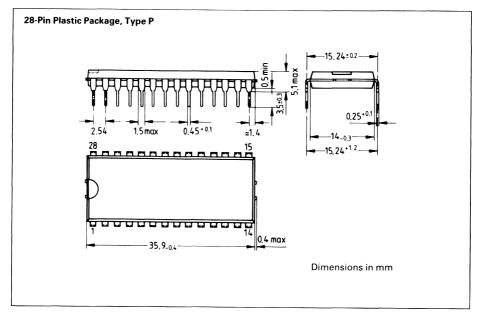




Notes: Interrupt output must remain high at least until leading edge of first INTA.

- 1) Cycle 1 in SAB 8086/88 systems, the data bus is not active.
- ²) Cycle 2.
- ³) Cycle 3 in SAB 8085 systems only.

Package Outline



SAB 8259A

Ordering Information

Туре	Description	Ordering Code
SAB 8259A	Programmable interrupt controller, 5 MHz, plastic package	Q67120-P46
SAB 8259A-2P	Programmable interrupt controller, 8 MHz, plastic package	Q67120-P81



SAB 8275 Programmable CRT Controller

- Programmable screen and character format
- 6 independent visual field attributes
- 11 visual character attributes (graphics capability)
- Cursor control (4 types)
- · Light pen detection and registers

- SAB 8051, SAB 8085, SAB 8086 and SAB 8088 compatible
- Dual row buffers
- Programmable DMA burst mode
- Single +5V supply
- High performance MYMOS technology
- Fully compatible with industry standard 8275

Pin configuration			Pin Names	
			LC0-LC3	Line Count
			DRQ	DMA Request
rall1	~~ <u></u>	Ъv«	DACK	DMA Acknowledge
1(2 2		P LAO	HRTC	Horizontal Retrace
LC1 🗖 3	31	LA1	VRTC	Vertical Retrace
LC0 🗆 4		LTEN	RD	Read Input
DRQ 5		S □ RVV S □ VSP	WR	Write Input
HRTC 7		GPA1	LPEN	Light Pen
VRTC 8	3.	GPA0	DB0-DB7	Bidirectional Three-State Data Bus Lines
RD □ 9	SAB 33	2 □ HLGT	LA0, LA1	Line Attribute Codes
₩R ☐ 10	8275 3	I DIRQ	LTEN	Light Enable
LPEN 11 DB0 12		D CC (6	RVV	Reverse Video
DB1 [13) (CS	VSP	Video Suppression
DB2 🗖 14	27) C(4	GPA0, GPA1	General Purpose Attribute Codes
DB3 🗆 15		<u> </u> (3	HLGT	Highlight
DB 4 16			IRQ	Interrupt Request
DB6 18		- L.	CCLK	Character Clock
DB7 19		<u> </u>	CC0-CC6	Character Codes
GND 20	21	DA0	CS	Chip Select
<u> </u>		-	A0	Port Address

The SAB 8275 programmable CRT controller is a single chip device to interface CRT raster scan displays. It is manufactured in Siemens advanced MYMOS technology. Its primary function is to refresh the display by buffering the information from main memory and keeping track of the

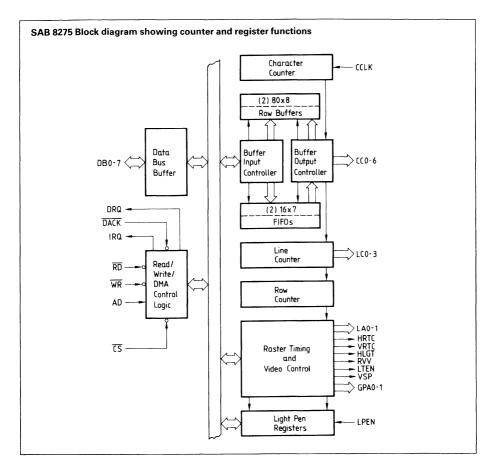
display position of the screen. The flexibility designed into the SAB 8275 will allow simple interface to almost any raster scan CRT display with a minimum of external hardware and software overhead.

Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function	
LC3 LC2 LC1 LC0	1 2 3 4	0	LINE COUNT: Output from the line counter which is used to address the character generator for the line positions on the screen.	
DRQ	5	0	DMA REQUEST: Output signal to the SAB 8237A DMA controller requesting a DMA cycle.	
DACK	6	1	DMA ACKNOWLEDGE: Input signal from the SAB 8237A DMA controller acknowledging that the requested DMA cy has been granted.	
HRTC	7	0	HORIZONTAL RETRACE: Output signal which is active dur the programmed horizontal retrace interval. During this per the VSP output is high and the LTEN output is low.	
VRTC	8	0	VERTICAL RETRACE: Output signal which is active during t programmed vertical retrace interval. During this period the VSP output is high and the LTEN output is low.	
RD	9	ı	READ INPUT: A control signal to read registers.	
WR	10	I	WRITE INPUT: A control signal to write commands into the control registers or write data into the row buffers during DMA cycle.	
LPEN	11	1	LIGHT PEN: Input signal from the CRT system signifying that a light pen signal has been detected.	
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7	12 13 14 15 16 17 18	1/0	BIDIRECTIONAL THREE-STATE DATA BUS LINES: The outputs are enable during a read of the C or P ports.	
LA0 LA1	39 38	0	LINE ATTRIBUTE CODES: These attribute codes have to be decoded externally by the dot/timing logic to generate the horizontal and vertical line combinations for the graphic displays specified by the character attribute codes.	
LTEN	37	0	LIGHT ENABLE: Output signal used to enable the video signa to the CRT. This output is active at the programmed underline cursor position, and at positions specified by attribute codes.	
RVV	36	0	REVERSE VIDEO: Output signal used to indicate the CRT circuitry to reverse the video signal. This output is active at the cursor position if a reverse video block cursor is programmed or at the positions specified by the field attribute codes.	

Pin Definitions and Functions (continued)

Symbol	Number	Input (I) Output (O)	Function	
VSP	35	0	VIDEO SUPPRESSION: Output signal used to blank the video signal to the CRT. This output is active: - During the horizontal and vertical retrace intervals. - at the top and bottom lines of rows if underline is programmed to be number 8 or greater. - when an end of row or end of screen code is detected. - when a DMA underrun occurs. - at regular intervals (1/16 frames frequency for cursor, 1/32 frame frequency for character and field attributes) – to create blinking displays as specified by cursor, character attribute, or field attribute programming.	
GPA1, GPA0	34 33	0	GENERAL-PURPOSE ATTRIBUTE CODES: Outputs which are enable by the general purpose field attribute codes.	
HLGT	32	0	HIGHLIGHT: Output signal used to intensify the display at particular positions on the screen as specified by the character attribute codes or field attribute codes.	
IRO	31	0	INTERRUPT REQUEST.	
CCLK	30	1	CHARACTER CLOCK (from dot/timing logic).	
CC6 CC5 CC4 CC3 CC2 CC1 CC0	29 28 27 26 25 24 23	0	CHARACTER CODES: Output from the row buffers used for character selection in the character generator.	
CS	22	ı	CHIP SELECT: The read and write are enabled by $\overline{\text{CS}}$.	
A0	21	ı	PORT ADDRESS: A high input on A0 selects the "C" port or command registers and a low input selects the "P" port or parameter registers.	
VCC	40	-	+5V Power supply.	
GND	20	_	Ground (0V)	



Functional Description

Data bus buffer

This three-state, bidirectional, 8-bit buffer is used to interface the SAB 8275 to the system data bus.

This functional block accepts inputs from the system control bus and generates control signals for overall device operation. It contains the command, parameter, and status registers that store various control formats for the device functional definition.

A0	Operation	Register	
0	Read	PREG	
0	Write	PREG	
1	Read	SREG	
1	Write	CREG	

A0	RD	WR	CS	
0	1	0	0	Write SAB 8275 parameter
0	0	1	0	Read SAB 8275 parameter
1	1	0	0	Write SAB 8275 command
1	0	1	0	Read SAB 8275 status
Х	1	1	0	Three-state
Χ	X	X	1	Three-state

RD (Read)

A "low" on this input informs the SAB 8275 that the CPU is reading data or status information from the SAB 8275.

WR (Write)

A "low" on this input informs the SAB 8275 that the CPU is writing data or control words to the SAB 8275.

CS (Chip select)

A "low" on this input selects the SAB 8275. No reading or writing will occur unless the device is selected. When \overline{CS} is high, the data bus in the float state and \overline{RD} and \overline{WR} will have no effect on the chip.

DRQ (DMA request)

A "high" on this output informs the DMA controller that the SAB 8275 desires a DMA transfer.

DACK (DMA acknowledge)

A "low" on this input informs the SAB 8275 that a DMA cycle is in progress.

IRQ (Interrupt request)

A "high" on this output informs the CPU that the SAB 8275 desires interrupt service.

Character counter

The character counter is a programmable counter that is used to determine the number of characters to be displayed per row and the length of the horizontal retrace interval. It is driven by the CCLK (character clock) input, which should be a derivative of the external dot clock.

Line counter

The line counter is a programmable counter that is used to determine the number of horizontal lines (sweeps) per character row. Its outputs are used to address the external character generator ROM.

Row counter

The row counter is a programmable counter that is used to determine the number of character rows to be displayed per frame and length of the vertical retrace interval.

Light pen registers

The light pen registers are two registers that store the contents of the character counter and the row counter whenever there is a rising edge on the LPEN (Light Pen) input.

Note: Software correction is required.

Raster timing and video controls

The raster timing circuitry controls the timing of the HRTC (Horizontal Retrace) and VRTC (Vertical Retrace) outputs. The video control circuitry controls the generation of LA0-1 (line attribute), HGLT (highlight), RVV (reverse video), LTEN (Light enable), VSP (video suppress), and GPA0-1 (general purpose attribute) outputs.

Row buffers

The row buffers are two 80 character buffers. They are filled from the microcomputer system memory with the character codes to be displayed. While one row buffer is displaying a row of characters, the other is being filled with the next row of characters.

FIFOs

There are two 16 character FIFOs in the 8275. They are used to provide extra row buffer length in the transparent attribute mode.

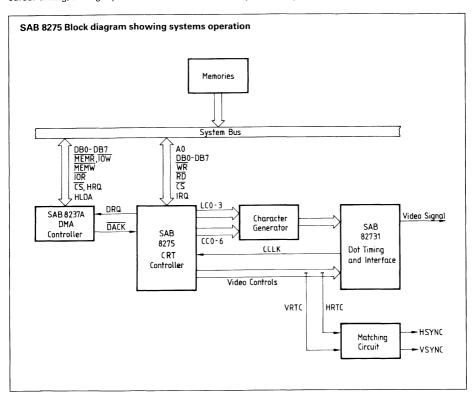
Buffer input/output controllers

The buffer input/output controllers decode the characters being placed in the row buffers. If the character is a character attribute, field attribute or special code, these controllers control the appropriate action (Examples: An "end of screenstop DMA" special code will cause the buffer input controller to stop further DMA requests. A "highlight" field attribute will cause the buffer output controller to activate the HGLT output).

System Operation

The SAB 8275 is programmable to a large number of different display formats. It provides raster timing, display row buffering, visual attribute decoding, cursor timing, and light pen detection.

It is designed to interface with the SAB 8237A DMA controller and standard character generator ROMs for dot matrix decoding. Dot level timing must be provided by external circuitry.



Raster timing

The character counter is driven by the character clock input (CCLK). It counts out the characters being displayed (programmable from 1 to 80). It then causes the line counter to increment, and it starts counting out the horizontal retrace (programmable from 2 to 32). This is constantly repeated.

The line counter is driven by the character counter. It is used to generate the line address outputs (LCO-3) for the character generator. After it counts all of the lines in a character row (programmable from 1 to 16), it increments the row counter, and starts over again. (See Character Format Section for detailed description of Line Counter functions.)

The row counter is an internal counter driven by the line counter. It controls the functions of the row buffers and counts the number of character rows displayed.

After the row counter counts all of the rows in a frame (programmable from 1 to 64), it starts counting out the vertical retrace interval (programmable from 1 to 4).

The video suppression output (VSP) is active during horizontal and vertical retrace intervals.

Dot level timing circuitry must synchronize these outputs with the video signal to the CRT display.

DMA timing

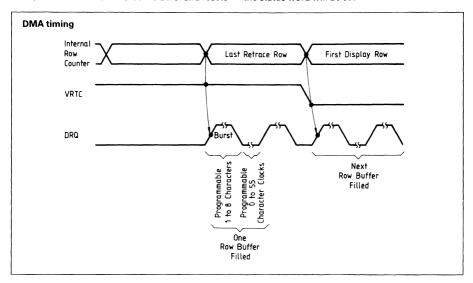
The SAB 8275 can be programmed to request burst DMA transfers of 1 to 8 characters. The interval between bursts is also programmable (from 0 to 55 character clock periods \pm 1). This allows the user to tailor his DMA overhead to fit his system needs.

The first DMA request of the frame occurs one row time before the end of vertical retrace. DMA requests continue as programmed, until the row buffer is filled. If the row buffer is filled in the middle of a burst, the SAB 8275 terminates the burst and resets

the burst counter. No more DMA requests will occur until the *beginning* of the *next* row. At that time, DMA requests are activated as programmed until the other buffer is filled.

The DMA request for a row will start at the first character clock of the preceding row. If the burst mode is used, the first DMA request may occur a number of character clocks later. This number is equal to the programmed burst space.

If, for any reason, there is a DMA underrun, a flag in the status word will be set.

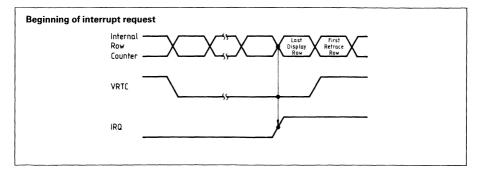


The DMA controller is typically initialized for the next frame at the end of the current frame.

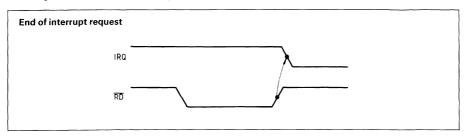
Interrupt timing

The SAB 8275 can be programmed to generate an interrupt request at the end of each frame. This can

be used to reinitialize the DMA controller. If the SAB 8275 interrupt enable flag is set, an interrupt request will occur at the *beginning* of the *last display row*.



IRQ will go inactive after the status register is read.



A reset command will also cause IRQ to go inactive, but this is not recommended during normal service.

Another method of reinitializing the DMA controller is to have the DMA controller itself interrupt on terminal count. With this method, the SAB 8275 interrupt enable flag should not be set.

Note: Upon power-up, the SAB 8275 interrupt Enable Flag may be set. As a result, the user's cold start routine should write a reset command to the SAB 8275 before system interrupts are enabled.

General systems operational description

The SAB 8275 provides a "window" into the micro-computer system memory.

Display characters are retrieved from memory and displayed on a row by row basis. The SAB 8275 has two row buffers. While one row buffer is being used for display, the other is being filled with the nextrow of characters to be displayed. The number of display characters per row and the number of character rows per frame are software programmable, providing easy interface to most CRT displays. (see programming section.)

The SAB 8275 requests DMA to fill the row buffer that is not being used for display. DMA burst length and spacing is programmable. (See programming section.)

The SAB 8275 displays character rows one line at a time.

The number of lines per character row, the underline position, and blanking of top and bottom lines are programmable. (See programming section.)

The SAB 8275 provides special control codes which can be used to minimize DMA or software overhead. It also provides visual attribute codes to cause special action or symbols on the screen without the use of the character generator (see visual attribute section).

The SAB 8275 also controls raster timing. This is done by generating horizontal retrace (HRTC) and

vertical retrace (VRTC) signals. The timing of these signals is programmable.

The SAB 8275 can generate a cursor. Cursor location and format are programmable. (See programming section.)

The SAB 8275 has a light pen input and registers. The light pen input is used to load the registers. Light pen registers can be read on command. (See programming section.)

Display row buffering

Before the start of a frame, the SAB 8275 requests DMA and one row buffer is filled with characters.

When the first horizontal sweep is started, character codes are output to the character generator from the row buffer just filled. Simultaneously, DMA begins filling the other row buffer with the next row of characters.

After all the lines of the character row are scanned, the roles of the two row buffers are reversed and the same procedure is followed for the next row.

This is repeated until all of the character rows are displayed.

Screen format

The SAB 8275 can be programmed to generate from 1 to 80 characters per row, and from 1 to 64 rows per frame.

The SAB 8275 can also be programmed to blank alternate rows. In this mode, the first row is displayed, the second blanked, the third displayed, etc. DMA is not requested for the blanked rows.

Row format

The SAB 8275 is designed to hold the line count stable while outputting the appropriate character codes during each horizontal sweep. The line count is incremented during horizontal retrace and the whole row of character codes are output again during the next sweep. This is continued until the whole character row is displayed.

The number of lines (horizontal sweeps) per character row is programmable from 1 to 16.

The output of the line counter can be programmed to be in one of two modes.

In mode 0, the output of the line *counter* is the same as the line *number*.

In mode 1, the line *counter* is offset by one from the line *number*.

Note: In mode 1, while the *first* line (line number 0) is being displayed, the *last* count is output by line counter.

Mode 0 is use ful for character generators that leave address zero blank and start at address 1, Mode 1 is useful for character generators which start at address zero.

Underline placement is also programmable (from line *number* 0 to 15). This is independent of the line *counter* mode.

If the line *number* of the underline is greater than 7 (line *number* MSB = 1), then the top and bottom lines will be blanked.

If the line *number* of the underline is less than or equal to 7 (line *number* MSB = 0), then the top and bottom lines will *not* be blanked.

If the line *number* underline is greater than the maximum number of lines, the underline will not appear.

Blanking is accomplished by the VSP (Video Suppression) signal. Underline is accomplished by the LTEN (light enable) signal.

Dot format

Dot width and character width are dependent upon the external timing and control circuitry.

Dot level timing circuitry should be designed to accept the parallel output of the character generator and shift it out serially at the rate required by the CRT display.

Dot width is a function of dot clock frequency.

Character width is a function of the character generator width.

Horizontal character spacing is a function of the shift register length.

Note: Video control and timing signals must be synchronized with the video signal due to the character generator access delay.

Visual Attributes and Special Codes

The characters processed by the SAB 8275 are 8-bit quantities. The character code outputs provide the character generator with 7 bits of address. The most significant bit is the extra bit and it is used to determine if it is a normal display character (MSB = 0), or if it is a Visual Attribute or Special Code (MSB = 1).

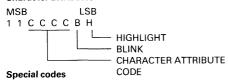
There are two types of visual attribute codes. They are character attributes and field attributes.

Character attribute codes

Character attribute codes are codes that can be used to generate graphics symbols without the use of a character generator. This is accomplished by selectively activating the line attribute outputs (LAO-1), the video suppression output (VSP), and the light enable output. The dot level timing circuitry can use these signals to generate the proper symbols.

Character attributes can be programmed to blink or be highlighted individually. Blinking is accomplished with the video suppression output (VSP). Blink frequency is equal to the screen refresh frequency divided by 32. Highlighting is accomplished by activating the highlight output (HGLT).

Character attributes



Four special codes are available to help reduce memory, software or DMA overhead.

Special control character



s s	Function
0 0 0 1 1 0	End of Row End of Row-stop DMA End of Screen End of Screen-stop DMA

The End-of-Row code (00) activates VSP and holds it to the end of the line.

The End-of-Row-Stop DMA code (01) causes the DMA control logic to stop DMA for the rest of the row when it is written into the row buffer. It affects the display in the same way as the end-of-row code (00).

The end-of-screen code (10) activates VSP and holds it to the end of the frame.

The end-of-screen-stop DMA code (11) causes the DMA control logic to stop DMA for the rest of the frame when it is written into the row buffer. It affects the display in the same way as the end-of-screen code (10).

If the stop DMA feature is not used, all characters after an end-of-row character are ignored, except for the end-of-screen character, which operates normally. All characters after an end-of-screen character are ignored.

Note: If a stop DMA character is not the last character in a burst or row, DMA is not stopped until after the next character is read. In this situation, a dummy character must be placed in memory after the stop DMA character.

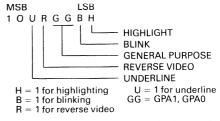
Field attributes

The field attributes are control codes which affect the visual characteristics for a field of characters, starting at the character following the code up to, and including, the character which precedes the *next* field attributes are reset during the vertical retrace interval

There are six field attributes:

- Blink Characters following the code are caused to blink by activating the Video Suppression Output (VSP). The blink frequency is equal to the screen refresh frequency divided by 32.
- Highlight Characters following the code are caused to be highlighted by activating the Highlight Output (HGLT).
- Reverse Video Characters following the code are caused to appear with reverse video by activating the Reverse Video Output (RVV).
- Underline Characters following the code are caused to be underlined by activating the Light Enable Output (LTEN).
- 6. General Purpose There are two additional SAB 8275 outputs which act as general purpose, independently programmable field attributes. GPA0 – 1 are active high outputs.

Field attribute code



* More than one attribute can be enabled at the same time. If the blinking and reverse video attributes are enabled simultaneously, only the reversed characters will blink.

The SAB 8275 can be programmed to provide visible or invisible field attribute characters.

If the SAB 8275 is programmed in the visible field attribute mode, all field attributes will occupy a position on the screen. They will appear as blanks caused by activation of the video suppression output (VSP). The chosen visual attributes are activated after this blanked character.

If the SAB 8275 is programmed in the invisible field attribute mode, the SAB 8275 FIFO is activated.

Each row buffer has a corresponding FIFO. These FIFOs are 16 characters by 7 bits in size.

When a field attribute is placed in the row buffer during DMA, the buffer input controller recognizes it and places the next character in the proper FIFO.

When a field attribute is placed in the buffer output controller during display, it causes the controller to immediately put a character from the FIFO on the character code outputs (CCO-8). The chosen visual attributes are also activated.

Since the FIFO in 16 characters long, no more then 16 field attribute characters may be used per line in this mode. If more are used, a bit in the status word is set and the first characters in the FIFO are written over and lost.

Note: Since the FIFO is 7 bits wide, the MSB of any characters put in it are stripped off. Therefore, a visual attribute or special code must *not* immediately follow a field attribute code. If this situation does occur, the visual attribute or special code will be treated as normal display character.

Field and character attribute interaction

Character attribute symbols are affected by the reverse video (RVV) and general purpose (GPA0 - 1) field attributes. They are not affected by underline, blink or highlight field attribute; however, these characteristics can be programmed *individually* for character attribute symbols.

Cursor timing

The cursor location is determined by a cursor row register and a character position register which are located by command to the controller. The cursor can be programmed to appear on the display as:

- a blinking underline
- 2. a blinking reverse video block
- 3. a non-blinking underline
- 4. a non-blinking reverse video block

The cursor blinking frequency is equal to the screen refresh frequency divided by 16.

If a non-blinking reverse video *cursor* appears in a non-blinking reverse video *field*, the cursor will appear as a normal video block.

If a non-blinking underline *cursor* appears in a nonblinking underline *field*, the cursor will not be visible.

Light pen detection

A light pen consists of a micro switch and a tiny light sensor. When the light pen is pressed against the CRT screen, the micro switch enable the light sensor. When the raster sweep reaches the light sensor, it triggers the light pen output.

If the output of the light pen is presented to the SAB 8275 LPEN input, the row and character position coordinates are stored in a pair of registers. These registers can be read on command. A bit in the status word is set, indicating that the light pen signal was detected. The LPEN input must be a 0 to 1 transition for proper operation.

Note: Due to internal and external delays, the character position coordinate will be off by at least three character positions. This has to be corrected in software.

Device programming

The SAB 8275 has two programming registers, the command register (CREG) and the parameter register (PREG). It also has a status register (SREG). The command register can only be written into and the Status registers can only be read from. They are addressed as follows:

$\overline{A_0}$	operation	register
0	Read	PREG
0	Write	PREG
1	Read	SREG
1	Write	CREG

The SAB 8275 expects to receive a command and a sequence of 0 to 4 parameters, depending on the command. If the proper number of parameter bytes are not received before another command is given, a status flag is set, indicating an improper command.

Instruction Set

The SAB 8275 instruction set consists of 8 commands.

Command	No. of parameter bytes
Reset	4
Start Display	0
Stop Display	0
Read Light Pen	2
Load Cursor	2
Enable Interrupt	0
Disable Interrupt	0
Preset Counters	l o

In addition, the status of the SAB 8275 (SREG) can be read by the CPU at any time.

1 Reset command

	Operation	A0	Description	NA	SB	D	ata	bus	3	10	SB
	Operation	AU	Description	IVI.	36						<u> </u>
Command	Write	1	Reset command	0	0	0	0	0	0	0	0
	Write	0	Screen Comp Byte 1	S	Н	Н	Н	Н	Н	Н	Н
Parameters	Write	0	Screen comp Byte 2	٧	٧	R	R	R	R	R	R
Taramotors	Write	0	Screen comp Byte 3	U	U	U	U	L	L	L	L
	Write	0	Screen comp Byte 4	М	F	С	С	Z	Z	Z	Z

Action – After the reset command is written, DMA requests stop, SAB 8275 interrupts are disabled, and the VSP output is used to blank the screen. HRTC and VRTC continue to run. HRTC and VRTC timing are random on power-up.

As parameters are written, the screen composition is defined.

Parameter - S Spaced rows

S	Functions
0	Normal rows
1	Spaced Rows

Parameter - HHHHHHHH	Harizantal	labaractore	1000
Parameter – HHHHHHH	Horizonia	i characiers.	row

Н	Н	Н	Н	Н	Н	Н	No. of characters per row
0	0	0	0	0	0	0	1
0	0	0	0	0	0	1	2
0	0	0	0	0	1	0	3
1	0	0	1	1	1	1	80
1	0	1	0	0	0	0	Undefined
1	1	1	1	1	1	1	Undefined

Parameter - RRRRRR Vertical rows/frame

R	R	R	R	R	R	No. of rows/frame
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
1	1	1	1	1	1	64

Parameter - UUUU Underline placement

U	U	U	U	Line number of underline
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
1	1	1	1	16

Parameter - VV Vertical retrace row count

٧	V	No. of row counts per VRTC
0	0	1
0	1	2
1	0	3
1	1	4

Note: uuuu MSB determines blanking of top and botton lines (1 = blanked, 0 = not blanked).

Parameter – LLLL Number of lines per character row Parameter – ZZZZ Horizontal retrace count

L	L	L	L	No. of lines/row
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
1	1	1	1	16

Z	Z	Z	Z	No. of character counts per HRTC
0	0	0	0	2
0	0	0	1	4
0	0	1	0	6
1	1	1	1	32

Parameter - M Line Counter Mode

M	Line counter mode
0	Mode 0 (non-offset)
1	Mode 1 (offset by 1 count)

Parameter - F Field attribute mode

F	Field attribute mode
0	Transparent
1	Non-transparent

Parameter - CC Cursor format

С	С	Cursor format
0	0	Blinking reverse video block
0	1	Blinking underline
1	0	Nonblinking reverse video block
1	1	Nonblinking underling

2 Start display command

				Data bus					s				
	Operation	A0	Description	MSB					LSI				
Command	Write	1	Start display	0	0	1	S	S	S	В	В		
No parameters													

SSS Burst space code

S	S	S	No. of character clocks between DMA requests
0	0	0	0
0	0	1	7
0	1	0	15
0	1	1	23
1	0	0	31
1	0	1	39
1	1	0	47
1	1	1	55

BB Burst count code

В	В	No. of DMA cycles per burst
0	0	1
0	1	2
1	0	4
1	1	8

Action – SAB 8275 interrupts are enabled, DMA requests begin, video is enabled, interrupt enable and video enable status flags are set.

3 Stop display command

				Data bus									
	Operation	A0	Description	MSB					LSB				
Command	Write	1	Stop display	0	1	0	0	0	0	0	0		
No parameters													

Action – Disables video, interrupts remain enabled. HRTC and VRTC continue to run, video enable status flag is reset, and the "Start display" command must be given to re-enable the display.

4 Read light pen command

		I		Data bus
	Operation	A0	Description	MSB LSB
Command	Write	1	read light pen	0 1 1 0 0 0 0 0
Parameters	Read	0	Char. number	(Char. position in row)
	Read	0	Row number	(Row number)

Action – The SAB 8275 is conditioned to supply the contents of the light pen position registers in the next two read cycles of the parameter register. Status flags are not affected.

Note: Software correction of light pen position is required.

5 Load cursor position

				Data	Data bus								
	Operation	A0	Description	MSB		LSI							
Command	Write	1	Load cursor	1 0 0 0	0 0	0	0						
Parameters	Write	0	Char. number	(Char. position in row)									
	Write	0	Row number	(Row number)	(Row number)								

Action – The SAB 8275 is conditioned to place, the next two parameter bytes into the cursor position registers. Status flags not affected.

6 Enable interrupt command

				ta bus						
	Operation	A0	Description	ИSВ					L	SB
Command	Write	1	Enable interrupt	0	1	0	0	0	0	0
No parameters										

Action – The interrupt enable status flag is set and interrupts are enabled.

7 Disable interrupt command

				Data bus									
	Operation	A0	Description	М	SB					L	SB		
Command	Write	1	Disable interrupt	1	1	0	0	0	0	0	0		
No parameters													

Action – Interrupts are disabled and the interrupt enable status flag is reset.

8 Preset counters command

			Data bus								
	Operation	A0	Description	M	SB					L	SB
Command	Write	1	Preset counters	1	1	1	0	0	0	0	0
No parameters											_

Action – The internal timing counters are preset, corresponding to a screen display position at the top left corner. Two character clocks are required for this operation. The counters will remain in this state until any other command is given.

This command is useful for system debug and synchronization of clustered CRT displays on a single CPU. After this command, two additional clock cycles are required before the first character of the first row is put out.

Status flags

	Operation	Α0	Description	Data I MSB	ous LSB
Command	Read	1	Status word	0 IE IR LP IC	VE DU F0

- IE (Interrupt Enable) Set or reset by command. It enables vertical retrace interrupt. It is automatically set by a "Start Display" command reset with the "Reset" command.
- IR (Interrupt Request) This flag is set at the beginning of display of the last row of the frame if the interrupt enable flag is set. It is reset after a status read operation.

- LP This flag is set when the light pen input (LPEN) is activated and the light pen registers have been loaded. This flag is automatically reset after a status read.
- IC (Improper Command) This flag is set when a command parameter string is too long or too short. The flag is automatically reset after a status read.
- VE (Video Enable) This flag indicates that video operation of the CRT is enabled. This flag is set on a "Start Display" command, and reset on a "Stop Display" or "Reset" command.
- DU (DMA Underrun) This flag is set whenever a data underrun occurs during DMA transfers. Upon detection of DU, the DMA operation is stopped and the screen is blanked until after the vertical retrace interval. This flag is reset after a status read.
- FO (FIFO Overrun) This flag is set whenever the FIFO is overrun. It is reset on a status read.

Absolute Maximum Ratings 1)

Temperature under bias 0 to $+70\,^{\circ}\mathrm{C}$ Storage temperature $-65\,$ to $+150\,^{\circ}\mathrm{C}$ All output ans supply and supply voltages $-0.5\,$ to $+7\,$ V All input voltages $-0.5\,$ to $+5.5\,$ V Power dissipation 1,0 W

DC Characteristics

 $(TA = 0^{\circ}C \text{ to } 70^{\circ}C, VCC = 5V \pm 5\%)$

Cumbal	Parameter	Limit values		I Imia	Test condition		
Symbol		Min.	Max.	Unit	rest condition		
VIL	Input low voltage	-0.5	0.8				
VIH	Input high voltage	2.0	VCC+0.5V	v			
VOL	Output low voltage	_	0.45	•	IOL = 2.2 mA		
VOH	Output high voltage	2.4	_		IOH = -400 μA		
IIL	Input load current		+ 10	uА	VIN = VCC to 0 V		
IOFL	Output float leakage]-	- 10		- 10		VOUT = VCC to 0.45 V
ICC	VCC supply current	1	160	mA	_		

Capacitance

 $(TA = 25^{\circ}C, VCC = GND = 0 V)$

Complete	Donom et al.	Limit values		11-:4	T	
Symbol	Parameter	Min.	Max.	Unit	Test condition	
CIN	Input capacitance		10	рF	fc = 1 MHz	
CI/O	I/O capacitance		20	Pi	Unmeasured pins returned to GND	

Stresses above those listed under "absolute maximum ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC Characteristics (SAB 8275)

(TA = 0 C to 70°C, VCC = 5.0 V \pm 5%, GND = 0 V)

Clock timing

	Parameter	Lin	nit values	Units	T
Symbol		Min.	Max.	Units	Test condition
TCLK	Clock period	480			_
TKH	Clock high	240	_		
TKL	Clock low	160		ns	
TKR	Clock rise	5	30		
TKF	Clock fall	J			

Bus parameters Read cycle

	Parameter	Limit values		Unit	Test condition
Symbol		Min.	Max.	Unit	lest condition
TAR	Address stable before READ	0]		
TRA	Address hold time for READ	Ů	_		-
TRR	READ pulse width	250		ns	
TRD	Data delay from READ		200		CL = 150 pF
TDF	READ to data floating		100		02 = 100 pi

Write cycle

		Lir	nit values	Unit	Tank and diking
Symbol	Parameter	Min.	Max.	Unit	Test condition
TAW	Address stable before WRITE	0			
TWA	Address hold time for WRITE	Ů			
TWW	WRITE pulse width	250	_	ns	-
TDW	Data seting time for WRITE	150			
TWD	Data hold time for WRITE	0			

Other timings

Symbol	Parameter	Lir	Limit values		T4		
Symbol		Min.	Max.	Unit	Test condition		
TCC	Character code output delay		150				
THR	Horizontal retrace output delay		200				
TLC	Line count output delay		400		CL = 50 pF		
TAT	Control-attribute output delay		275				
TVR	Vertical retrace output delay	-	275	ns			
TRI	IRQ↓ from RD↑		250				
TWQ	DRQ↑ from WR↑		230				
TRQ	DRQ↓ from WR↓		200				
TLR	DACK↓ to WR↓	0					
TRL	WR↑ to DACK↑	7	-		_		
TPR	LPEN rise	-	50				
TPH	LPEN hold	100	_				

AC Characteristics (SAB 8275-2)

(TA = 0 C to 70°C, VCC = 5.0 V \pm 5%, GND = 0 V)

Clock timing

	Parameter	Lin	nit values		Test condition
Symbol		Min.	Max.	Unit	
TCLK	Clock period	320			
TKH	Clock high	120	-		
TKL	Clock low	120		ns	
TKR	Clock rise	5	30		
TKF	Clock fall	J			

Bus parameters Read cycle

	Parameter	Limit value		11	T
Symbol		Min.	Max.	Unit	Test condition
TAR	Address stable before READ				
TRA	Address hold time for READ				_
TRR	READ pulse width	250		ns	
TRD	Data delay from READ		200		CL = 150 pF
TDF	READ to data floating		100		CL = 150 pF

Write cycle

<u> </u>	Parameter	Limit values		1.1	Tank as a dikina
Symbol		Min.	Max.	Unit	Test condition
TAW	Address stable before WRITE	0			
TWA	Address hold time for WRITE	0			
TWW	WRITE pulse width	250	_	ns	_
TDW	Data seting time for WRITE	150			
TWD	Data hold time for WRITE	0			

Other timings

Combal	Parameter	Lin	Limit values		Tank and dising
Symbol		Min.	Max.	Unit	Test condition
TCC	Character code output delay		150		
THR	Horizontal retrace output delay		130	ns	
TLC	Line count output delay				CL = 50 pF
TAT	Control-attribute output delay	-	250		
TVR	Vertical retrace output delay				
TRI	IRQ↓ from RD↑				
TWQ	DRQ↑ from WR↑				
TRQ	DRQ↓ from WR↓		200		
TLR	DACK to WR	0			
TRL	WR↑ to DACK↑	Ů			
TPR	LPEN rise	-	50	7	
TPH	LPEN hold	100	_	7	

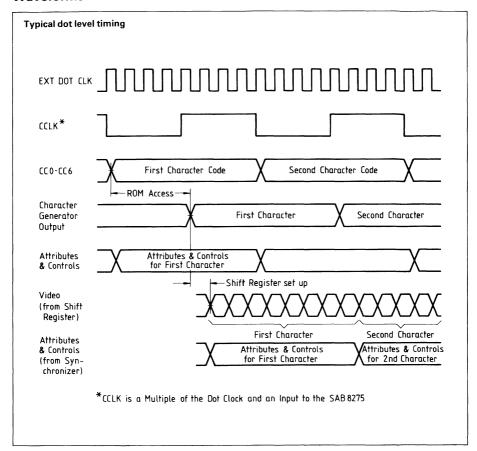
A.C. Testing input/output

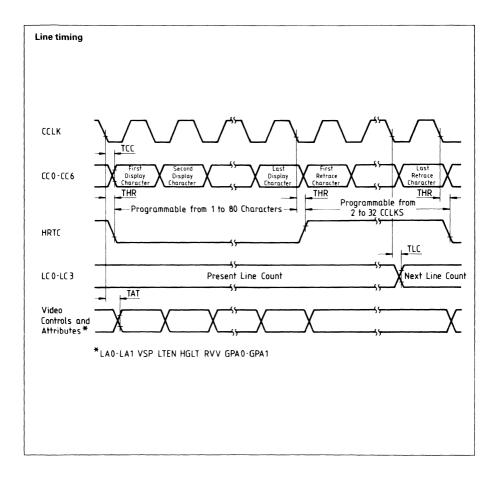


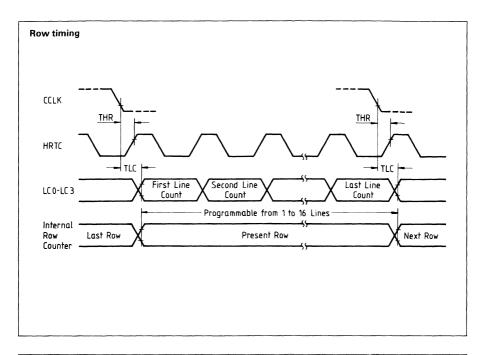
AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".

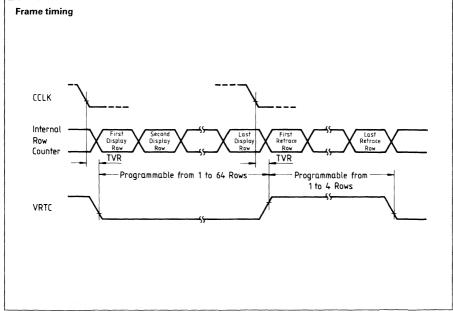
A.C. Testing load circuit Device Under Test CL Includes Jig Capacitance

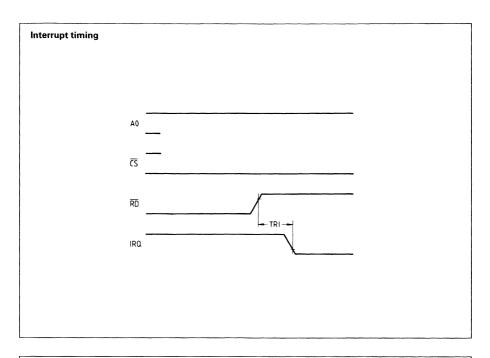
Waveforms

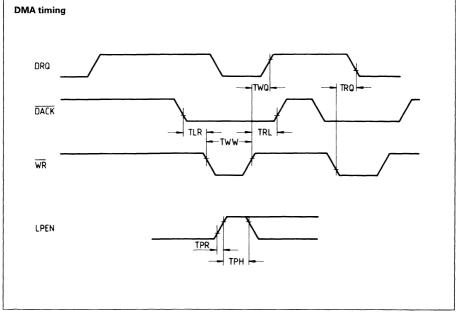


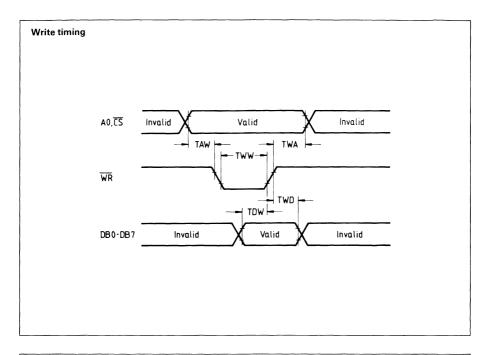


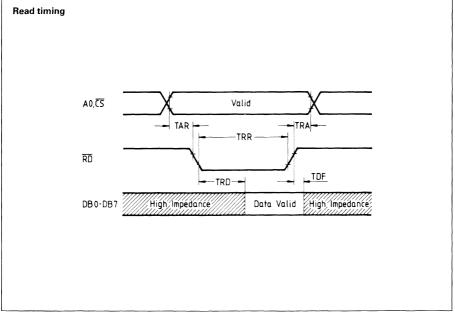


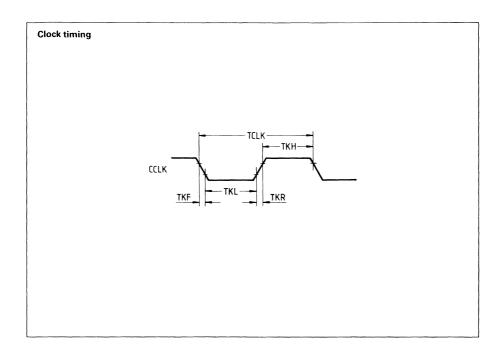




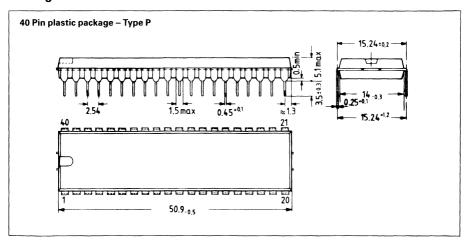








Package outline



SAB 8275

Ordering Information

Туре	Description	Ordering code
SAB 8275-P	Programmable CRT controller, 2 MHz	Q67120-P58
SAB 8275-2-P	Programmable CRT controller, 3 MHz	Q67120-P92



SAB 8276 Small System CRT Controller

- Programmable screen and character format
- 6 independent visual attributes
- Cursor control (4 types)
- SAB 8051, SAB 8085, SAB 8086 and SAB 8088 compatible
- Dual row buffers
- Programmable DMA burst mode
- Single +5V supply
- High performance MYMOS technology
- Fully compatible with industry standard 8276

Pin configuration		Pin Names	Pin Names		
		LC0-LC3	Line Count		
LC3 1 LC2 1 2	40 VCC	BRDY	Buffer Ready		
LC1 [] 3	39 NC 38 NC	BS	Buffer Select		
100 4	37 DLTEN	HRTC	Horizontal Retrace		
BRDY 5	36 🗆 RVV	VRTC	Vertical Retrace		
BS C	35 VSP	RD	Read Input		
HRTC 7	34 GPA1 33 GPA0	WR	Write Input		
RD 19	32 HLGT	DB0-DB7	Bidirectional Three-State Data Bus Line		
WR ☐ 10 827		LTEN	Light Enable		
NC 📑 11	30 CCLK	RVV	Reverse Video		
DB0 12 DB1 13	29 006	VSP	Video Suppression		
0B2 14	27 7 664	GPA0, GPA1	General Purpose Attribute Codes		
DB3 🗆 15	26 🗆 ((3	HLGT	Highlight		
DB 4 🖂 16	25 🗆 СС 2	INT	Interrupt Output		
DB 5 17	24 0001	CCLK	Character Clock		
DB6 18 DB7 19	23 000				
GND 19	22 : (S 21 : CIP	CC0-CC6	Character Codes		
370 420		CS	Chip Select		
		C/P	Port Address		

The SAB 8276 Small System CRT Controller is a single chip device to interface CRT raster scan displays. It is manufactured in Siemens advanced MYMOS technology. Its primary function is to refresh the display by buffering the information from main memory and keeping track of the

display position of the screen. The flexibility designed into the SAB 8276 will allow simple interface to almost any raster scan CRT display with a minimum of external hardware and software overhead.

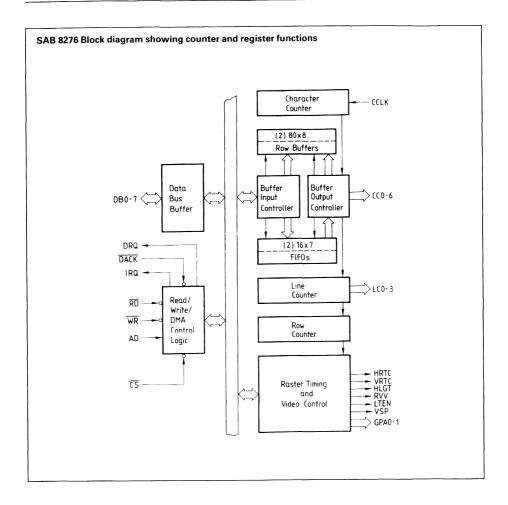
2.85

Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function		
LC3 LC2 LC1 LC0	1 2 3 4	0	LINE COUNT: Output from the line counter which is used to address the character generator for the line positions on the screen.		
BRDY	5	1	BUFFER READY: Output signal indicating that a row buffer is ready for loading of character data.		
BS	6	0	BUFFER SELECT: Input signal enabling WR for character data into the row buffers.		
HRTC	7	0	HORIZONTAL RETRACE: Output signal which is active during the programmed horizontal retrace interval. During this period the VSP output is high and the LTEN output is low.		
VRTC	8	0	VERTICAL RETRACE: Output signal which is active during the programmed vertical retrace interval. During this period the VSP output is high and the LTEN output is low.		
RD	9	ı	READ INPUT: A control signal to read registers.		
WR	10	I	WRITE INPUT: A control signal to write commands into the control registers or write data into the row buffers during a DMA cycle.		
NC	11		No Connection		
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7	12 13 14 15 16 17 18 19	1/0	BIDIRECTIONAL THREE-STATE DATA BUS LINES: The outputs are enable during a read of the C or P ports.		
NC	38/39		No Connection		
LTEN	37	0	LIGHT ENABLE: Output signal used to enable the video signal to the CRT. This output is active at the programmed underline cursor position, and at positions specified by attribute codes.		
RVV	36	0	REVERSE VIDEO: Output signal used to indicate the CRT circuitry to reverse the video signal. This output is active at the cursor position if a reverse video block cursor is programmed or at the positions specified by the field attribute codes.		

Pin Definitions and Functions (continued)

Symbol	Number	Input (I) Output (O)	Function			
VSP	35	0	VIDEO SUPPRESSION: Output signal used to blank the video signal to the CRT. This output is active: - During the horizontal and vertical retrace intervals. - at the top and bottom lines of rows if underline is programmed to be number 8 or greater. - when an end of row or end of screen code is detected. - when a DMA underrun occurs. - at regular intervals (1/16 frames frequency for cursor, 1/32 frame frequency for character and field attributes) – to create blinking displays as specified by cursor or field attribute programming.			
GPA1 GPA0	34 33	0	GENERAL-PURPOSE ATTRIBUTE CODES: Outputs which a enable by the general purpose field attribute codes.			
HLGT	32	О	HIGHLIGHT: Output signal used to intensify the display at particular positions on the screen as specified by the character attribute codes or field attribute codes.			
INT	31	0	INTERRUPT OUTPUT			
CCLK	30	ı	CHARACTER CLOCK (from dot/timing logic).			
CC6 CC5 CC4 CC3 CC2 CC1 CC0	29 28 27 26 25 24 23	O	CHARACTER CODES: Output from the row buffers used for character selection in the character generator.			
CS	22	ı	CHIP SELECT: The read and write are enabled by $\overline{\text{CS}}$.			
C/P	21	I	PORT ADDRESS: A high input on C/P̄ selects "C" port or command registers and a low input selects the "P" port or parameter registers.			
VCC	40	-	+5V Power supply.			
GND	20	-	Ground (0V)			



Functional Description

Data bus buffer

This three-state, bidirectional, 8-bit buffer is used to interface the SAB 8276 to the system data bus.

This functional block accepts inputs from the system control bus and generates control signals for overall device operation. It contains the command, parameter, and status registers that store various control formats for the device functional definition.

C/P	Operation	Register
0	Read	Reserved
0	Write	Parameter
1	Read	STATUS
1	Write	COMMAND

C/P	RD	WR	CS	BS	
0	0	1	0	1	Reserved
0	1	0	0	1	Write 8276 Parameter
1	0	1	0	1	Read 8276 Status
1	1	0	0	1	Write 8276 Command
X	1	0	1	0	Write 8276 Row Buffer
X	1	1	Х	Х	High Impedance
X	Х	Х	1	1	High Impedance

RD (Read)

A "low" on this input informs the SAB 8276 that the CPU is reading data or status information from the SAB 8276.

WR (Write)

A "low" on this input informs the SAB 8276 that the CPU is writing data or control words to the SAB 8276.

CS (Chip select)

A "low" on this input selects the SAB 8276. No reading or writing will occur unless the device is selected. When CS is high, the data bus in the float state and RD and WR will have no effect on the chip.

BRDY (BUFFER READY)

A "high" on this output indicates that the SAB 8276 is ready to receive character data.

BS (BUFFER SELECT)

A "low" on this input enables WR of character data to the SAB 8276 row buffers.

INT (Interrupt Output)

A "high" on this output informs the CPU that the SAB 8276 desires interrupt service.

Character counter

The character counter is a programmable counter that is used to determine the number of characters to be displayed per row and the length of the horizontal retrace interval. It is driven by the CCLK (character clock) input, which should be a derivative of the external dot clock.

Line counter

The line counter is a programmable counter that is used to determine the number of horizontal lines (sweeps) per character row. Its outputs are used to address the external character generator ROM.

Row counter

The row counter is a programmable counter that is used to determine the number of character rows to be displayed per frame and length of the vertical retrace interval.

Raster timing and video controls

The raster timing circuitry controls the timing of the HRTC (Horizontal Retrace) and VRTC (Vertical Retrace) outputs. The video control circuitry controls the generation of HGLT (highlight), RVV (reverse video), LTEN (Light enable), VSP (video suppress), and GPA0-1 (general purpose attribute) outputs.

Row buffers

The row buffers are two 80 character buffers. They are filled from the microcomputer system memory with the character codes to be displayed. While one row buffer is displaying a row of characters, the other is being filled with the next row of characters.

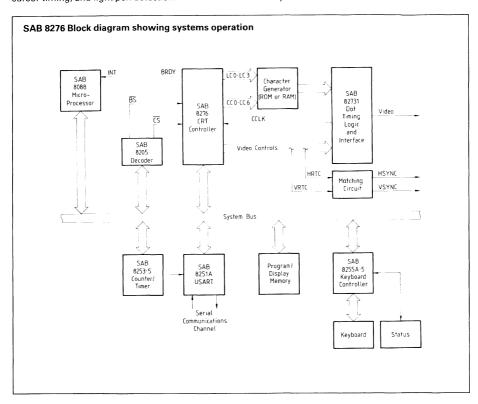
Buffer input/output controllers

The buffer input/output controllers decode the characters being placed in the row buffers. If the character is a character attribute, field attribute or special code, these controllers control the appropriate action (Examples: A "HIGHLIGHT" attribute will cause the Buffer Output Controller to activate the HGLT output).

System Operation

The SAB 8276 is programmable to a large number of different display formats. It provides raster timing, display row buffering, visual attribute decoding, cursor timing, and light pen detection.

It is designed to interface with standard character generator for dot matrix decoding. Dot level must be provided by external circuitry.



Raster timing

The character counter is driven by the character clock input (CCLK). It counts out the characters being displayed (programmable from 1 to 80). It then cause the line counter to increment, and it starts counting out the horizontal retrace (programmable from 2 to 32). This is constantly repeated.

The line counter is driven by the character counter. It is used to generate the line address outputs (LCO-3) for the character generator. After it counts all of the lines in a character row (programmable from 1 to 16), it increments the row counter, and starts over again. (See Character Format Section for detailed description of Line Counter functions.)

The row counter is an internal counter driven by the line counter. It controls the functions of the row buffers and counts the number of character rows displayed.

After the row counter counts all of the rows in a frame (programmable from 1 to 64), it starts counting out the vertical retrace interval (programmable from 1 to 4).

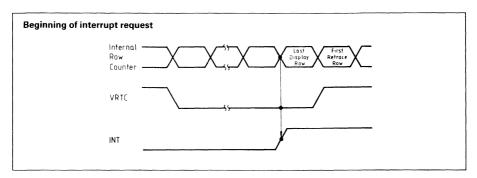
The video suppression output (VSP) is active during horizontal and vertical retrace intervals.

Dot level timing circuitry must synchronize these outputs with the video signal to the CRT display.

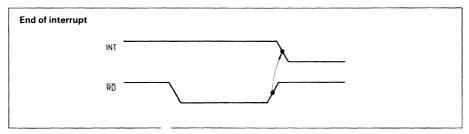
Interrupt timing

The SAB 8276 can be programmed to generate an interrupt request at the end of each frame.

If the SAB 8276 interrupt enable flag is set, an interrupt request will occur at the *beginning* of the *last display row*.



IRQ will go inactive after the status register is read.



A reset command will also cause IRQ to go inactive, but this is not recommended during normal service.

Note: Upon power-up, the SAB 8276 interrupt Enable Flag may be set. As a result, the user's cold start routine should write a reset command to the SAB 8276 before system interrupts are enabled.

General systems operational description

Display characters are retrieved from memory and displayed on a row by row basis. The SAB 8276 has two row buffers. While one row buffer is being used for display, the other is being filled with the nextrow of characters to be displayed. The number of display characters per row and the number of character rows per frame are software programmable, providing easy interface to most CRT displays (see programming section).

The SAB 8276 uses BRDY to request data to fill the row buffer that is not being used for display. The SAB 8276 displays character rows one line at a time. The number of lines per character row, the

underline position, and blanking of top and bottom lines are programmable (see programming section).

The SAB 8276 provides special control codes which can be used to minimize overhead. It also provides visual attribute codes to cause special action on the screen without the use of the character generator (see visual attribute section).

The SAB 8276 also controls raster timing. This is done by generating horizontal retrace (HRTC) and vertical retrace (VRTC) signals. The timing of these signals is programmable.

The SAB 8276 can generate a cursor. Cursor location and format are programmable (see programming section).

Display row buffering

Before the start of a frame, the SAB 8276 uses BRDY and BS to fill one row buffer with characters.

When the first horizontal sweep is started, character codes are output to the character generator from the row buffer just filled. Simultaneously, the other row buffer is filled with the next row of characters.

After all the lines of the character row are scanned, the roles of the two row buffers are reversed and the same procedure is followed for the next row.

This is repeated until all of the character rows are displayed.

Screen format

The SAB 8276 can be programmed to generate from 1 to 80 characters per row, and from 1 to 64 rows per frame.

The SAB 8276 can also be programmed to blank alternate rows. In this mode, the first row is displayed, the second blanked, the third displayed, etc. Display data is not requested for the blanked rows.

Row format

The SAB 8276 is designed to hold the line count stable while outputting the appropriate character codes during each horizontal sweep. The line count is incremented during horizontal retrace and the whole row of character codes are output again during the next sweep. This is continued until the whole character row is displayed.

The number of lines (horizontal sweeps) per character row is programmable from 1 to 16.

The output of the line counter can be programmed to be in one of two modes.

In mode 0, the output of the line *counter* is the same as the line *number*.

In mode 1, the line *counter* is offset by one from the line *number*

Note: In mode 1, while the *first* line (line number 0) is being displayed, the *last* count is output by line counter.

Mode 0 is useful for character generators that leave address zero blank and start at address 1, Mode 1 is useful for character generators which start at address zero.

Underline placement is also programmable (from line *number* 0 to 15). This is independent of the line *counter* mode.

If the line *number* of the underline is greater than 7 (line *number* MSB = 1), then the top and bottom lines will be blanked.

If the line *number* of the underline is less than or equal to 7 (line *number* MSB = 0), then the top and bottom lines will *not* be blanked.

If the line *number* underline is greater than the maximum number of lines, the underline will not appear.

Blanking is accomplished by the VSP (Video Suppression) signal. Underline is accomplished by the LTEN (light enable) signal.

Dot format

Dot width and character width are dependent upon the external timing and control circuitry.

Dot level timing circuitry should be designed to accept the parallel output of the character generator and shift it out serially at the rate required by the CRT display.

Dot width is a function of dot clock frequency.

Character width is a function of the character generator width.

Horizontal character spacing is a function of the shift register length.

Note: Video control and timing signals must be synchronized with the video signal due to the character generator access delay.

Visual Attributes and Special Codes

The characters processed by the SAB 8276 are 8-bit quantities. The character code outputs provide the character generator with 7 bits of address. The most significant bit is the extra bit and it is used to determine if it is a normal display character (MSB = 0), or if it is a Visual Attribute or Special Code (MSB = 1).

Special codes

Four special codes are available to help reduce memory, software or DMA overhead.

Special control character

MSB	LSB	
1 1 1 1	0 0 S S	
		SPECIAL CONTROL CODE

S	S	Function
0	0	End of Row End of Row-stop Buffer Loading
1	0	End of Screen
1	1	End of Screen-stop Buffer Loading

The end-of-row code (00) activates VSP and holds it to the end of the line.

The end-of-row Buffer Loading code (BRDY) causes the Buffer Loading control logic to stop Buffer Loading for the rest of the row when it is written into the row buffer. It affects the display in the same way as the end-of-row code (00).

The end-of-screen code (10) activates VSP and holds it to the end of the frame.

The end-of-screen-stop Buffer Loading code (BRDY) causes the Buffer Loading control logic to stop Buffer Loading for the rest of the frame when it is written into the row buffer. It affects the display in the same way as the end-of-screen code (10).

If the stop Buffer Loading feature is not used, all characters after an end-of-row character are ignored, except for the end-of-screen character, which operates normally. All characters after an end-of-screen character are ignored.

Note: If a stop Buffer Loading character is not the last character in a burst or row, Buffer Loading is not stopped until after the next character is read. In the situation, a dummy character must be placed in memory after the stop Buffer Loading character.

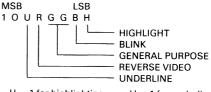
Field attributes

The field attributes are control codes which affect the visual characteristics for a field of characters, starting at the character following the code up to, and including, the character which precedes the *next* field attribute code, or up to the end of the frame. The field attributes are reset during the vertical retrace interval.

There are six field attributes:

- Blink Characters following the code are caused to blink by activating the Video Suppression Output (VSP). The blink frequency is equal to the screen refresh frequency divided by 32.
- Highlight Characters following the code are caused to be highlighted by activating the Highlight Output (HGLT).
- Reverse Video Characters following the code are caused to appear with reverse video by activating the Reverse Video Output (RVV).
- Underline Characters following the code are caused to be underlined by activating the Light Enable Output (LTEN).
- 5, 6. General Purpose There are two additional SAB 8276 outputs which act as general purpose, independently programmable field attributes. GPA0-1 are active high outputs.

Field attribute code



H = 1 for highlightingB = 1 for blinkingR = 1 for reverse video

U = 1 for underline GG = GPA1, GPA0

* More than one attribute can be enabled at the same time. If the blinking and reverse video attributes are enabled simultaneously, only the reversed characters will blink.

Cursor timing

The cursor location is determined by a cursor row register and a character position register which are located by command to the controller. The cursor can be programmed to appear on the display as:

- 1. a blinking underline
- 2. a blinking reverse video block
- 3. a non-blinking underline
- 4. a non-blinking reverse video block

The cursor blinking frequency is equal to the screen refresh frequency divided by 16.

If a non-blinking reverse video *cursor* appears in a non-blinking reverse video *field*, the cursor will appear as a normal video block.

If a non-blinking underline *cursor* appears in a non-blinking underline *field*, the cursor will not be visible.

Device programming

The SAB 8276 has two programming registers, the command register and the parameter register. It also has a status register. The command register can only be written into and the Status registers can only be read from. They are addressed as follows:

$\overline{A_0}$	operation	register
0	Read	Reserved
0	Write	Parameter
1	Read	Status
1	Write	Command

The SAB 8276 expects to receive a command and a sequence of 0 to 4 parameters, depending on the command. If the proper number of parameter bytes are not received before another command is given, a status flag is set, indicating an improper command.

Instruction Set

The SAB 8276 instruction set consists of 7 commands.

4
0
0
2
0
0
0

In addition, the status of the SAB 8276 can be read by the CPU at any time.

1 Reset command

						Е	ata	bus			
	Operation	C/P	Description	MS	SB ——					L	SB
Command	Write	1	Reset command	0	0	0	0	0	0	0	0
	Write	0	Screen comp Byte 1	s	Н	Н	Н	Н	Н	Н	Н
Parameters	Write	0	Screen comp Byte 2	V	V	R	R	R	R	R	R
	Write'	0	Screen comp Byte 3	U	U	U	U	L	L	L	L
	Write	0	Screen comp Byte 4	М	1	С	С	Z	Z	Z	Z

Action – After the reset command is written, BRDY goes inactive, SAB 8276 interrupts are disabled, and the VSP output is used to blank the screen. HRTC and VRTC continue to run. HRTC and VRTC timing are random on power-up. As parameters are written, the screen composition is defined.

Parameter - S Spaced rows

S	Functions
0	Normal rows
1	Spaced rows

Parameter-HHHHHHH Horizontal characters/row

Н	Н	Н	Н	Н	Н	Н	No. of characters per rov
0	0	0	0	0	0	0	1
0	0	0	0	0	0	1	2
0	0	0	0	0	1	0	3
1	0	0	1	1	1	1	80
1	0	1	0	0	0	0	Undefined
1	1	1	1	1	1	1	Undefined

R	R	R	R	R	R	No. of rows/frame
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
1	1	1	1	1	1	64

Parameter - RRRRRR Vertical rows/frame

Parameter - UUUU Underline placement

U	U	U	U	Line number of underline
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
1	1	1	1	16

Parameter - VV Vertical retrace row count

٧	V	No. of row counts per VRTC
0	0	1
0	1	2
1	0	3
1	1	4

Note: uuuu MSB determines blanking of top and bottom lines (1 = blanked, 0 = not blanked).

Parameter – LLLL Number of lines per character row

L	L	L	L	No. of lines/row
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
				•
1	1	1	1	16

Parameter - ZZZZ Horizontal retrace count

Z	Z	Z	Z	No. of character counts per HRTC
0	0	0	0	2
0	0		1	4
0	0	1	0	6
1	1	1	1	32

Parameter - M Line counter mode

M	Line counter mode
0	Mode 0 (non-offset)
1	Mode 1 (offset by 1 count)

Parameter - CC Cursor format

С	С	Cursor format
0	0	Blinking reverse video block
0	1	Blinking underline
1	0	Nonblinking reverse video block
1	1	Nonblinking underline

2 Start display command

					Data bus								
	Operation	C/P Description		M	SB					L	SB		
Command	Write	1	Start display	0	0	1	0	0	0	0	0		
No parameters													

Action – SAB 8276 interrupts are enabled, DMA requests begin, video is enabled, interrupt enable and video enable status flags are set.

3 Stop display command

					Data bus						
	Operation	C/P	Description	MS	SB					L	SB
Command	Write	1	Stop display	0	1	0	0	0	0	0	0
No parameters											

Action – Disables video, interrupts remain enabled. HRTC and VRTC continue to run, video enable status flag is reset, and the "Start display" command must be given to re-enable the display.

4 Load cursor position

					Data bus							
	Operation	C₽	Description	MSB	MSB			LS				
Command	Write	1	Load cursor	1 0 (0	0	0	0	0			
Parameters	Write	0	Char. number	(Char. p in row)	ositio	n						
	Write	0	Row number	(Row nu	(Row number)							

Action – The SAB 8276 is conditioned to place, the next two parameter bytes into the cursor position registers. Status flags not affected.

5 Enable interrupt command

				Data bus								
	Operation	C/P	Description	М	SB					L	SB	
Command	Write	1	Enable interrupt	1	0	1	0	0	0	0	0	
No parameters												

Action – The interrupt enable status flag is set and interrupts are enabled.

6 Disable interrupt command

	Operation	C/P	Description	!	ЛSВ					L	SB
Command	Write	1	Disable interrupt		1	0	0	0	0	0	0
No parameters											

Action – Interrupts are disabled and the interrupt enable status flag is reset.

7 Preset counters command

					Data bus					s		
	Operation	C/P	Description	M	SB					L	SB	
Command	Write	1	Preset counters	1	1	1	0	0	0	0	0	
No parameters												

Action – The internal timing counters are preset, corresponding to a screen display position at the top left corner. Two character clocks are required for this operation. The counters will remain in this state until any other command is given.

This command is useful for system debug and synchronization of clustered CRT displays on a single CPU. After this command, two additional clock cycles are required before the first character of the first row is put out.

Status flags

							Dat	ta b	us		
	Operation	C/P	Description	М	SB					L:	SB
Command	Read	1	Status word	0	ΙE	IR	Χ	IC	VE	BU	X

- IE (Interrupt Enable) Set or reset by command. It enables vertical retrace interrupt. It is automatically set by a "Start Display" command reset with the "Reset" command.
- IR (Interrupt Request) This flag is set at the beginning of display of the last row of the frame if the interrupt enable flag is set. It is reset after a status read operation.
- IC (Improper Command) This flag is set when a command parameter string is too long or too short. The flag is automatically reset after a status read.
- VE (Video Enable) This flag indicates that video operation of the CRT is enabled. This flag is set on a "Start Display" command, and reset on a "Stop Display" or "Reset" command.
- BU (Buffer Underrun) This flag is set whenever a Row Buffer is not filled with character data in time for buffer swap required by the display. Upon activation of this bit, buffer loading ceases, and the screen is blanked until after the vertical retrace interval.

SAB 8276

Absolute Maximum Ratings 1)

Temperature under bias 0 to $+70\,^{\circ}\mathrm{C}$ Storage temperature $-65\,$ to $+150\,^{\circ}\mathrm{C}$ All output ans supply and supply voltages $-0.5\,$ to $+7\,$ V All input voltages $-0.5\,$ to $+5.5\,$ V Power dissipation 1.0 W

D.C. Characteristics

 $(TA = 0 \text{ to } 70^{\circ}\text{C}, VCC = 5 \text{ V } \pm 5\%)$

Symbol	Davamatav	Limit values		I I - is	T		
	Parameter	Min.	Max.	Unit	Test condition		
VIL	Input low voltage	-0.5	0.8				
VIH	Input high voltage	2.0	VCC+0.5V	l _v			
VOL	Output low voltage	_	0.45	ľ	IOL = 2.2 mA		
VOH	Output high voltage	2.4	_		$IOH = -400 \mu A$		
IIL	Input load current		±10	uΑ	VIN = VCC to 0 V		
IOFL	Output float leakage	_	- 10	μΑ	VOUT = VCC to 0.45 V		
ICC	VCC supply current		160	mA	_		

Capacitance

 $(TA = 25^{\circ}C, VCC = GND = 0 V)$

Symbol	Parameter	Limit	values	Unit	Test condition	
		Min.	Max.	Offic		
CIN	Input capacitance	_	10	pF	fc = 1 MHz	
CI/O	I/O capacitance		20	pi	Unmeasured pins returned to GND	

Stresses above those listed under "absolute maximum ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

A.C. Characteristics (SAB 8276)

(TA = 0 to 70°C, VCC = $5.0 \text{ V} \pm 5\%$, GND = 0 V)

Clock timing

Symbol Parar	Parameter	Limit	values	Units	Test condition	
		Min.	Max.	Units		
TCLK	Clock period	480	30			
TKH	Clock high	240				
TKL	Clock low	160		ns	_	
TKR	Clock rise	5				
TKF	Clock fall]				

Bus parameters Read cycle

Symbol	Parameter	Limi	t values	Unit	Test condition	
		Min.	Max.			
TAR	Address stable before READ	0				
TRA	Address hold time for READ	1	_		_	
TRR	READ pulse width	250		ns		
TRD	Data delay from READ		200		CL = 150 pF	
TDF	READ to data floating	1	100		CL - 150 pr	

Write cycle

Symbol	Parameter	Lin	nit values	1.1	T		
	raiameter	Min.	Max.	Unit	Test condition		
TAW	Address stable before WRITE	0					
TWA	Address hold time for WRITE	U					
TWW	WRITE pulse width	250		ns	-		
TDW	Data setting time for WRITE	150					
TWD	Data hold time for WRITE	0					

Other timings

Symbol		Lin	Limit values		Test condition	
	Parameter	Min.	Max.	Unit	Test condition	
TCC	Character code output delay		150			
THR	Horizontal retrace output delay		200			
TLC	Line count output delay		400 275		CL = 50 pF	
TAT	Control-attribute output delay					
TVR	Vertical retrace output delay			ns		
TRI	INT↓ from RD↑		250			
TWQ	BRDY↑ from WR↑					
TRQ	BRDY↓ from WR↓		200			
TLR	BS↓ to WR↓	0	_		_	
TRL	WR↑ to BS↑	Ĭ				

A.C. Characteristics (SAB 8276-2)

 $(TA = 0 C \text{ to } 70^{\circ}\text{C}, VCC = 5.0 \text{ V} \pm 5\%, GND = 0 \text{ V})$

Clock timing

Symbol Parameter	Parameter	Li	mit values	111-14	Test condition
	rarameter	Min.	Max.	Unit	
TCLK	Clock period	320			
TKH	Clock high	120	_		_
TKL	Clock low	120		ns	
TKR	Clock rise	5	30	1	
TKF	Clock fall	5	30		

Bus parameters Read cycle

Symbol	Roramator	Lin	nit values	11-1-1	T4
	raiameter	Min.	Max.	Unit	Test condition
TAR	Address stable before READ	0			
TRA	Address hold time for READ	Ů.	-		-
TRR	READ pulse width	250		ns	
TRD	Data delay from READ		200		CL = 150 pF
TDF	READ to data floating		100	7	CL = 150 pr

Write cycle

Symbol	Parameter	Limit values		11-14	T	
	i didiletei	Min.	Max.	Unit	Test condition	
TAW	Address stable before WRITE	0				
TWA	Address hold time for WRITE	7				
TWW	WRITE pulse width	250]-	ns	_	
TDW	Data setting time for WRITE	150	1			
TWD	Data hold time for WRITE	0				

Other timings

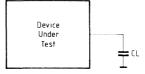
		Lim	nit values	Unit	Test condition	
Symbol	Parameter	Min.	Max.	Unit	Test condition	
TCC	Character code output delay		150			
THR	Horizontal retrace output delay		,00			
TLC	Line count output delay			ns		
TAT	Control-attribute output delay	_			CL = 50 pF	
TVR	Vertical retrace output delay		250	ns		
TRI	INT↓ from RD↑					
TWQ	BRDY↑ from WR↑					
TRQ	BRDY↓ from WR↓		200			
TLR	BS↑ to WR↓	0				
TRL	WR↑ to BS↑					

A.C. Testing input/output



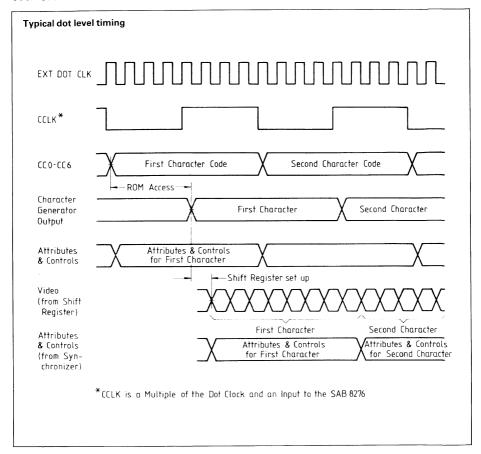
AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".

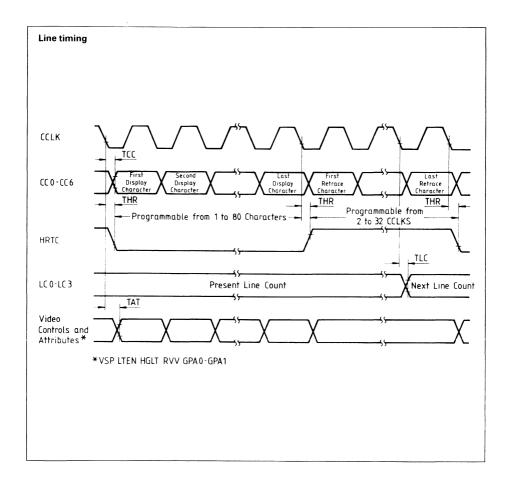
A.C. Testing load circuit

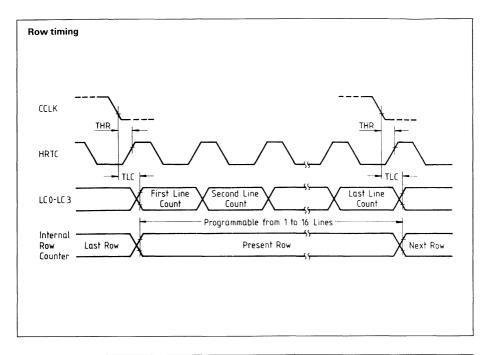


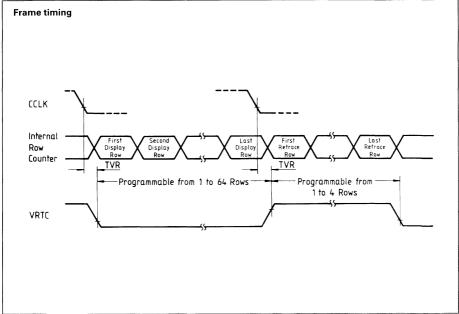
CL Includes Jig Capacitance

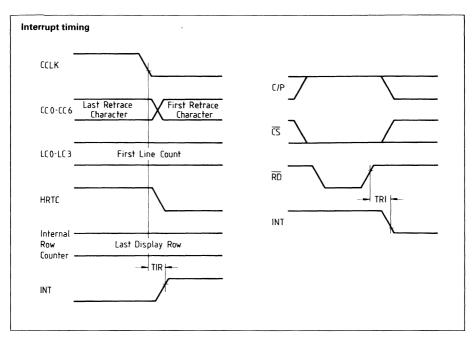
Waveforms

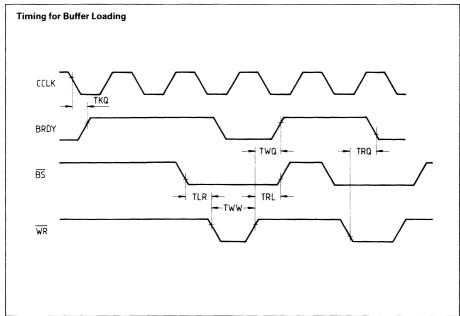


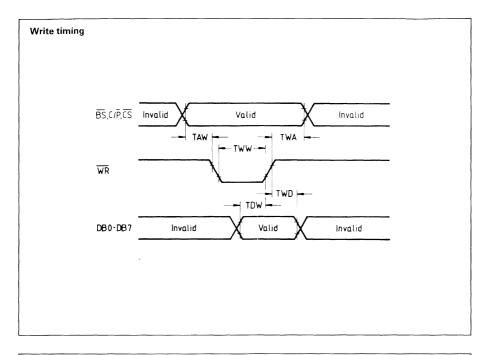


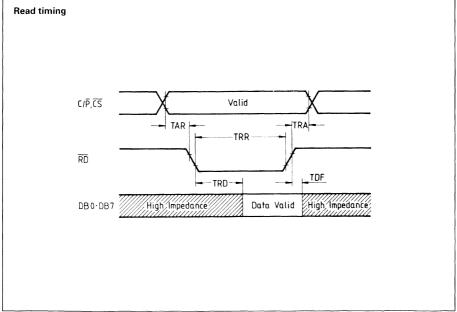


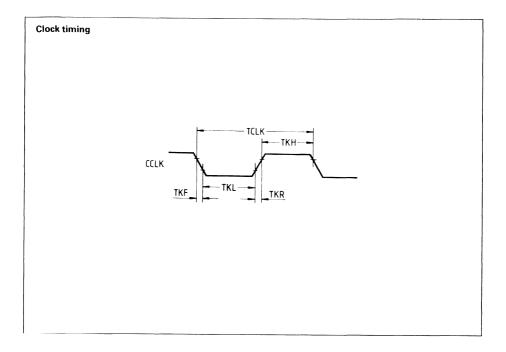




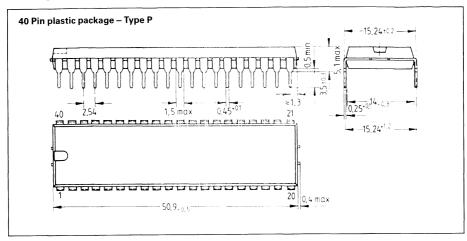








Package outline



Ordering Information

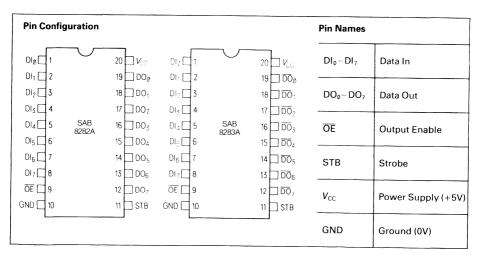
Туре	Description	Ordering code
SAB 8276-P	Small System CRT Controller, 2 MHz	Q67120-P83
SAB 8276-2-P	Small System CRT Controller, 3 MHz	Q67120-P93

Preliminary

SAB 8282A/SAB 8283A Octal Latch

- Fully compatible with SAB 8282/SAB 8283
- 40% Less Power Supply Current than Standard SAB 8282/SAB 8283
- Address Latch for SAB 80286, SAB 80186, SAB 8086, SAB 8085, SAB 8048 and SAB 8051 Families
- High Output Drive Capability for Driving System Data Bus

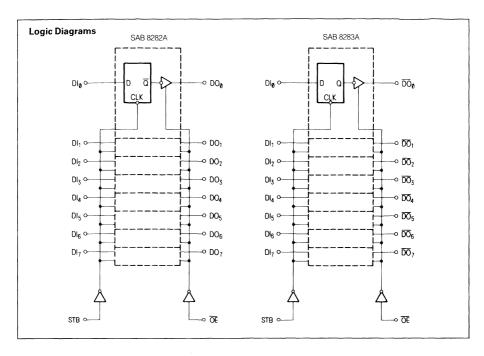
- Fully Parallel 8-Bit Data Register and Buffer
- No Output Low Noise when Entering or Leaving High Impedance State
- 3-State Outputs
- Transparent during Active Strobe
- 20-Pin Package



The SAB 8282A and SAB 8283A are 8-bit bipolar latches with 3-state output buffers. They can be used to implement latches, buffers, or multiplexers. The SAB 8283A inverts the input data at its outputs while the SAB 8282A does not.

Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with these devices.

This device is fabricated in a fast bipolar ASBC (Advanced Standard Buried Collector) process of Siemens.



Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function
STB	11	1	STROBE – STB is an input control pulse used to strobe data at the data input pins $(A_0 - A_7)$ into the data latches. This signal is active HIGH to admit input data. The data is latched at the HIGH to LOW transition of STB.
ŌĒ	9	I	OUTPUT ENABLE $-\overline{OE}$ is an input control signal which when active LOW enables the contents of the data latches onto the data output pin (DO_0-DO_7) or $\overline{DO_0}-\overline{DO_7}$). \overline{OE} being inactive HIGH forces the output buffers to their high impedance state.
DI ₀ -DI ₇	1-8	I	DATA INPUT PINS – Data presented at these pins satisfying setup time requirements when STB is strobed and latched into the data input latches.
DO ₀ -DO ₇ (SAB 8282A) DO ₀ -DO ₇ (SAB 8283A)	12-19	0	DATA OUTPUT PINS — When $\overline{\text{OE}}$ is true, the data in the data latches is presented as inverted (SAB 8283A) or non-inverted (SAB 8282A) data onto the data output pins.
V _{cc}	20	_	Power Supply (+5V)
GND	10	_	Ground (0V)

Functional Description

The SAB 8282A and SAB 8283A octal latches are 8-bit latches with 3-state output buffers. Data having satisfied the setup time requirements is latched into the data latches by strobing the STB line HIGH to LOW. Holding the STB line in its active HIGH state makes the latches appear transparent.

Data is presented to the data output pins by activating the \overline{OE} input line. When \overline{OE} is inactive HIGH the output buffers are in their high impedance state. Enabling or disabling the output buffers will not cause negative-going transients to appear on the data output bus.

Absolute Maximum Ratings¹⁾

Temperature Under Bias 0 to $+70^{\circ}$ C Storage Temperature -65 to $+150^{\circ}$ C All Output and Supply Voltages -0.5 to +7V All Input Voltages -1.0 to +5.5V Power Dissipation 1W

D. C. Characteristics

 $T_A = 0 \text{ to } 70^{\circ}\text{C}; V_{CC} = +5\text{V} \pm 10\%$

Cumbal	Donomotor.	Limi	t Values	11	T . O . IIII	
Symbol	Parameter	Min.	Max.	Units	Test Conditions	
V _C	Input Clamp Voltage		-1	V	$I_{\rm C} = -5 \mathrm{mA}$	
I _{cc}	Power Supply Current SAB 8282A SAB 8283A	-	100 90	mA	all outputs open	
I _F	Forward Input Current	-	-0.2		$V_{\rm F} = 0.45 {\rm V}$	
I_{R}	Reverse Input Current		50	μА	$V_{\rm R} = 5.25 \rm V$	
V _{OL}	Output LOW Voltage		0.45	1,,	I _{OL} = 32 mA	
V _{OH}	Output HIGH Voltage	2.4	-	7 V	$I_{OH} = -5 \text{ mA}$	
I _{OFF}	Output Off Current		±50	μА	$V_{\rm OFF} = 0.45 \text{ to } 5.25 \text{V}$	
V _{IL}	Input LOW Voltage		0.8			
V _{IH}	Input HIGH Voltage	2.0	-		$V_{\rm CC} = 5.0 {\rm V}^{2}$	
C _{IN}	Input Capacitance	-	12	pF	F = 1 MHz $V_{\text{BIAS}} = 2.5 \text{ V}, V_{\text{CC}} = 5 \text{ V}$ $T_{\text{A}} = 25^{\circ}\text{C}$	

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2) Output Loading:
$$I_{\rm OL}=32$$
 mA; $I_{\rm OH}=-5$ mA; $C_{\rm L}=300$ pF

A.C. Characteristics

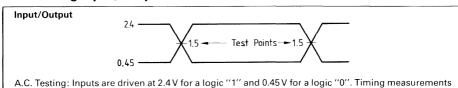
 $T_A = 0 \text{ to } +70^{\circ}\text{C}; V_{CC} = +5 \text{ V} \pm 10\%$

Loading

Outputs: $I_{OL} = 32 \text{ mA}$; $I_{OH} = -5 \text{ mA}$; $C_L = 300 \text{ pF}$

0 1 1	B	Limi	t Values	I I I mile -	T. 10 111	
Symbol	Parameter	Min.	Max.	Units	Test Conditions	
t _{IVOV}	Input to Output Delay —Inverting —Non-Inverting	5 5	22 30			
shov	STB to Output Delay -Inverting -Non-Inverting	10 10	40 45			
t _{EHOZ}	Output Disable Time	5	18		2)	
ELOV	Output Enable Time	10	30	ns		
Ivsl	Input to STB Setup Time	0				
SLIX	Input to STB Hold Time	25	_			
SHSL	STB HIGH Time	15				
ILIH, [†] OLOH	Input, Output Rise Time		20		From 0.8 to 2.0 V	
inil, tohol	Input, Output Fall Time		12	7	From 2.0 to 0.8 V	

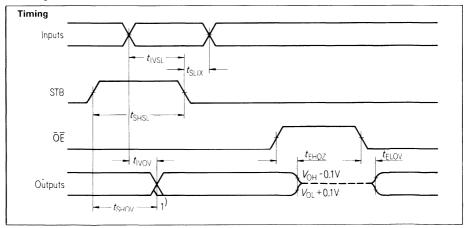
A.C. Testing Input, Output Waveform



are made at 1.5 V for both a logic "1" and "0".

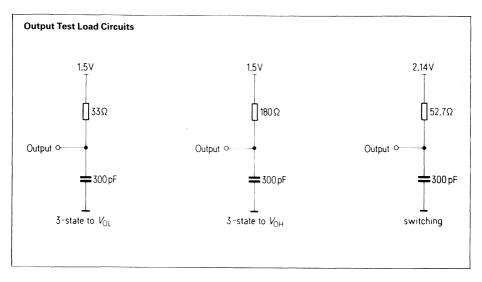
Waveforms

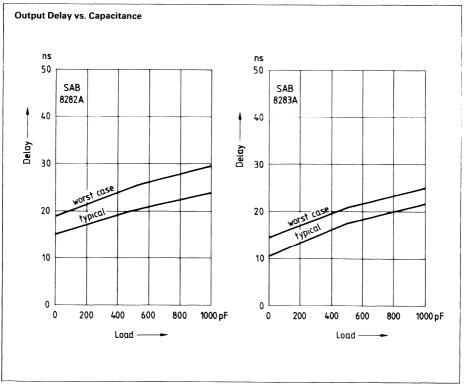
All timing measurements are made at 1.5 V unless otherwise noted.



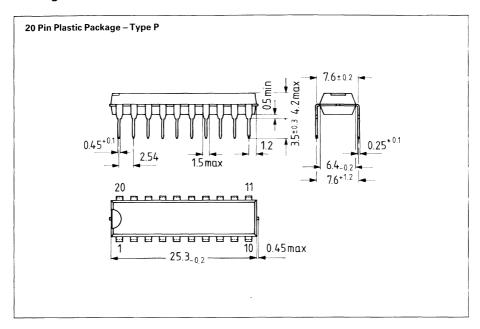
¹⁾ SAB 8283A Only – Output may be momentarily invalid following the high going STB transition.

2) See waveforms and test load circuit.





Package Outline



Ordering Information

Туре	Description	Ordering code
SAB 8282A – P	Octal Latch, non inverting (plastic)	Q 67020-Y149
SAB 8283A-P	Octal Latch, inverting (plastic)	Q 67020-Y150

P_{reliminary}

SAB 8284B, SAB 8284B-1 Clock Generator and Driver for SAB 8086 Family Processors

- Fully compatible with SAB 8284A, SAB 8284A-1
- 30% Less Power Supply Current than Standard SAB 8284A, SAB 8284A-1
- Generates the System clock for SAB 8086 and SAB 8088 Processors: upto 8 MHz with SAB 8284B upto 10 MHz with SAB 8284B-1
- · Uses a Crystal or a TTL Signal for Frequency Source upto 30 MHz

- Provides Synchronization for Synchronous and Asynchronous READY Signals
- 18-Pin Package
- Single +5V Power Supply
- Generates System Reset Output from Schmitt Trigger Input
- Capable of Clock Synchronization with Other SAB 8284Bs

Figure 1			Pin Names	
Pin Configuration			X ₁ X ₂	Connections for crystal
			F/C	Clock source select
	〜		EFI	External clock input
CYSNC 🗆 1		18 🗀 V _{CC}	CSYNC	Clock synchronization input
PCLK ☐ 2		17 🗀 X ₁	ASYNC	Ready synchronization select
ĀĒN₁ ☐ 3		16 X ₂	RDY ₁ RDY ₂	Ready signal
RDY₁ ☐ 4	SAB	15 ASYNC	AEN ₁ AEN ₂	Address enabled qualifiers for RDY _{1,2}
READY5	8284B	14 EFI	RES	Reset input
$RDY_2 \square 6$		13 🏻 F/C	RESET	Synchronized reset output
$\overline{AEN}_2 \square 7$		12 🗆 OSC	OSC	Oscillator output
CLK 🗆 8		11 RES	CLK	MOS Clock for the processor
GND ☐9		10 RESET	PCLK	TTL Clock for peripherals
			READY	Synchronized ready output
			V _{cc}	Power Supply (+5V)
			GND	Ground (OV)

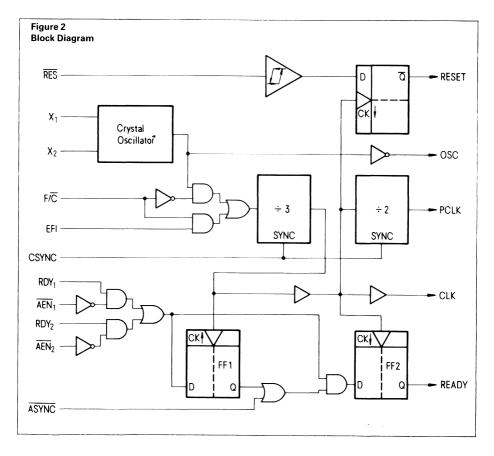
SAB 8284B is a bipolar clock generator/driver designed to provide clock signals for SAB 8086 and SAB 8088 processors and peripherals. It also contains READY logic for operation with two bus systems and provides the processors required

READY synchronization and timing. Reset logic with hysteresis and synchronization is also provided. This device is fabricated in a fast bipolar ASBC (Advanced Standard Buried Collector) process of Siemens.

Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function
AEN ₁ AEN ₂	3, 7	1	ADDRESS ENABLE. AEN is an active LOW signal. AEN serves to qualify its respective Bus Ready Signal (RDY, or RDY ₂). AEN, validates RDY, while AEN ₂ validates RDY ₂ . Two AEN signal inputs are useful in system configurations which permit the processor to access two Multi-Master System Busses. In non Multi-Master configurations the AEN signal inputs are tied true (LOW).
RDY ₁ , RDY ₂	4, 6	1	BUS READY (Transfer Complete). RDY is an active HIGH signal which is an indication from a device located on the system data bus that data has been received, or is available. RDY1 is qualified by AEN ₁ while RDY2 is qualified by AEN ₂ .
ASYNC	15	I	READY SYNCHRONIZATION SELECT. ASYNC is an input which defines the synchronization mode of the READY logic. When ASYNC is low, two stages of READY synchronization are provided. When ASYNC is left open or HIGH a single stage of READY synchronization is provided.
READY	5	0	READY. READY is an active HIGH signal which is the synchronized RDY signal input. READY is cleared after the guaranteed hold time to the processor has been met.
X ₁ , X ₂	16, 17	1	CRYSTAL IN. X_1 and X_2 are the pins to which a crystal is attached. The crystal frequency is 3 times the desired processor clock frequency.
F/C	13	I	FREQUENCY/CRYSTAL SELECT. F/\overline{C} is a strapping option. When strapped LOW, F/\overline{C} permits the processors clock to be generated by the crystal. When F/\overline{C} is strapped HIGH, CLK is generated from the EFI input.
EFI	14	I	EXTERNAL FREQUENCY IN. When F/\overline{C} is strapped HIGH, CLK is generated from the input frequency appearing on this pin. The input signal is a square wave 3 times the frequency of the desired CLK output.
CLK	8	0	PROCESSOR CLOCK. CLK is the clock output used by the processor and all devices which directly connect to the processor's local bus (i.e., the bipolar support chips and other MOS devices). CLK has an output frequency which is 1/3 of the crystal or EFI input frequency and a 1/3 duty cycle. An output HIGH of 4.5 volts ($V_{\rm CC}=5V$) is provided on this pin to drive MOS devices.
PCLK	2	0	PERIPHERAL CLOCK. PCLK is a TTL level peripheral clock signal whose output frequency is 1/2 that of CLK and has 50% duty cycle.
OSC	12	0	OSCILLATOR OUTPUT. OSC is the TTL level output of the internal oscillator circuitry. Its frequency is equal to that of the crystal.
RES	11	1	RESET IN. RES is an active LOW signal which is used to generate RESET. The SAB 8284B provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration.

Symbol	Number	Input (I) Output (O)	Function
RESET	10	0	RESET. RESET is an active HIGH signal which is used to reset the SAB 8086 family processors. Its timing characteristics are determined by RES.
CSYNC	1	I	CLOCK SYNCHRONIZATION. CSYNC is an active HIGH signal which allows multiple SAB 8284B to be synchronized to provide clocks that are in phase. When CSYNC is HIGH the internal counters are reset. When CSYNC goes LOW the internal counters are allowed to resume counting. CSYNC needs to be externally synchronized to EFI. When using the internal oscillator CSYNC should be hard-wired to ground.
$V_{\rm cc}$	18	-	Power Supply (+5V)
GND	9	-	Ground (OV)



Functional Description

General

The SAB 8284B is a single chip clock generator/driver for SAB 8086 and SAB 8088 processors. The chip contains a crystal-controlled oscillator, a divide-by-three counter, "Ready" synchronization and reset logic. Refer to Figure 2 for "Block Diagram" and Figure 1 for "Pin Configuration".

Oscillator

The oscillator circuit of the SAB 8284B is designed primarily for use with an external series resonant fundamental mode crystal from which the basic operating frequency is derived.

The crystal frequency should be selected at three times the required CPU clock. X1 and X2 are the two crystal input crystal connections. For the most stable operation of the oscillator (OSC) output circuit, two series resistors $(R_1=R_2=510\;\Omega)$ as shown in figure 7 are recommended. The output of the oscillator is buffered and brought out on OSC so that other system timing signals can be derived from this stable, crystal-controlled source.

It is advisable to limit stray capacitances to less than 10pF on X1 and X2 to minimize deviation from operating at the fundamental frequency.

Clock Generator

The clock generator consists of a synchronous divide-by-three counter with a special clear input that inhibits the counting. This clear input (CSYNC) allows the output clock to be synchronized with an external event (such as another SAB 8284B clock). It is necessary to synchronize the CSYNC input to the EFI clock external to the SAB 8284B. This is accomplished with two Schottky flip-flops (see figure 3). The counter output is a 33% duty cycle clock at one-third the input frequency.

The F/\overline{C} input is a strapping pin that selects either the crystal oscillator or the EFI input as the clock for the ± 3 counter. If the EFI input is selected as the clock source, the oscillator section can be used independently for another clock source. Output is taken from OSC.

Clock Outputs

The CLK output is a 33% duty cycle MOS clock driver designed to drive the SAB 8086 and SAB 8088 processors directly. PCLK is a TTL level peripheral clock signal whose output frequency is 1/2 that of CLK. PCLK has 50% duty cycle.

Reset Logic

The reset logic provides a Schmitt trigger input (RES) and a synchronizing flip-flop to generate the reset timing. The reset signal is synchronized to the falling edge of CLK. A simple RC network can be used to provide power-on reset by utilizing this function of the SAB 8284B. Waveforms for clocks and reset signals are illustrated in Figure 4.

READY Synchronization

Two READY inputs (RDY₁, RDY₂) are provided to accomodate two Multi-Master system busses. Each input has a qualifier ($\overline{AEN_1}$ and $\overline{AEN_2}$, respectively).

The AEN signals validate their respective RDY signals. If a Multi-Master system is not being used the AEN pin should be tied LOW.

Synchronization is required for all asynchronous active going edges of either RDY input to guarantee that the RDY setup and hold times are met. Inactivegoing edges of RDY in normally ready systems do not require synchronization but must satisfy RDY setup and hold as a matter of proper system design.

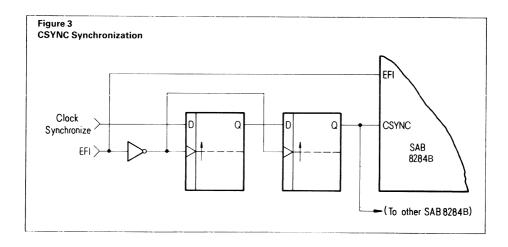
The ASYNC input defines two modes of READY synchronization operation.

When $\overline{\text{ASYNC}}$ is LOW, two stages of synchronization are provided for active READY input signals. Positive-going asynchronous READY inputs will first be synchronized to flip-flop one at the rising edge of CLK (requiring a setup time t_{RIVCH}) and then synchronized to flip-flop two at the next falling edge of CLK, after which time the READY

output will go active (HIGH). Negative-going asynchronous READY inputs will be synchronized directly to flip-flop two at the falling edge of CLK, after which time the READY output will go inactive. This mode of operation is intended for use by asynchronous (normally not ready) devices in the system which cannot be guaranteed by design to meet the required RDY setup timing, $t_{\rm RIVCL}$, on each bus cycle (Refer to Figure 5).

When ASYNC is high or left open, the first READY flip-flop is bypassed in the READY synchronization logic. READY inputs are synchronized by flip-flop two on the falling edge of CLK before they are presented to the processor. This mode is available for synchronous devices that can be guaranteed to meet the required RDY time (Refer to Figure 6).

ASYNC can be changed on every bus cycle to select the appropriate mode of synchronization for each device in the system.



SAB 8284B

Absolute maximum ratings 1)

Temperature Under Bias $0 \text{ to } 70^{\circ}\text{C}$ Storage Temperature $-65 \text{ to } 150^{\circ}\text{C}$ All Output and Supply Voltages -0.5 to 7 V All Input Voltages -1.0 to 5.5 V Power Dissipation 1 W

D.C. Characteristics

 $T_{\rm A} = 0 \text{ to } 70^{\circ} \text{C}; \ V_{\rm CC} = +5 \, \text{V} \pm 10\%$

Symbol	Parameter	Limit	Limit Values		T . O . III.
		Min.	Max.	Unit	Test Condition
I _F	Forward Input Current (ASYNC) Other Inputs		-1.3 -0.5	mA	$V_F = 0.45 \text{ V}$ $V_F = 0.45 \text{ V}$
I _R	Reverse Input Current (ASYNC) Other Inputs	_	50 50	μΑ	$V_{R} = V_{CC}$ $V_{R} = 5.25 \text{ V}$
V _C	Input Forward Clamp Voltage		-1.0	V	$I_{\rm C} = -5 \rm mA$
I _{CC}	Power Supply Current		110	mA	All outputs open
V _{IL}	Input LOW Voltage		0.8		
V _{IH}	Input HIGH Voltage	2.0			_
V_{IHR}	Reset Input HIGH Voltage	2.6			
VoL	Output LOW Voltage	_	0.45	V	5 mA
V _{OH}	Output HIGH Voltage CLK Other Outputs	4 2.4	_		-1 mA -1 mA
$V_{IHR} - V_{ILR}$	RES Input Hysteresis	0.25	7		-

¹⁾ Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

A.C. Characteristics

 $T_A = 0 \text{ to } +70^{\circ}\text{C}; V_{CC} = +5 \text{ V} \pm 10\%$

Timing Requirements

Symbol	Parameter	Limit Values		Unit	T Cdisi
		Min.	Max.	Unit	Test Condition
t _{EHEL}	External Frequency HIGH Time	13			90%-90% V _{IN}
t _{ELEH}	External Frequency LOW Time	7 '3	-	ns	10% - 10% V _{IN}
ELEL	EFI Period	$t_{EHEL} + t_{ELEH} + \delta$			3)
	XTAL Frequency	12	25 ⁷)	MHz	-
RIVCL	RDY ₁ , RDY ₂ Active Setup to CLK				ASYNC = HIGH
t _{R1VCH}	RDY ₁ , RDY ₂ Active Setup to CLK	35			ASYNC = LOW
t _{R1VCL}	RDY ₁ , RDY ₂ Inactive Setup to CLK				
t _{CLR1X}	RDY ₁ , RDY ₂ Hold to CLK	0			
t _{AYVCL}	ASYNC Setup to CLK	50			
CLAYX	ASYNC Hold to CLK	0	1		
t _{A1VR1V}	AEN ₁ , AEN ₂ Setup to RDY ₁ , RDY ₂	15]-	ns	-
CLA1X	ĀĒN₁, ĀĒN₂ Hold to CLK	0			
t _{YHEH}	CSYNC Setup to EFI	20			
t _{EHYL}	CSYNC Hold to EFI	10			
YHYL	CSYNC Width	2 · t _{ELEL}			
t _{I1HCL}	RES Setup to CLK	65			4)
СП1Н	RES Hold to CLK	20			,
t _{ILIH}	Input Rise Time		20		From 0.8 V to 2.0 V
t _{iHIL}	Input Fall Time	7	12		From 2.0 V to 0.8 V

Notes see next page.

SAB 8284B

Timing Responses

Symbol	Parameter	Limit Values			T . 0
		Min.	Max.	Unit	Test Condition
t_{CLCL}	CLK Cycle Period	100			-
t _{CHCL}	CLK HIGH Time	1)	-		Fig. 7 & Fig. 8
t _{CLCH}	CLK LOW Time	2)			Fig. 7 & Fig. 8
t _{CH1CH2} t _{CL2CL1}	CLK Rise or Fall Time	_	10		1.0 V to 3.5 V
t _{PHPL}	PCLK HIGH Time	t _{CLCL} -20			
t _{PLPH}	PCLK LOW Time	t _{CLCL} -20	_		
t _{RYLCL}	Ready Inactive to CLK ⁶)	-8		ns	Fig. 9 & Fig. 10
t _{RYHCH}	Ready Active to CLK 5)	2)			Fig. 9 & Fig. 10
t _{CLIL}	CLK to Reset Delay		40		
t _{CLPH}	CLK to PCLK HIGH Delay	-			
t _{CLPL}	CLK to PCLK LOW Delay		22		_
t _{OLCH}	OSC to CLK HIGH Delay	-5		-	
t _{OLCL}	OSC to CLK LOW Delay	2	35		
t _{OLOH}	Output Rise Time (except CLK)	_	20		From 0.8 V to 2.0 V
t_{OHOL}	Output Fall Time (except CLK)		12		From 2.0 V to 0.8 V

¹) $(1/3 t_{CLCL})$ +2 for CLK Freq. \leq 8 MHz $(1/3 t_{CLCL})$ +6 for CLK Freq. = 10 MHz

²) $(2/3 t_{CLCL}) - 15$ for CLK Freq. ≤ 8 MHz $(2/3 t_{CLCL}) - 14$ for CLK Freq. = 10 MHZ

³⁾ $\delta = \text{EFI rise (5 ns max)} + \text{EFI fall (5 ns max)}.$

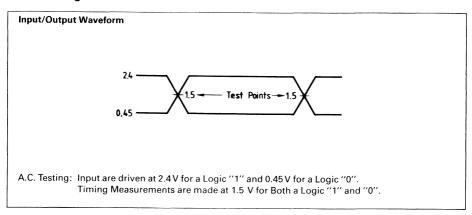
⁴) Setup and hold necessary only to guarantee recognition at next clock.

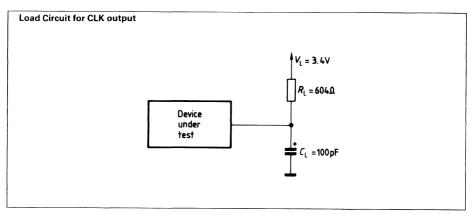
⁵) Applies only to T₃ and T_w states.

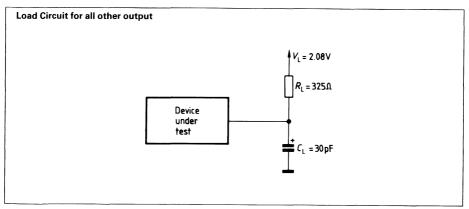
⁶⁾ Applies only to T₂ states.

^{7) 30} MHz for SAB 8284B-1

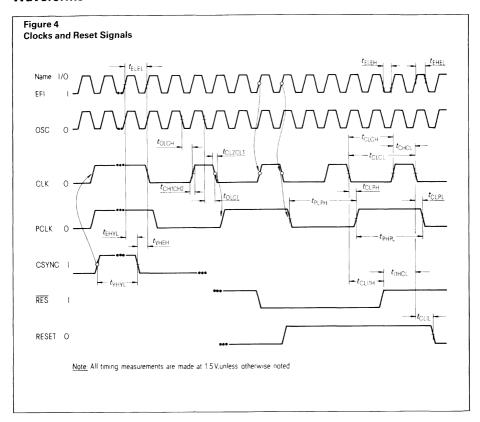
A.C. Testing

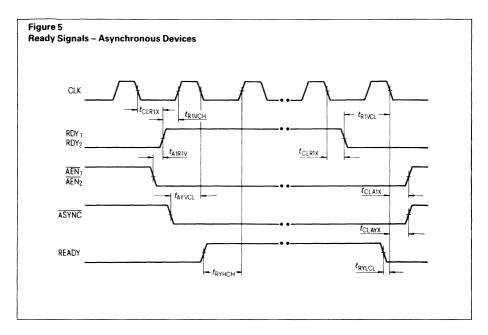


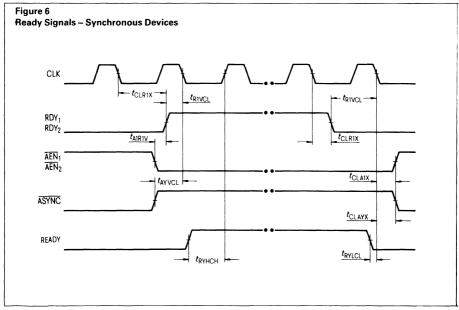




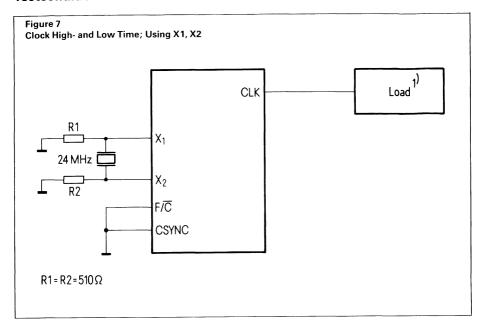
Waveforms

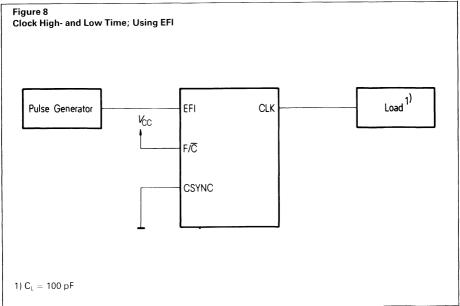


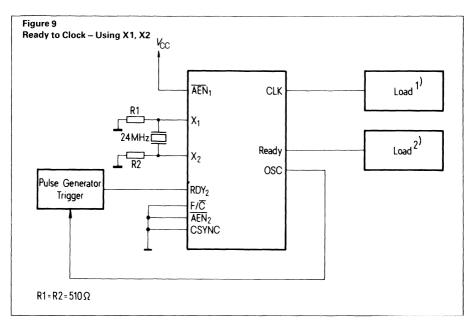


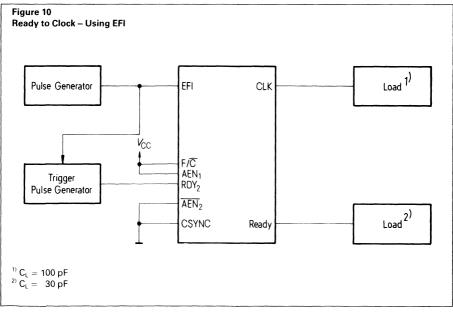


Testconditions

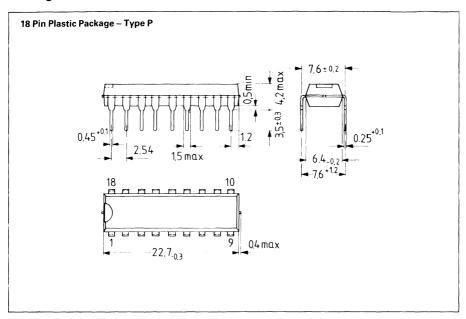








Package Outline



Ordering Information

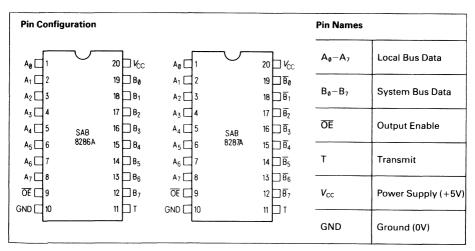
Component	Description	Ordering Code
	Clock Generator- (Plastic Package)	
SAB 8284B – P	upto 8 MHz	Q67020-Y151
SAB 8284B-1 – P	upto 10 MHz	Q67020-Y152

Preliminary

SAB 8286A/SAB 8287A Octal Bus Transceiver

- Fully compatible with SAB 8286/SAB 8287
- 40% Less Power Supply Current than Standard SAB 8286/SAB 8287
- Data Bus Buffer Driver for SAB 80286, SAB 80186, SAB 8086, SAB 8085, SAB 8048 and SAB 8051 Families
- High Output Drive Capability for Driving System Data Bus

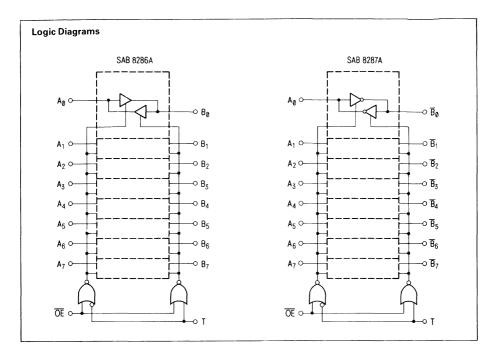
- Fully Parallel 8-Bit Transceivers
- 3-State Outputs
- 20-Pin Package
- No Output Low Noise when Entering or Leaving High Impedance State



The SAB 8286A and SAB 8287A are 8-bit bipolar transceivers with 3-state outputs. The SAB 8287A inverts the input data at its outputs while the SAB 8286A does not. Thus, a wide variety of applications for

buffering in microcomputer systems can be met. This device is fabricated in a fast bipolar ASBC (Advanced Standard Buried Collector) process of Siemens.

1.85



Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function
T	11	I	TRANSMIT – T is an input control signal used to control the direction of the transceivers. When HIGH, it configures the transceiver's B_0-B_7 as outputs with A_0-A_7 as inputs. T LOW configures $A_{\theta-7}$ as the outputs with B_0-B_7 serving as the inputs.
ŌĒ	9	I	OUTPUT ENABLE $ \overline{OE}$ is an input control signal used to enable the appropriate output driver (as selected by T) onto its respective bus. This signal is active LOW.
A ₀ -A ₇	1-8	I/O	LOCAL BUS DATA PINS – These pins serve to either present data to or accept data from the processor's local bus depending upon the state of the T pin.
B ₀ -B ₇ (SAB 8286A) B ₀ -B ₇ (SAB 8287A)	12-19	1/0	SYSTEM BUS DATA PINS – These pins serve to either present data to or accept data from the system bus depending upon the state of the T pin.
V _{cc}	20	-	Power Supply (+5V)
GND	10	-	Ground (0V)

Functional Description

The SAB 8286A and SAB 8287A transceivers are 8-bit transceivers with high impedance outputs. With T active HIGH and \overline{OE} active LOW, data at the A_0-A_7 pins is driven onto the B_0-B_7 pins.

With T inactive LOW and \overline{OE} active LOW, data at the B₀-B₇ pins is driven onto the A₀-A₇ pins. No output low glitching will occur whenever the transceivers are entering or leaving the high impedance state.

Absolute Maximum Ratings¹⁾

Temperature Under Bias Storage Temperature All Output and Supply Voltages All Input Voltages Power Dissipation 0 to +70°C -65 to +150°C -0.5 to +7 V -1.0 to +5.5 V 1 W

D. C. Characteristics

 $T_{\rm A} = 0 \text{ to } 70^{\circ}\text{C}; V_{\rm CC} = +5\text{V} \pm 10\%$

Symbol	Parameter	Limit Values		1	T . O . I'
		Min.	Max.	Unit	Test Condition
V _C	Input Clamp Voltage		- 1	V	$I_{\rm C} = -5 \mathrm{mA}$
I _{cc}	Power Supply Current	7	90	mA	All outputs open
I _F	Forward Input Current		-0.2	7 ''''	$V_{\rm F} = 0.45 \rm V$
I _R	Reverse Input Current		50	μА	$V_{R} = 5.25V$
V _{OL}	Output LOW Voltage – B Outputs – A Outputs		0.45 0.45	v	$I_{OL} = 32 \text{ mA}$ $I_{OL} = 16 \text{ mA}$
V _{OH}	Output HIGH Voltage – B Outputs – A Outputs	2.4	-		$I_{OH} = -5 \text{ mA}$ $I_{OH} = -1 \text{ mA}$
I _{OFF}	Output Off Current Output Off Current		I _F	-	$V_{OFF} = 0.45V$ $V_{OFF} = 5.25V$
V _{IL}	Input LOW Voltage – A Side – B Side		0.8 0.9	V	$V_{CC} = 5.0V$, See Note 2 $V_{CC} = 5.0V$, See Note 2
V _{IH}	Input HIGH Voltage	2.0		1	$V_{\rm CC} = 5.0$ V, See Note 2
C _{IN}	Input Capacitance	_	12	pF	F = 1 MHz $V_{\text{BIAS}} = 2.5 \text{V}, V_{\text{CC}} = 5 \text{V}$ $T_{\text{A}} = 25^{\circ} \text{C}$

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

²⁾ B Outputs: $I_{OL} = 32 \text{ mA}$; $I_{OH} = -5 \text{ mA}$; $C_L = 300 \text{ pF}$ A Outputs: $I_{OL} = 16 \text{ mA}$; $I_{OH} = -1 \text{ mA}$; $C_L = 100 \text{ pF}$

A.C. Characteristics

 $T_A = 0 \text{ to } +70^{\circ}\text{C}$; $V_{CC} = +5 \text{ V} \pm 10\%$

Loading

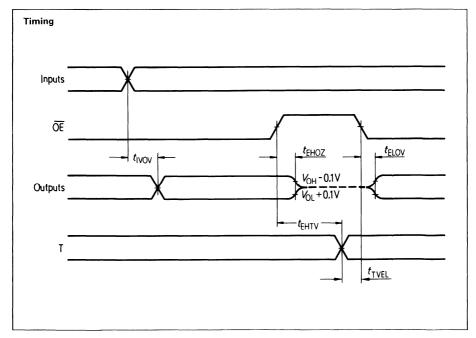
B Outputs: $I_{OL} = 32 \text{ mA}$; $I_{OH} = -5 \text{ mA}$; $C_L = 300 \text{ pF}$ A Outputs: $I_{OL} = 16 \text{ mA}$; $I_{OH} = -1 \text{ mA}$; $C_L = 100 \text{ pF}$

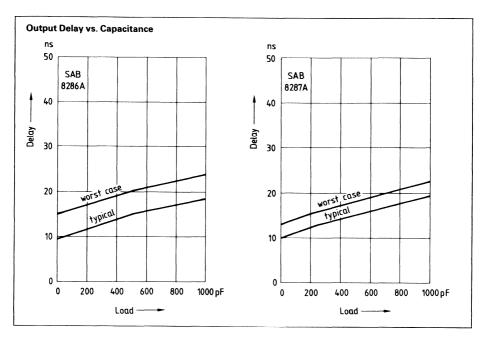
Symbol	Parameter	Limit Values			T O
		Min.	Max.	Unit	Test Condition
t _{IVOV}	Input to Output Delay Inverting Non-Inverting	5 5	22 30	ns	1)
t_{EHTV}	Transmit/Receive Hold Time	5			
t _{TVEL}	Transmit/Receive Setup	10			
t_{EHOZ}	Output Disable Time	5	18		
t_{ELOV}	Output Enable Time	10	30		
$t_{\rm ILIH}$, $t_{\rm OLOH}$	Input, Output Rise Time		20		From 0.8 to 2.0 V
$t_{\text{IHIL}}, t_{\text{OHOL}}$	Input, Output Fall Time		12		From 2.0 to 0.8 V

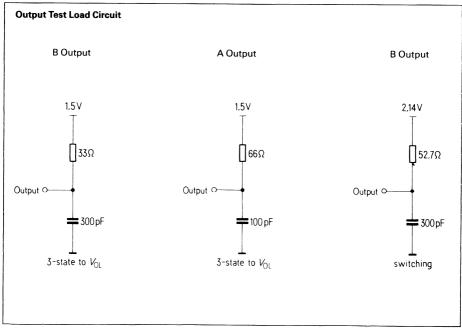
¹⁾ See waveforms and test load circuit.

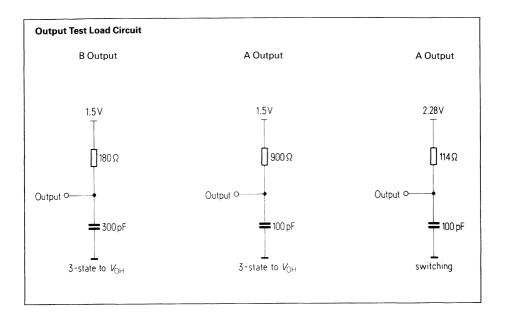
Waveforms

All timing measurements are made at 1.5 V unless otherwise noted.

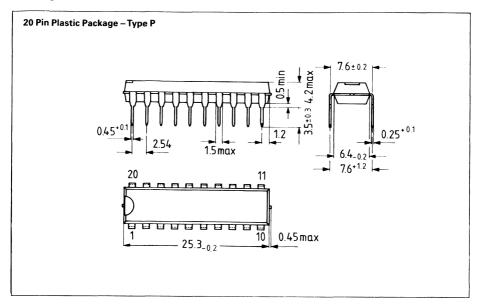








Package Outline



SAB 8286A / SAB 8287A

Ordering Information

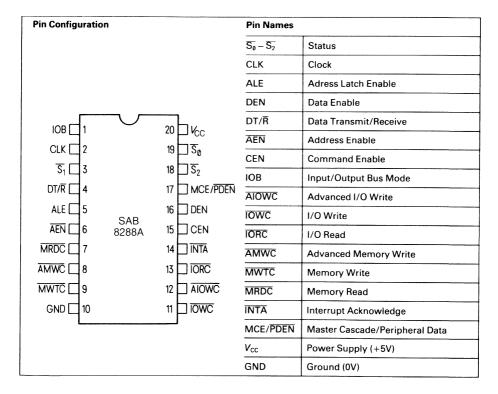
Туре	Description	Ordering code
SAB 8286A-P	Octal Bus Transceiver, non inverting (plastic)	Q 67020-Y 153
SAB 8287A-P	Octal Bus Transceiver, inverting (plastic)	Q 67020-Y 154



SAB 8288A Bus Controller for SAB 8086 Family Processors

- Fully compatible with SAB 8288
- 40% Less Power Supply Current than Standard SAB 8288
- Bipolar Drive Capability
- Provides Advanced Commands

- Provides Wide Flexibility in System Configurations
- 3-State Command Output Drivers
- Configurable for Use with an I/O Bus
- Facilitates Interface to One or Two Multi-Master Busses

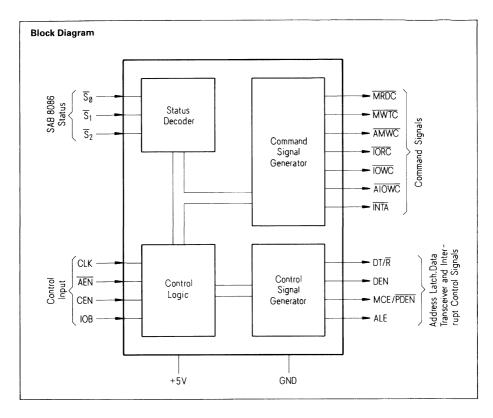


SAB 8288A Bus Controller is a 20-pin bipolar component for use with medium-to-large SAB 80186, SAB 80188, SAB 8086 and SAB 8088 processing systems. The bus controller provides command and control timing generation as well as bipolar bus drive capability while optimizing system performance.

A strapping option on the bus controller configures it for use with a multi-master system bus and separate I/O bus.

This device is fabricated in a fast bipolar ASBC (Advanced Standard Buried Collector) process of Siemens.

1.85



Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function
IOB	1	I	INPUT/OUTPUT BUS MODE – When the IOB is strapped HIGH the SAB 8288A functions in the I/O Bus mode. When it is strapped LOW, the SAB 8288A functions in the System Bus mode. (See sections on I/O Bus and Systems Bus modes).
CLK	2	1	CLOCK – This is a clock signal from the SAB 8284A or SAB 8284B clock generator and serves to establish when command and control signals are generated.
$\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$	3, 18, 19	I	STATUS INPUT PINS – These pins are the status input pins from the SAB 80186, SAB 80188, SAB 8086 or SAB 8088 processors. The SAB 8288A decodes these inputs to generate command and control signals at the appropriate time. When these pins are not in use (passive) they are all HIGH. (See chart under Functional Description).

Symbol	Number	Input (I) Output (O)	Function	
DT/R	4	0	DATA TRANSMIT/RECEIVE – This signal establishes the direction of data flow through the transceivers. A HIGH on this line indicates Transmit (write to I/O or memory) and a LOW indicates Receive (Read).	
ALE	5	0	ADDRESS LATCH ENABLE – This signal serves to strol an address into the address latches. This signal is activ HIGH and latching occurs on the falling (HIGH to LOW transition. ALE is intended for use with transparent D type latches.	
AEN	6		ADDRESS ENABLE – ĀĒN enables command outputs the SAB 8288A Bus Controller at least 105 ns after it becomes active (LOW). ĀĒN going inactive immediate 3-states the command output drivers. ĀĒN does not af the I/O command lines if the SAB 8288A is in the I/O B mode (IOB tied HIGH).	
MRDC	7	0	MEMORY READ COMMAND – This command line instructs the memory to drive its data onto the data b This signal is active LOW.	
AMWC	8	0	ADVANCED MEMORY WRITE COMMAND – The AMW issues a memory write command earlier in the machin cycle to give memory devices an early indication of a winstruction. Its timing is the same as a read command signal. AMWC is active LOW.	
MWTC	9	0	MEMORY WRITE COMMAND – This command line instructs the memory to record the data present on the data bus. This signal is active LOW.	
IOWC	11	0	I/O WRITE COMMAND – This command line instructs an I/O device to read the data on the data bus. This signal is active LOW.	
AIOWC	12	0	ADVANCED I/O WRITE COMMAND – The Alowc issues an I/O Write Command earlier in the machine cycle to give I/O devices an early indication of a write instruction. Its timing is the same as a read command signal. Alowc is active LOW.	
IORC	13	0	I/O READ COMMAND – This command line instructs an I/O device to drive its data onto the data bus. This signal is active LOW.	
INTA	14	0	INTERRUPT ACKNOWLEDGE – This command line tells a interrupting device that its interrupt has been acknowledge and that it should drive vectoring information onto the data bus. This signal is active LOW.	
CEN	15	I	COMMAND ENABLE – When this signal is LOW all SAB 8288A command outputs and the DEN and PDEN control outputs are forced to their inactive state. When this signal is HIGH, these same outputs are enabled.	
DEN	16	0	DATA ENABLE – This signal serves to enable data transceivers onto either the local or system data bus. This signal is active HIGH.	

Pin	Definitions	and Fu	unctions	(continued)
ГШ	Dellillillons	anuı	4116CHOH5 1	(COHUHUCU)

Symbol	Number	Input (I) Output (O)	Function		
MCE/PDEN	17	0	This is a dual function pin: MCE (IOB is tied LOW) – Master Cascade Enable occurs during an interrupt sequence and serves to read a Cascade. Address from a master PIC (Priority Interrupt Controller) onto the data bus. The MCE signal is active HIGH. PDEN (IOB is tied HIGH) – Peripheral Data Enable enables the data bus transceiver for the I/O bus during I/O instructions. It performs the same function for the I/O bus that DEN performs for the system bus. PDEN is active LOW.		
V _{cc}	20	_	Power Supply (+5V)		
GND	10	-	Ground (0V)		

Functional Description

The command logic decodes the three SAB 80186, SAB 80188, SAB 8086 or SAB 8088 CPU status lines $(\overline{S_0}, \overline{S_1}, \overline{S_2})$ to determine what command is to be issued. This chart shows the meaning of each status "word".

S2	\$ 1	SØ	Processor State	SAB 8288A Command
Ø	Ø	Ø	Interrupt Acknowledge	INTA
0	Ø	1	Read I/O Port	IORC
Ø	1	Ø	Write I/O Port	IOWC, AIOWC
Ø	1	1	Halt	None
1	Ø	Ø	Code Access	MRDC
1	Ø	1	Read Memory	MRDC
1	1	Ø	Write Memory	MWTC, AMWC
1	1	1	Passive	None

The command is issued in one of two ways dependent on the mode of the SAB 8288A Bus Controller.

I/O Bus Mode – The SAB 8288A is in the I/O Bus mode if the IOB pin is strapped HIGH. In the I/O Bus mode all I/O command lines (IORC, IOWC, AIOWC, INTA) are always enabled (i.e., not dependent on AEN). When an I/O command is initiated by the processor, the SAB 8288A immediately activates the command lines using PDEN and DT/R to control the I/O bus transceiver. The I/O command lines should not be used to control the system bus in this configuration because no arbitration is present. This mode allows one SAB 8288A Bus Controller to handle two external busses. No waiting is involved

when the CPU wants to gain access to the I/O bus. Normal memory access requires a "Bus Ready" signal (AEN LOW) before it will proceed. It is advantageous to use the IOB mode if I/O or peripherals dedicated to one processor exist in a multi-processor system.

System Bus Mode – The SAB 8288A is in the System Bus mode if the IOB pin is strapped LOW. In this mode no command is issued until 115 ns after the AEN Line is activated (LOW). This mode assumes bus arbitration logic will inform the bus controller (on the AEN line) when the bus is free for use. Both memory and I/O commands wait for bus arbitration. This mode is used when only one bus exists. Here, both I/O and memory are shared by more than one processor.

Command Outputs

The advanced write commands are made available to initiate write procedures early in the machine cycle. This signal can be used to prevent the processor from entering an unnecessary wait state.

The command output are:

MRDC - Memory Read Command

MWTC - Memory Write Command
IORC - I/O Read Command

IOWC - I/O Write Command

AMWC - Advanced Memory Write Command

AIOWC - Advanced I/O Write Command

INTA - Interrupt Acknowledge

INTA (Interrupt Acknowledge) acts as an I/O read during an interrupt cycle. Its purpose is to inform an interrupting device that its interrupt is being acknowledged and that it should place vectoring information onto the data bus.

Control Outputs

The control outputs of the SAB 8288A are Data Enable (DEN), Data Transmit/Receive (DT/ \overline{R}) and Master Cascade Enable/Peripheral Data Enable (MCE/ \overline{PDEN}). The DEN signal determines when the external bus should be enable onto the local bus and the DT/ \overline{R} determines the direction of data transfer. These two signals usually go to the chip select and direction pins of a transceiver.

The MCE/PDEN pin changes function with the two modes of the SAB 8288A. When the SAB 8288A is in the IOB mode (IOB HIGH) the PDEN signal serves as a dedicated data enable signal for the I/O or Peripheral System bus.

Interrupt Acknowledge and MCE

The MCE signal is used during an interrupt acknowledge cycle if the SAB 8288A is in the System Bus mode (IOB LOW). During any interrupt sequence there are two interrupt acknowledge cycle no data or address transfers take place. Logic should be provided to mask off MCE during this cycle. Just before the second cycle begins the MCE signal gates a master Priority Interrupt Controller's (PIC) cascade address onto the processor's local bus where ALE (Address Latch Enable) strobes it into the address latches. On the leading edge of the second interrupt cycle the addressed slave PIC gates an interrupt vector onto the system data bus where it is read by the processor.

If the system contains only one PIC, the MCE signal is not used. In this case the second Interrupt Acknowledge signal gates the interrupt vector onto the processor bus.

Address Latch Enable and Halt

Address Latch Enable (ALE) occurs during each machine cycle and serves to strobe the current address into the address latches. ALE also serves to strobe the status $(\overline{S_0}, \overline{S_1}, \overline{S_2})$ into a latch for halt state decoding.

Command Enable

The Command Enable (CEN) input acts as a command qualifier for the SAB 8288A. If the CEN pin is high the SAB 8288A functions normally. If the CEN pin is pulled LOW, all command lines are held in their inactive state (not 3-state). This feature can be used to implement memory partitioning and to eliminate address conflicts between system bus devices and resident bus devices.

Absolute Maximum Ratings 1)

Temperature Under Bias $0 \text{ to } + 70^{\circ}\text{C}$ Storage Temperature $-65 \text{ to } + 150^{\circ}\text{C}$ All Output and Supply Voltages -0.5 to + 7VAll Input Voltages -1.0 to + 5.5 VPower Dissipation 1W

D.C. Characteristics

 $T_{\rm A} = 0 \text{ to } 70^{\circ} \text{C}; V_{\rm CC} = +5 \, \text{V} \pm 10\%$

0 1 1	D	Limi	t Values	Units	T C I'm
Symbol	Parameter	Min.	Max.	Units	Test Conditions
$V_{\rm C}$	Input Clamp Voltage		-1	V	$I_{\rm C} = -5 {\rm mA}$
$I_{\rm CC}$	Power Supply Current		140	mA	All outputs open
I _F	Forward Input Current	-	-0.7] '''	$V_{\rm F} = 0.45 {\rm V}$
I _R	Reserve Input Current		50	μА	$V_{\rm R} = V_{\rm CC}$
V _{OL}	Output Low Voltage Command Outputs Control Outputs		0.5 0.5		I _{OL} = 32 mA I _{OL} = 16 mA
V _{OH}	Output High Voltage Command Outputs Control Outputs	2.4 2.4	-	V	$I_{OH} = -5 \text{ mA}$ $I_{OH} = -1 \text{ mA}$
V _{IL}	Input Low Voltage	<u> </u>	0.8		_
V _{IH}	Input High Voltage	2.0	_		
I_{OFF}	Output Off Current	-	100	μА	$V_{\rm OFF} = 0.4 \text{ to } 5.25 \text{ V}$

A.C. Characteristics

 $T_A = 0 \text{ to } 70^{\circ}\text{C}; V_{CC} = +5 \text{ V} \pm 10\%$

Timing Requirements

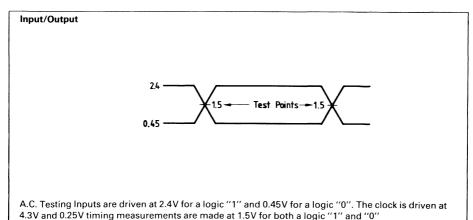
C b l	D	Limi	t Values	11-14-	T . C	
Symbol	Parameter	Min.	Max.	Units	Test Conditions	
t_{CLCL}	CLK Cycle Period	100				
t _{CLCH}	CLK Low Time	50				
t _{CHCL}	CLK High Time	30				
t _{svch}	Status Active Setup Time	35	-	ns	_	
t _{CHSV}	Status Active Hold Time	10				
t _{SHCL}	Status Inactive Setup Time	35	7		·	
t_{CLSH}	Status Inactive Hold Time	10				
t _{ILIH}	Input, Rise Time		20		From 0.8V to 2.0V	
t _{IHIL}	Input, Fall Time	12	7	From 2.0V to 0.8V		

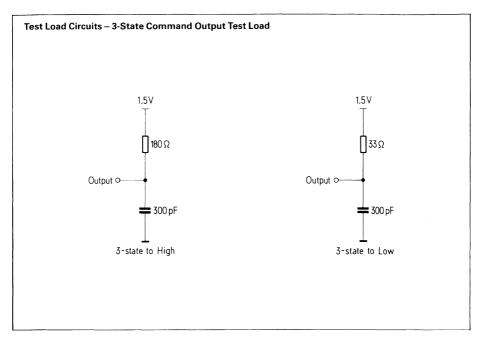
¹⁾ Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

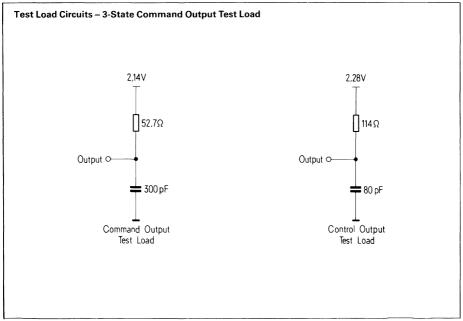
Timing Responses

Symbol	Parameter	Limit	Values	11-:4-	Test Conditions		
	rarameter	Min.	Max.	Units			
t _{CVNV}	Control Active Delay		45				
t _{CVNX}	Control Inactive Delay	10	1 43				
$t_{\text{CLLH}}, t_{\text{CLMCH}}$	ALE MCE Active Delay (from CLK)		20				
t _{SVLH} , t _{SVMCH}	ALE MCE Active Delay (from Status)		20				
t _{CHLL}	AIE Inactive Delay	4	15		MRDC		
t_{CLML}	Command Active Delay	10	35	ns	MWTC	$I_{OL} = 32 \text{ mA}$	
t _{CLMH}	Command Inactive Delay	10		lis	IOWC INTA	$I_{OH} = -5 \text{ mA}$ $C_{L} = 300 \text{ pF}$	
t_{CHDTL}	Direction Control Active Delay		50		AIOWC		
t_{CHDTH}	Direction Control Inactive Delay		30		/,		
t _{AELCH}	Command Enable Time		40		Other	$\begin{cases} I_{OL} = 16 \text{ mA} \\ I_{OH} = -1 \text{ mA} \\ C_{L} = 80 \text{ pF} \end{cases}$	
t _{AEHCZ}	Command Disable Time	1	40		Cinci	$C_{\rm L} = 80 \rm pF$	
t _{AELCV}	Enable Delay Time	115	200				
t _{AEVNV}	AEN to DEN		20				
t _{CEVNV}	CEN to DEN, PDEN		25				
t _{CELRH}	CEN to Command	_	t _{CLML}				
t_{OLOH}	Output, Rise Time		20		From 0.8V	to 2.0V	
t _{OHOL}	Output, Fall Time	1	12		From 2.0V	to 0.8V	

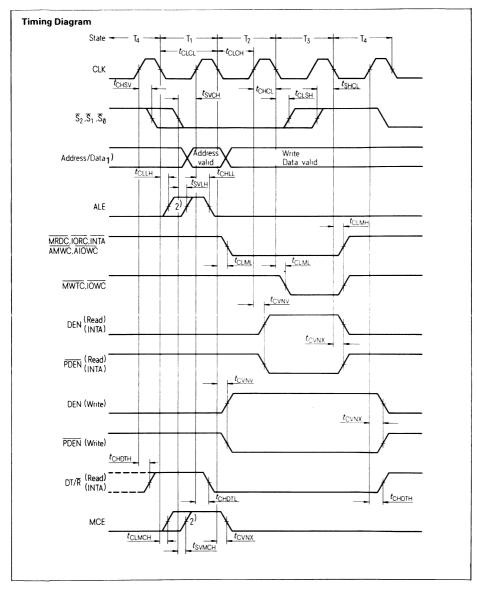
A.C. Testing Input, Output Waveform



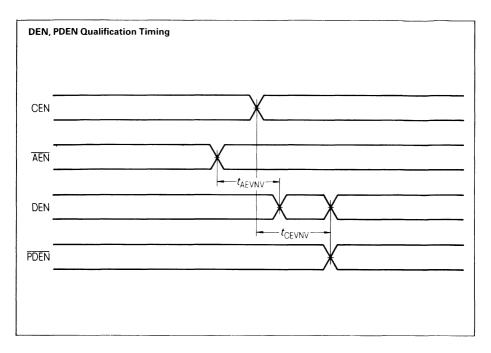


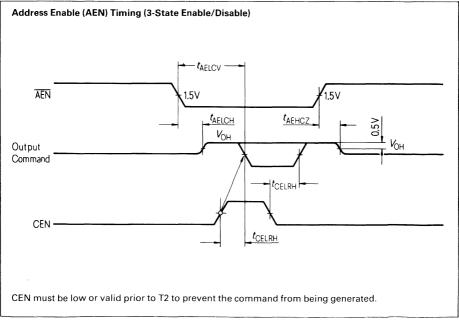


Waveforms

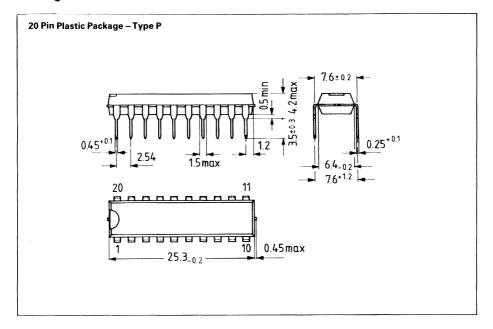


- 1) Address/Data Bus is shown only for reference purposes
- 2) Leading edge of ALE and MCE is determined by the falling edge of CLK or status going active,
- whichever occurs last.
- All timing measurements are made at 1.5V unless specified otherwise.





Package Outline



SAB 8288A

Ordering Information

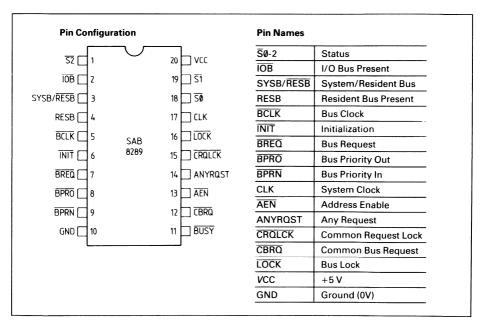
Туре	Description	Ordering code
SAB 8288A-P	Bus Controller (plastic)	Q 67020-Y 155

Preliminary

SAB 8289 Bus Arbiter

SAB 8289 8 MHz SAB 8289-1 10 MHz

- Provides Multi-Master System Bus Protocol
- Synchronizes SAB 8086/SAB 8088 Processors with Multi-Master Bus
- Provides Simple Interface with SAB 8288 Bus Controller
- Four Operating Modes for Flexible System Configuration
- Compatible with Intel Bus Standard MULTIBUS[™] (MULTIBUS is a trademark of INTEL Corporation USA)
- Provides System Bus Arbitration for SAB 8089 IOP in Remote Mode



The SAB 8289 Bus Arbiter is a 20-pin, 5-volt-only bipolar component for use with medium to large SAB 8086/SAB 8088 multi-master/multiprocessing systems. The SAB 8289 provides system bus

arbitration for systems with multiple bus masters, such as an SAB 8086 CPU with SAB 8089 IOP in its REMOTE mode, while providing bipolar buffering and drive capability.

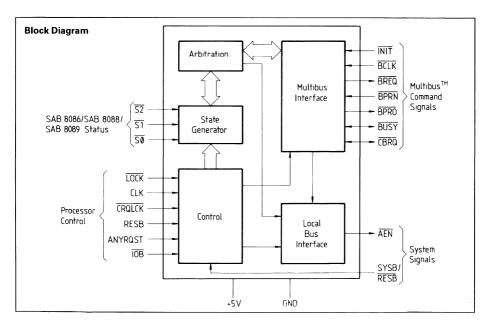
Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function		
SØ, S1, S2	1, 18, 19	1	Status Input Pins These pins are the status input pins from an SAB 8086, SAB 8088 or SAB 8089 processor. The SAB 8289 decodes these pins to initiate bus request and surrender actions.		
CLK	17	1	Clock This is the clock from the SAB 8284A clock chip and serves to establish when bus arbiter actions are initiated.		
LOCK	16	I	Lock LOCK is a processor generated signal which when activated (low) serves to prevent the arbiter from surrendering the multi-master system bus to any other bus arbiter, regardless of its priority.		
CROLCK	15	I	Common Request Lock CRQLCK is an active low signal which serves to prevent the arbiter from surrendering the multi-master system bus to other bus arbiter requesting the bus through the CBRQ inppin.		
RESB	4	I	Resident Bus RESB is a strapping option to configure the arbiter to operate in systems having both a multi-master system bus and a Resident Bus. When it is strapped high the multi-master system bus is requested or surrendered as a function of the SYSB/RESB input pin. When it is strapped low the SYSB/RESB input is ignored.		
ANYRQST	14	1	Any Request ANYRQST is a strapping option which permits the multimaster system bus to be surrendered to a lower priority arbiter as though it were an arbiter of higher priority (i.e., when a lower priority arbiter requests the use of the multi-master system bus, the bus is surrendered as soon as it is possible). Strapping CBRQ low and ANYRQST high forces the SAB 8289 arbiter to surrender the multi-master system bus after each transfer cycle. Note that when surrender occurs BREQ is driven false (high).		
ĪŌB	2	1	IOB us IOB is a strapping option which configures the SAB 8289 Arbiter to operate in systems having both an IO Bus (Peripheral Bus) and a multimaster system bus. The arbiter requests and surrenders the use of the multimaster system bus as a function of the status line, \$\overline{52}\$. The multi-master system bus is permitted to be surrendered while the processor is performing IO commands and is requested whenever the processor performs a memory command. Interrupt cycles are assumed as coming from the peripheral bus and are treated as would be an IO command.		
AEN	13	0	Address Enable AEN is the output of the SAB 8289 Arbiter to the processor's address latches, to the SAB 8288 Bus Controller and SAB 8284A Clock Generator. AEN serves to instruct the Bus Controller and address latches when to tri-state their output drivers.		

Symbol	Number	Input (I) Output (O)	Function
SYSB/RESB	3	1	System Bus/Resident Bus SYSB/RESB is an input signal when the arbiter is configured in the S.R. Mode (RESB is strapped high) which serves to determine when the multimaster system bus is requested and when the multi-master system bus surrendering is permitted. The signal is intended to originate from some form of address mapping circuitry such as a decoder or PROM attached to the resident address bus. Signal transitions and glitches are permitted on this pin from Ø1 of T4 to Ø1 to T2 of the processor cycle. During the period from Ø1 of T2 to Ø1 of T4 only clean transitions are permitted on this pin (no glitches). If a glitch does occur the arbiter may capture or miss it, and the multi-master system bus may be requested or surrendered, depending upon the state of the glitch. The arbiter requests the multi-master system bus in the S.R. Mode when the state of the SYSB/RESB pin is high and permits the bus to be surrendered when this pin is low.
CBRQ	12	1/0	Common Bus Request
	12		CBRQ is an input signal which serves to instruct the arbiter if there are any other arbiters of lower priority requesting the use of the multi-master system bus. The CBRQ pins (open-collector output) of all the SAB 8289 Bus Arbiters which are to surrender the multi-master-system bus upon request are connected together. The Bus Arbiter running the current transfer cycle will not itself pull the CBRQ line low. Any other arbiter connected to the CBRQ line can request the multi-master system bus. The arbiter presently running the current transfer cycle drops its BREQ signal and surrenders the bus whenever the proper surrender conditions exist. Strapping CBREQ low and ANYRQST – high allows the multi-master system bus to be surrendered after each transfer cycle. See the pin definition of ANYRQST.
INIT	6	l	Initialize INIT is an active low multimaster system bus input signal which is used to reset all the bus arbiters on the multi-master system bus. After initialization, no arbiters have the use of the multi-master system bus.
BCLK	5	1	Bus Clock BCLK is the multi-master system bus clock to which all multimaster system bus interface signals are synchronized.
BREQ	7	0	Bus Request BREQ is an active low output signal in the parallel Priority Resolving Scheme which the arbiter activates to request the use of the multi-master system bus.
BPRN	9	1	Bus Priority In BPRN is the active low signal returned to the arbiter to instruct it that it may acquire the multimaster system bus on the next falling edge of BCLK. BPRN indicates to the arbiter that it is the highest priority requesting arbiter presently on the bus. The loss of BPRN instructs the arbiter that it has loss priority to a higher priority arbiter.

Pin Definitions and Functions (continued)

Symbol	Number	Input (I) Output (O)	Function
BPRO	8	0	Bus Priority Out BPRO is an active low output signal which is used in the serial priority resolving scheme where BPRO is daisy chained to BPRN of the next lower priority arbiter.
BUSY	11	I/O	Busy BUSY is an active low open collector multi-master system bus interface signal which is used to instruct all the arbiters on the bus when the multi-master system bus is available. When the multi-master system bus is available the highest requesting arbiter (determined by BPRN) seizes the bus and pulls BUSY low to keep other arbiters off of the bus. When the arbiter is done with the bus it releases the BUSY signal permitting it to go high and thereby allowing another arbiter to acquire the multi-master system bus.
VCC	20	1	Power Supply (+5 V ± 10%)
GND	10	1	Ground (OV)



Functional Description

The SAB 8289 Bus Arbiter operates in conjunction with the SAB 8288 Bus Controller to interface SAB 8086/SAB 8088/ SAB 8089 processors to a multi-master system bus (both the SAB 8086 and the SAB 8088 are configured in their max mode). The processor is unaware of the arbiter's existence and issues commands as though it has exclusive use of the system bus. If the processor does not have the use of the multi-master system bus, the arbiter prevents the Bus Controller (SAB 8288), the data transceivers and the address latches from accessing the system bus (e.g. all bus driver outputs are forced into the high impedance state). Since the command sequence was not issued by the SAB 8288, the system bus will appear as "Not Ready" and the processor will enter wait states. The processor will remain in Wait until the Bus Arbiter acquires the use of the multi-master system bus whereupon the arbiter will allow the bus controller, the data transceivers, and the address latches to access the system. Typically, once the command has been issued and a data transfer has taken place, a transfer acknowledge (XACK) is returned to the processor to indicate "READY" from the accessed slave device. The processor then completes its transfer cycle. Thus the arbiter serves to multiplex a processor (or bus master) onto a multi-master system bus and avoid contention problems between bus masters.

Arbitration between Bus Masters

In general, higher priority masters obtain the bus when a lower priority master completes its present transfer cycle. Lower priority bus masters obtain the bus when a higher priority master is not accessing the system bus. A strapping option (ANYRQST) is provided to allow the arbiter to surrender the bus to a lower priority master as though it were a master of higher priority. If there are no other bus masters requesting the bus, the arbiter maintains the bus so long as its processor has not entered the HALT State. The arbiter will not voluntarily surrender the system bus and has to be forced off by another master's bus request, the HALT State being the only exception. Additional strapping options permit other modes of operation wherein the multimaster system bus is surrendered or requested under different sets of conditions.

Modes of Operation

There are two types of processors in the SAB 8086 family. An Input/Output processor (the SAB 8089 IOP) and the SAB 8086/SAB 8088 CPUs. Consequently, there are two basic operating modes in the SAB 8289 bus arbiter. One, the IOB (I/O Peripheral Bus) mode, permits the processor access to both an I/O Peripheral Bus and a multi-master system bus. The second, the RESB (Resident Bus mode), permits the processor to communicate over both a Resident Bus and a multi-master system bus. An I/O Peripheral Bus is a bus where all devices on that bus, including memory, are treated as I/O devices and are addressed by I/O commands. All memory commands are directed to another bus, the multi-master system bus. A Resident Bus can issue both memory and I/O commands, but it is a distinct and separate bus from the multi-master system bus. The distinction is that the Resident Bus has only one master, providing full availability and being dedicated to that one master.

The $\overline{\text{IOB}}$ strapping option configures the SAB 8289 Bus Arbiter into the $\overline{\text{IOB}}$ mode and the strapping option RESB configures it into the RESB mode. It might be noted at this point that if both strapping options are strapped false, the arbiter interfaces the processor to a multi-master system bus only. With both options strapped true, the arbiter interfaces the processor to a multi-master system bus, a Resident Bus, and an I/O Bus.

In the $\overline{\text{IOB}}$ mode, the processor communicates and controls a host of peripherals over the Peripheral Bus. When the I/O Processor needs to communicate with system memory, it does so over the system memory bus.

The SAB 8086 and SAB 8088 processor can communicate with a Resident Bus and a multimaster system bus. Two bus controllers and only one Bus Arbiter would be needed in such a configuration. In such a system configuration the processor would have access to memory and peripherals of both busses. Memory mapping techniques are applied to select which bus is to be accessed. The SYSB/RESB input on the arbiter serves to instruct the arbiter as to whether or not the system bus is to be accessed. The signal connected to SYSB/RESB also enables or disables commands from one of the bus controllers.

Summary of SAB 8289 Modes, Requesting and Relinquishing the Multi-master system bus

Statu SAB 8	-	es Fro / 88 /	m 89	IOB Mode Only		ode) Only RESB=High	IOB Mode R		Single Bus Mode IOB=High RESB=Low
	S2	S1	S0	IOB=Low	SYSB/RESB	SYSB/RESB	SYSB/RESB	SYSB/RESB	
					=High	=Low	=High	=Low	
I/O	0	0	0	×		×	×	×	
COMMANDS	0	0	1	×		x	x	×	
	0	1	0	x		×	x	x	
HALT	0	1	1	x	x	x	x	х	х
MEM	1	0	0			×		x	
COMMANDS	1	0	1			x		x	
	1	1	0			x		×	
IDLE	1	1	1	x	x	х	х	x	х

NOTE:

x = Multi-Master System Bus is allowed to be Surrendered.

Mode	Pin	Multi-Master System Bus				
wiode	Strapping	Requested**	Surrendered*			
Single Bus Multi-Master Mode	IOB=High RESB=Low	Whenever the processor's status lines go active	HLT+TI•CBRQ+HPBRQ***			
RESB Mode Only	IOB=High RESB=High	SYSB/RESB=High● ACTIVE STATUS	(SYSB/RESB=Low+TI)● CRBQ+HLT+HPBRQ			
IOB Mode Only	IOB=Low RESB=Low	Memory Commands	(I/O Status+TI)●CBRQ+ HLT+HPBRQ			
IOB Mode●RESB Mode	IOB=Low RESB=High	(Memory Command)● (SYSB/RESB=High)	((I/O Status Commands)+ SYSB/RESB=LOW)●CBRQ +HPBRQ***+HLT			

NOTES:

- *LOCK prevents surrender of Bus to any other arbiter, CRQLCK prevents surrender of Bus to any lower priority arbiter.
- **Except for HALT and Passive or IDLE Status.
- ***HPBRQ, Higher priority Bus request or BPRN = 1.
- 1. IOB Active Low.
- 2. RESB Active High.
- 3. +is read as "OR" and as "AND".
- 4. TI=Processor Idle Status \$\overline{S2}\$, \$\overline{S1}\$, \$\overline{S0}=111\$
- 5. HLT=Processor Halt Status \$\overline{S2}\$, \$\overline{S1}\$, \$\overline{S0}\$=011

Absolute Maximum Ratings*

D.C. Characteristics

TA = 0 to 70° C, $VCC = 5 \text{ V} \pm 10\%$

Complete	B	Limit	Values	11	Test Condition	
Symbol	Parameter	Min.	Max.	Unit	lest Condition	
VC	Input Clamp Voltage		-1.0	V	VCC=4.5 V, /C=-5 mA	
/F	Input Forward Current		-0.5	mA	VCC=5.5 V, VF=0.45 V	
/R	Reverse Input Leakage Current		60	μΑ	VCC=5.5 V, VR=5.5 V	
VOL	Output Low Voltage BUSY, CBRQ AEN BPRO, BREQ		0.45	v	/OL = 20 mA /OL = 16 mA /OL = 10 mA	
VOH	Output High Voltage BUSY, CBRQ	0	pen Colle	ctor	_	
	All Other Outputs	2.4	-	V	/OH=400 μA	
/CC	Power Supply Current		165	mA		
ИL	Input Low Voltage		0.8	V		
ИН	Input High Voltage	2.0	_] '	_	
Cin Status	Input Capacitance		25	T		
Cin (Others)	Input Capacitance		12	pF		

^{*)} Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

A.C. Characteristics

TA=0 to 70°C, VCC=5 V \pm 10%

Timing Requirements

			Limit '	11:-	T . 0 . 133		
Symbol	Parameter	SAB	8289 SAB 8		3289-1	Unit	Test Condition
		Min.	Max.	Min.	Max.		
TCLCL	CLK Cycle Period	125		100			
TCLCH	CLK Low Time	65	_	53	_		
TCHCL	CLK High Time	35		35			
TSVCH	Status Active-Setup	65	TCLCL-10	55	TCLCL-10		
TSHCL	Status Inactive-Setup	50	TOLOL-10	45	TCLCL-10		
THVCH	Status Active Hold	10		10			
THVCL	Status Inactive Hold	10		10			
TBYSBL	Busy↑↓Setup to BCLK↓	20	-	20	_		_
TCBSBL	CBRQ↑↓Setup to BCLK↓	20		20		ns	
TBLBL	BCLK Cycle Time	100		100			
TBHCL	BCLK High Time	30	0.65 [TBLBL]	30	0.65 [TBLBL]		
TCLLL1	LOCK Inactive Hold	10		10			
TCLLL2	LOCK Active Setup	40		40			
TPNBL	BPRN↓↑ to BCLK Setup Time	15	_	15	_		
TCLSR1	SYSB/RESB Setup	0		0			
TCLSR2	SYSB/RESB Hold	20		20			
TNIH	Initialization Pulse Width	3TBLBL+ 3TCLCL		3TBLBL+ 3TCLCL			
TILIH	Input Rise Time	_	20		20		From 0.8 to 2.0 \
TIHIL	Input Fall Time		12		12		From 2.0 to 0.8 \

^{↑↓} Denotes the spec applies to both transitions of the signal.

A.C. Testing Input/Output Waveform

Input/Output



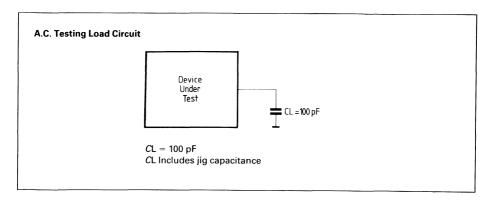
A.C. Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". The clock is driven at 4.3 V and 0.25 V. Timing measurements are made at 1.5 V for both a logic "1" and "0".

Timing Responses

Symbol	Parameter	Limi	t Values	11-:4	Test Condition	
,	rarameter	Min.	Max.	Unit		
TBLBRL	BCLK to BREQ Delay↓↑		35			
TBLPOH	BCLK to BPRO↓↑¹)		40			
TPNPO	BPRN↓↑ to BPRO↓↑ Delay¹)		25		-	
TBLBYL	BCLK to BUSY Low		60	1-		
TBLBYH	BCLK to BUSY Float ²⁾		35			
TCLAEH	CLK to AEN High	_	65	ns		
TBLAEL	BCLK to AEN Low		40			
TBLCBL	BCLK to CBRQ Low		60	1		
TBLCRH	BCLK to CBRQ Float ²⁾		35	1		
TOLOH	Output Rise Time		20	1	From 0.8 to 2.0 V	
TOHOL	Output Fall Time		12		From 2.0 to 0.8 V	

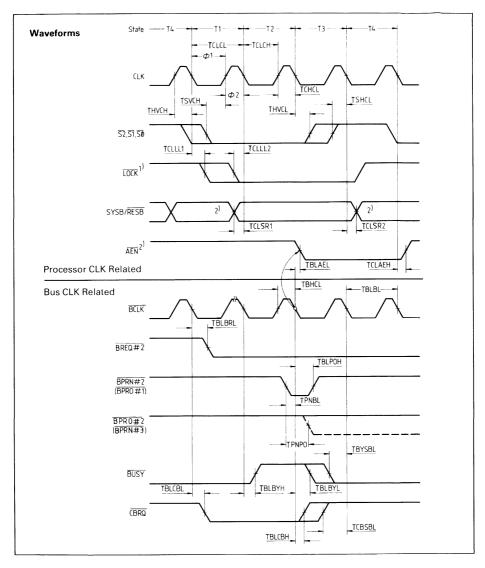
 $[\]downarrow\uparrow$ Denotes the spec applies to both transitions of the signal.

NOTES:



¹⁾ BCLK generates the first BPRO wherein subsequent BPRO changes lower in the chain are generated through BPRON.

²⁾ Measured at 0.5 V above GND.



NOTES:

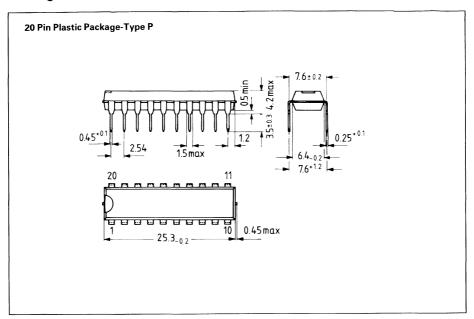
- 1. LOCK active can occur during any state, as long as the relationships shown above with respect to the CLK are maintained.
 - **LOCK** inactive has no critical time and can be asynchronous.
 - CROLCK has no critical timing and is considered an asynchronous input signal.
- 2. Glitching of SYSB/RESB pin is permitted during this time. After I 2 of T1, and before I 1 of T4, SYSB/RESB should be stable.
- 3. AEN leading edge is related to BCLK, trailing edge to CLK. The trailing edge of AEN occurs after bus priority is lost.

Additional Notes:

The signals related to CLK are typical processor signals, and do not relate to the depicted sequence of events of the signals referenced to \overline{BCLK} . The signals shown related to the \overline{BCLK} represent a hypothetical sequence of events for illustration. Assume 3 bus arbiters of priorities 1, 2 and 3 configured in serial priority resolving scheme as shown in Figure 6. Assume arbiter has the bus and is holding busy low. Arbiter #2 detects its processor wants the bus and pulls low \overline{BREQ} #2. If \overline{BPRN} #2 is high (as shown), arbiter #2 will pull low \overline{CBRQ} line. \overline{CBRQ} signals to the higher priority arbiter #1 that a lower priority arbiter wants the bus. [A higher priority arbiter would be granted BPRN when it makes the bus request rather than having to wait for another arbiter to release the bus through \overline{CBRQ}].** Arbiter #1 will relinquish the multi-master system bus when it enters a state not requiring it (see Table 1), by lowering its \overline{BPRO} #1 (tied to \overline{BPRN} #2) and releasing BUSY. Arbiter #2 now sees that it has priority from \overline{BPRN} #2 being low and releases CBRQ. As soon as BUSY signifies the bus is available (high), arbiter #2 pulls BUSY low on next falling edge of BCLK. Note that if arbiter #2 didn't want the bus at the time it received priority, it would pass priority to the next lower priority arbiter by lowering its \overline{BPRO} #2 [TPNPO].

^{**}Note that even a higher priority arbiter which is acquiring the bus through BPRN will momentarily drop CBRQ until it has acquired the bus.

Package Outline



Ordering Information

Component	Description	Ordering Code
SAB 8289-P	Bus-Arbiter 8 MHz (plastic)	Q67020-Y74
SAB 8289-1-P	Bus-Arbiter 10 MHz (plastic)	Q67120-Y85



SAB 82200 Local Bus Arbiter (LBA)

DMA Mode

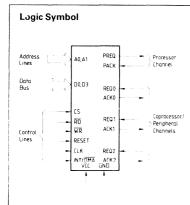
 Arbitrates a local processor bus between up to four potential bus masters (CPU plus three coprocessors)

Interrupt mode

 Multiplexes up to three vectored interrupt sources to one processor interrupt channel

General Features

- Directly cascadable for expansion
- Flexible, programmable priority schemes
- Nested mode of operation possible
- Each input channel individually maskable



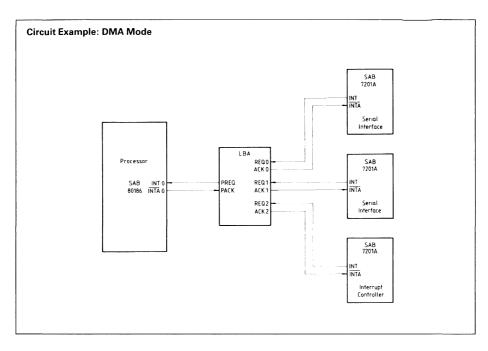
Pin names	
A0, A1	Address Inputs for Register Selection
D0-D3	Data Bus for Programming/Status Read
CS	Chip Select Input
RD	Read Control Line
WR	Write Control Line
INT/DMA	Mode Selection Pin
CLK	Clock Input
RESET	Device Reset
PREQ	Request Output to Processor
PACK	Acknowledge Input from Processor
REQx	Request Inputs from Coprocessor/Peripherals
ACKx	Acknowledge Outputs to Coprocessors/ Peripherals
VCC, GND	Power Supply

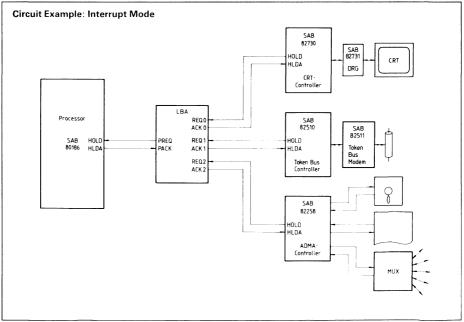
The SAB 82200 Local Bus Arbiter (LBA) is a system support component integrating functions that are needed in complex modern microcomputer systems. In DMA mode it directly arbitrates a processor's local bus between the processor and up to three coprocessors, DMA controllers or peripherals with on-chip DMA controller. Easy adaption to system needs is supported by flexible priority schemes and programmability. Arbitration for more than four bus masters is implemented by directly cascading two or more LBAs

In interrupt mode the LBA can be used to connect several interrupt controllers with vector capability to one processor interrupt channel without requiring compatibility with a specific cascading scheme. Also in interrupt mode the number of devides handled can be expanded by cascading two or more LBAs. The flexible and programmable priority schemes are also provided in this case.

The LBA is fabricated in high-speed ASBC technology and is housed in a 22-pin package.

6.85



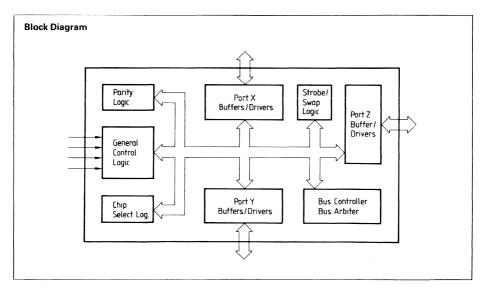


Advance Information

SAB 82220 Bus Interface Controller (BIC)

- Highly integrated microprocessor system support component
- Integrates into one package microprocessor interface logic, like bus drivers, bus control logic, etc.
- · Reduction of
 - chip count up to 80%
 - board space up to 60%
 - power consumption up to 60%
 - design and test effort
 - cost

- Six modes of operation for flexible adaption to different applications
- Support of parity-protected bus systems
- Bus control and arbitration support for Siemens/ Intel 16-bit microprocessors
- Multibus I compatible bus drivers
- Low power consumption due to CMOS technology



Designing modern high-performance microcomputer systems leads to multiprocessor architectures with multiple buses and/or dual-port memories. Those types of architecture require an increasing amount of interface logic. Designed with standard components, however, that logic would need many packages with a great number of interconnections and consume a lot of board space and power consumption. The SAB 82220 Bus Interface Controller (BIC) solves those problems by integrating

many interface functions into one package, thus providing easy interface design. Flexible adaption to different systems and applications is supported by its six different modes of operation. The selection of the operating modes and the respective programming is done via strapping pins thus avoiding processor programming and control overhead. The BIC is housed in a 68-pin plastic leaded chip carrier package and fabricated in Siemens Advanced CMOS Technology.

6.85

BIC Operating Modes

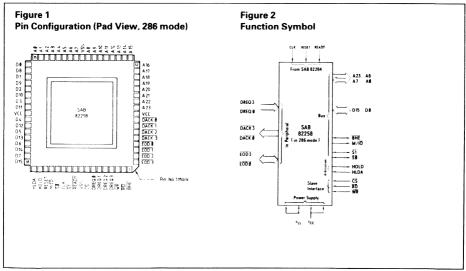
MODE 1:	Tridirectional Transceiver In this mode three buses can be interconnected. Transfers between those three buses are possible in any direction. Data transfers and address transfers are supported (unlatched and latched operation). Instead of 18-bit transfer width, 16-bit transfer width byte paritiy check/generation can also be selected. One port support active low buses (automatic signal inversion). Byte swap in every transfer direction is possible.
MODE 2:	Bidirectional Transceiver Similar to mode 1 but with two 27-bit buses (or 24 bit with byte parity).
MODE 3:	Bidirectional Transceiver with CS Generation The main application of this mode lies in address transfer. Five chip select (CS) outputs can be generated for programmable address ranges.
MODE 4:	Bidirectional Transceiver with Bus Control Logic In mode 4 the BIC implements a bidirectional data/address transceiver with bus control function. The function of the bus controller can be selected as being a SAB 8288 or a SAB 82288.
MODE 5:	Bidirectional Transceiver with Bus Controller and Bus Arbiter In this mode BIC provides in addition to a 16-bit bidirectional bus transceiver the functions of the SAB 82288 Bus Controller and the SAB 82289 Bus Arbiter.
MODE 6:	Multiplex Bus Tranceiver This mode supports applications using processors (coprocessors) with multiplex bus interface.

Advance Information

SAB 82258 ADMA-Advanced DMA Controller for 16 bit Microcomputer Systems

- 16 bit DMA Controller for 16 bit Family Processors SAB 80286 SAB 8086/88 SAB 80186/188
- 4 Independent Channels
- 16 Mbyte Addressing Range
- 16 Mbyte Byte Count
- Memory Based Communication with CPU
- "On-the-Fly" Compare, Translate and Verify Operations

- Transfer Rates up to 8 Mbyte/sec
- Single and Double Cycle Transfer
- Automatic Chaining of Command Blocks
- Automatic Chaining of Data Blocks
- Multiplexor Mode Operation with 32 Subchannels
- Local and Remote (Stand Alone) Mode of Operation



SAB 82258 is an advanced DMA (Direct Memory Access) Controller designed especially for the 16 bit microprocessors SAB 80286 and SAB 8086/186/88/188. In addition, the operation with other processors is supported by the remote mode. It has 4 independent DMA channels which can transfer data at rates up to 8 Mbytes/second at 8 MHz

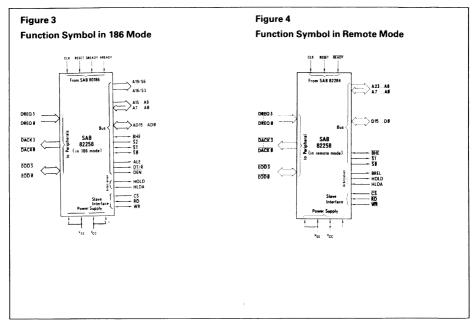
clock in a SAB 80286 system or up to 4 Mbytes/ second at 8 MHz in a 8086/80186 system. This great bandwidth allows the user to handle very fast data transfer or a large number of concurrent peripherals. The device is fabricated in advanced +5 Volt N-channel Siemens MYMOS technology and packaged in a 68 pin package.

2.85

Modes of Operation, Adaptive Bus Interface

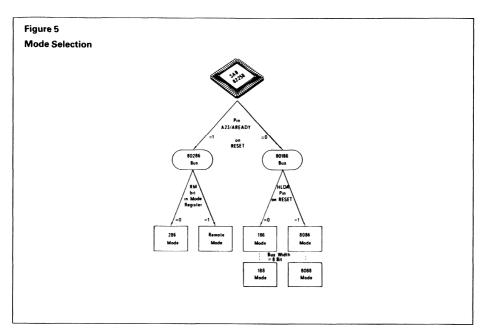
SAB 82258 has been defined to work with all 16 bit processors, i.e. SAB 80286, SAB 80186/188 and SAB 8086/88 without additional support and interface logic. Hence the local busses of above

processors are different in signals, functions and timings, SAB 82258 has an adaptive bus interface to meet the different requirements of these local busses.



As a result of this, a bus compatibility with identical timing is attained with processors SAB 80286, SAB 80186 and SAB 8086. A compatibility with the 8 bit bus versions of these processors SAB 8088 and SAB 80188 is also guaranteed by defining the

physical bus width of SAB 82258 (per software) as 8 bits. The only difference in operation with SAB 8086 or SAB 80186 is that for SAB 8086 the HOLD pin functions as $\overline{RQ}/\overline{GT}$ line (if HLDA is held high on RESET).



SAB 82258 can also operate in a remote or stand alone mode where it is not coupled directly to a processor. Figure 5 shows the way how SAB 82258 detects with which processor or in which mode it is operating. Figure 2 shows the logic pinning in the 286 mode – for operation with SAB 80286. Figure 3 shows the logic pinning in the 186 mode – for operation with SAB 80186/188 and SAB 8086/88, and Figure 4 shows the pinning when SAB 82258 is in the remote mode and not directly coupled to a processor.

Pin Definitions and Functions

The pins of SAB 82258 have different meaning for each of the 4 modes of bus operation. The pinning in 286 mode and remote mode as well as 186 and 8086 mode are very similar. Table 1 summarizes the pinning of SAB 82258 in the various modes, the following sections give a detailed description of the pin function in each of the modes.

Table 1 Pin Name and Function

Pin No.	28	6 mode	Rem	ote mode	186/8	186/8086 mode	
PIN NO.	Designa- tion	Input/ Output	Designa- tion	Input/ Output	Designa- tion	Input/ Output	
16	HOLD	0	HOLD	0	HOLD or RQ/GT	O (186) I/O (8086)	
17	HLDA	1	HLDA	1	HLDA	1	
1	BHE	1/0	BHE	1/0	BHE	1/0	
14	M/IO	o	BREL	О	<u>52</u>	О	
11	<u>\$1</u>	1/0	<u>\$1</u>	О	<u>51</u>	1/0	
13	<u>50</u>	1/0	<u>50</u>	О	<u>50</u>	1/0	
8	CS		cs	1	cs	1	
2	RD	1,	RD	1	RD	1/0	
3	WR	- Li	WR	l i	WR	1/0	
10	READY	i	READY	1	SREADY	1	
59	A23	0	A23	О	AREADY	1	
58	A22	o	A22	lo	ALE	0	
57	A21	0	A21	o	DT/R	o	
56	A20	o	A20	lo	DEN	lo	
55	A19	o	A19	О	A19/S6	О	
54	A18	o	A18	o	A18/S5	О	
53	A17	o	A17	lo	A17/S4	О	
52	A16	О	A16	О	A16/S3	О	
51	A15	О	A15	0	A15	О	
50	A14	О	A14	О	A14	О	
49	A13	О	A13	lo	A13	0	
48	A12	О	A12	lo	A12	0	
47	A11	o	A11	0	A11	О	
46	A10	0	A10	0	A10	О	
45	A9	О	A9	О	A9	0	
44	A8	О	A8	0	A8	0	
42	A7	1/0	A7	1/0	A7	1/0	
41	A6	1/0	A6	1/0	A6	I/O	
40	A5	1/0	A5	1/0	A 5	1/0	
39	A4	1/0	A4	1/0	A4	I/O	
38	А3	1/0	A3	1/0	A3	1/0	
37	A2	I/O	A2	1/0	A2	1/0	
36	A1	1/0	A1	1/0	A1	1/0	
35	A0	1/0	A0	1/0	A0	1/0	

Pin No.	28	286 mode		ote mode	186/8	186/8086 mode	
111110.	Designa- tion	Input/ Output	Designa- tion	Input/ Output	Designa- tion	Input/ Output	
18	D15	1/0	D15	1/0	AD15	1/0	
20	D14	I/O	D14	1/0	AD14	1/0	
22	D13	1/0	D13	1/0	AD13	1/0	
24	D12	1/0	D12	1/0	AD12	1/0	
27	D11	1/0	D11	1/0	AD11	1/0	
29	D10	1/0	D10	1/0	AD10	1/0	
31	D9	I/O	D9	1/0	AD9	1/0	
33	D8	I/O	D8	1/0	AD8	I/O	
19	D7	I/O	D7	1/0	AD7	1/0	
21	D6	I/O	D6	1/0	AD6	1/0	
23	D5	1/0	D5	1/0	AD5	1/0	
25	D4	1/0	D4	1/0	AD4	1/0	
28	D3	I/O	D3	1/0	AD3	1/0	
30	D2	I/O	D2	1/0	AD2	1/0	
32	D1	1/0	D1	1/0	AD1	1/0	
34	D0	1/0	D0	1/0	AD0	1/0	
7	DREQ0	1	DREQ0	1	DREQ0	1	
6	DREQ1	11	DREQ1	1	DREQ1	1	
5	DREQ2	- 1	DREQ2	1	DREQ2	1	
4	DREQ3	1	DREQ3	į į	DREQ3	1	
61	DACK0	0	DACK0	0	DACK0	0	
62	DACK1	0	DACK1	0	DACK1	0	
63	DACK2	0	DACK2	0	DACK2	0	
64	DACK3	О	DACK3	О	DACK3	0	
65	EOD0	1/0	EOD0	1/0	EOD0	1/0	
66	EOD1	1/0	EOD1	1/0	EOD1	1/0	
67	EOD2	1/0	EOD2	1/0	EOD2	1/0	
68	EOD3	1/0	EOD3	1/0	EOD3	1/0	
15	RESET	1	RESET	1	RESET	ı	
12	CLK	1	CLK	1	CLK	1	
9,43	vss	(Ground)	vss	(Ground)	vss	(Ground)	
26,60	vcc	(Power Supply)	vcc	(Power Supply)	vcc	(Power Supply)	

Pinning in 286 Mode

In the 286 mode the SAB 82258 bus signals and bus timings are the same as of the SAB 80286 processor. Additional features of SAB 82258 require a slight change in pin definitions. The processor can access internal registers of the SAB 82258. Therefore the bus signals must

support these accesses. This means that some of the bus control signals must be bidirectional and some additional bus control signals are necessary. All pins and their functions are listed below.

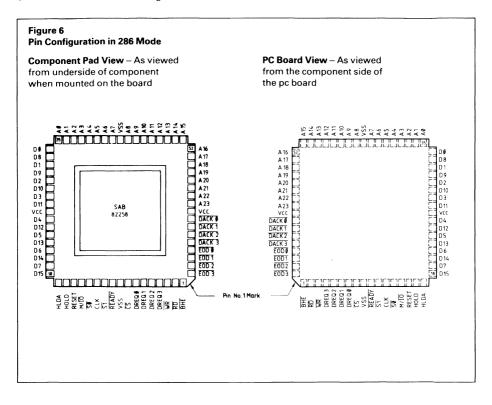


Table 2
Pin Description for 286 Mode

(Contains also the description for pins identical in all modes)

Symbol	Number	Input (I) Output (O)	Functions				
BHÉ	1	1/0	Bus High Enable indicates transfer of data on the upper byte of the data bus, D15–8. Eight-bit oriented devices assigned to the upper byte of the data bus would normal use BHE to condition chip select functions. BHE is active LOW and floats to 3-state OFF when the SAB 82258 doe not own the bus.				
			BHE and A0 encodings				
			BHE A0 Function				
			0 0 Word transfer (D15-0) 0 1 Byte transfer on upper half of data bus (D15-8) 1 0 Byte transfer on lower half of data bus (D7-0) 1 1 Odd addressed byte on 8 bit bus (D7-0)				
RD	2	1	Read command in conjunction with chip select enables reading out of SAB 82258 register which is addressed by the address lines A7—A0. This signal can be asynchronous to SAB 82258 clock.				
WR	3	I	Write command is used for writing into SAB 82258 registers. This signal can be asynchronous to SAB 82258 clock.				
DREQ0- DREQ3	4-7	1	DMA request input signals are used for synchronized DMA transfers. DREQ3 has the meaning of I/O request (IOREQ) if channel 3 is a multiplexer channel. These signals can be asynchronous to SAB 82258 clock.				
cs	8	I	Chip select is used to enable the access of a processor to SAB 82258 registers. This access is additionally controlled either by bus status signals or by the Read or Write command signals. Chip select can be asynchronous to SAB 82258 clock.				
READY	10	I	Bus Ready terminates a bus cycle. Bus cycles are extended without limit until terminated by READY LOW. READY is an active LOW synchronous input requiring setup and hold times relative to the system clock be met for correct operation.				

Symbol	Number	Input (I) Output (O)	Fun	ctions		
S0, S1	11, 13	1/0	The both indicate of the control of	begin n going cated I us rea type o 86 mo same r ve only reas in ress or owing I M/IO	ning o g active by all s dy sign of bus o de) or meanin wher n 286 r n the a bus cy	ignals control the support circuits. If a bus cycle is indicated by \$\overline{37}\$ or \$\overline{30}\$ or e. The termination of a bus cycle is status signals going inactive in 186 mode nal (\$\overline{READY}\$) going active in 286 mode. cycle is indicated by \$\overline{30}\$, \$\overline{31}\$ and \$\overline{32}\$ or \$\overline{31}\$ or \$\overline{32}\$ and \$\overline{31}\$ or \$\overline{32}\$ signal can be not least one of \$\overline{31}\$ or \$\overline{30}\$ is active, mode the \$\overline{M/IO}\$ signal is valid with the address lines. \$\overline{348}\$ SAB 82258 can generate the received by activating the status signals \$\overline{358}\$ mode): Cycle Type
			0	0	0	Read I/O-Vector
			0	0	1	(for Multiplexor channel) Read from I/O Space
			0	1	0 1	Write into I/O Space No bus cycle, does not occur in 186 mode
			1	0	0	Does not occur
		Read from Memory Space Write into Memory Space				
			1	1	1	No bus cycle
			syn- tabl	chrono e shov	ous aco	re used as inputs for detection of cesses to SAB 82258. The following bus status and CS, signals and their y SAB 82258. Description
			1	X	X	SAB 82258 is not (no action)
			0	0	0	selected no SAB 82258 access (no action)
			0	0	1	Read from an SAB 82258 register
			0	1	0	Write into an
			0	1	1	SAB 82258 register No bus cycle (Note 1)
			Not	ac m	cess is	258 is selected but no synchronous s activated. In this case SAB 82258 s RD and WR signals for detection of an onous access.
CLK	12	1	two the the circ gen inpi	times SAB 8: SAB 8 uitry c erator ut, or b	the sy 2284 C 2258 in an be by a L by first	des the fundamental timing. It must be stem clock. It can be directly connected to LK output. It is divided by two to generate nternal clock. The on chip divide-by-two synchronized to the external clock. OW to HIGH transition on the RESET HIGH to LOW transition on the Status after RESET.

Symbol	Number	Input (I) Output (O)	Functions			
M/IO	14	0	Distinction between memory and I/O space addresses.			
RESET	15	I	An activation of the reset signal forces SAB 82258 to the initial state. The reset signal must be synchronous to CLK			
HOLD	16	0	HOLD output, when true, indicates a request for contro of the local bus. When the SAB 82258 relinquishes the bus it drops the HOLD output.			
HLDA	17	I	HLDA, when true, indicates that the SAB 82258 can acquire the control of the bus. When it goes low SAB 822 must relinguish the bus at the end of its current cycle. It can be asynchronous to the SAB 82258 clock.			
D0-D15	18-25, 27-34	I/O	Data Bus – This is the bidirectional 16 bit data bus. For use with an 8 bit bus, only the lower 8 data lines D7-D0 are relevant.			
A0-A7	35-42	I/O	The lower 8 address lines for DMA transfers. They are all used to input the register address when the processor accesses a SAB 82258 register.			
A8-A23	44-59	0	Higher address outputs.			
DACKO- DACK3	61-64	0	The DACK i signal acknowledges the requests on the related DREQ i signal. It is activated when the requested transfer(s) is (are) performed. If the channel 3 is a multiplexor channel the signal DACK3 has the meaning of I/O acknowledge (IOACK).			
EODO- EOD3	65-68	1/0	The End of DMA signals are implemented as open drain output drivers with a high impedance pull up resistor and thus can be used as bidirectional lines. As outputs the signals are activated for two system clock cycles at the end of the DMA transfer of the corresponding channel (if enabled) or they are activated under program control (EOD output or interrupt output). If the signals are held internally high but forced to low by external circuitry, they act as "End-of-DMA" inputs . The current transfer is aborted and SAB 82258 continues with the next command. Additionally, a special function is possible with the EOD2 pin: this pin can also be used as common interrupt signa for all 4 channels. In this mode this signal is not a open drain output but a pushpull output (output only). The other EOD pins may be used as EOD outputs/inputs described above.			
VCC	26,60		Power supply (5 V)			
VSS	9,43		Ground (0 V)			

Pinning in 186 Mode

In 186 mode many pins have a different meaning than in the 286 mode. They are listed below (for corresponding 286 names see table 1).

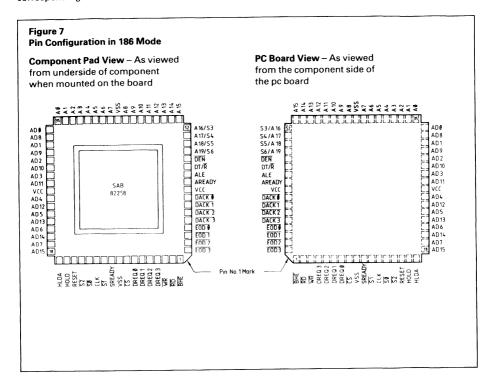


Table 3
Changes of Pin Description in 186 mode

Symbol	Number	Input (I) Output (O)	Functions			
RD WR	2,3	1/0	In 186 mode, the RD and WR pins are additionally used as output pins to support 80186 or 8086 minimum mod systems.			
ALE	58	0	Address latch enable signal provides a strobe to separate the address information on the multiplexed AD lines.			
DEN	56	0	Data enable signal is used for enabling the data transceiver.			
DT/R	57	0	Data transmit/receive signal controls the direction of data transceivers. When LOW, data is transferred to tl SAB 82258, when HIGH the ADMA places data on to tl data bus.			
<u>\$2</u>	14	0	Status signal as for SAB 186/8086/88 processors (see also \$\overline{51}\$, \$\overline{50}\$ description in 286 mode).			
AREADY	59	I	This is an asynchronous bus ready signal, the rising edge is internally synchronized, the falling edge must be synchronous to CLK. During reset this signal must be low for entering the 186 mode.			
SREADY	10	ı	Synchronous ready input. This signal must be synchronized externally. The use of this pin permits a relaxed system-timing specification by eliminating the clock phase which is required for resolving the signal level when using the AREADY input.			
CLK	12	1	This is the input for the one time system clock. No internal prescaling is done.			
AD0- AD15	18-25 27-34	1/0	Lower address and data information is multiplexed on pin AD0-AD15. Additionally the demultiplexed address			
A0-A7 A8-A15	35-42 44-51	I/O O	information is available on address pin A0 – A15.			
A16/S3- A19/S6	52, 55	0	The higher address bits are multiplexed with additional status information.			

Pinning in 8086 Mode

In 8086 mode the bus arbitration is done via $\overline{RQ}/\overline{GT}$ protocol instead of the HOLD/HLDA protocol in 186

mode. The function of the other pins is identical to 186 mode.

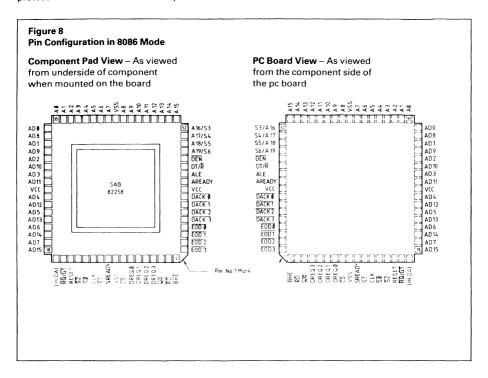


Table 4
Changes of Pin Description in 8086 Mode

Symbol	Number	Input (I) Output (O)	Functions
RG/GT	16	1/0	In the 8086 mode the HOLD input acts as REQUEST/GRANT line. The REQUEST/GRANT protocol implements a one-line communication dialog required to arbitrate the use of the system bus normally done via HOLD/HLDA. The RG/GT signal is active low and has an internal pullup.
HLDA	17	I	After entering 8086-mode this pin no longer acts as hold-acknowledge input for the bus arbitration with the processor. But it can still be used to force the SAB 82258 off the bus by a low input level (e.g. it a third priority bus master needs the bus).

Pinning in Remote Mode

In remote mode most of the bus signals have the same functions as in the $286 \, \text{mode}$. The other pins are listed below.

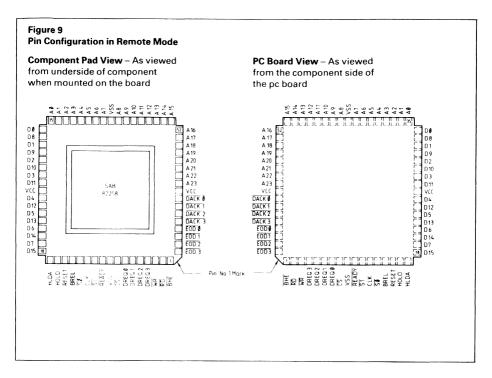


Table 5
Changes of Pin Description in Remote Mode

Symbol	Number	Input (I) Output (O)	Functions
BREL	14	0	In this mode pin 14 is used to indicate when SAB 82258 has released the control of the local bus.
<u>cs</u>	8		In Remote Mode the $\overline{\text{CS}}$ input has two functions: besides enabling the access to SAB 82258 internal registers it works as an Access Request input. When forced to low it signals the SAB 82258 that another bus master needs access to the local bus of the SAB 82258 (e.g. to read/write SAB 82258 registers). SAB 82258 releases the bus as soon as possible and indicates this by activating the BREL output.
HOLD HLDA	16 17	O 	Signals on these pins are only used for access to the system bus. They are connected to the bus arbiter. Resident bus accesses are directly executed (without HOLD/HLDA sequence).

Functional Description

General

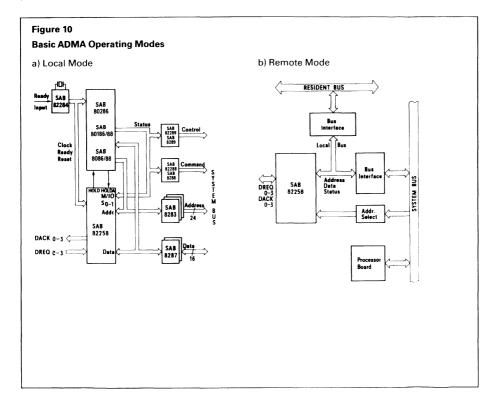
SAB 82258 is an advanced general purpose DMA controller especially tailored for efficient high speed data transfers on a SAB 80286 as well as an SAB 80186/188 or SAB 8086/88 bus.

It supports two basic operating modes:

- local mode (tightly coupled to a processor) and
- remote mode (loosely coupled to a processor).

In the first case SAB 82258 is directly coupled to the CPU and uses the same system support/control devices as the CPU (see figure 10a). This mode is possible with the above mentioned processors.

As a second basic operating mode a remote (stand alone) mode is supported (see fig. 10b). Here the SAB 82258 has his own sets of bus interface circuits and thus can dispose of its own local bus. This allows the DMA-controller to work in parallel to the main CPU and therefore overall system performance could be increased. Besides that, this mode is very useful for the design of modular systems and allows connecting the ADMA to any other processor via the system bus independent of the processor's unique local bus.

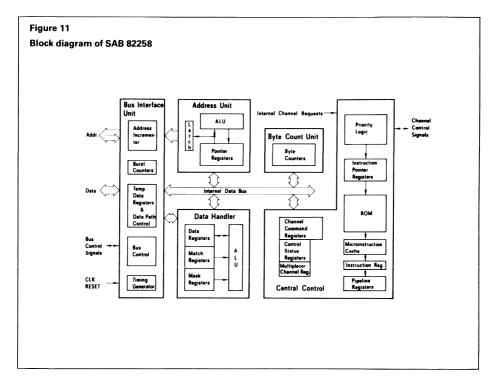


SAB 82258 has four independent DMA channels that can transfer up to 8 Mbytes/sec in the single cycle mode (2 clocks/transfer). In the 2 cycle transfer mode the maximum rate is 4 Mbytes/sec.

Switching between channels induces no time penalty. Thus the overall maximum transfer rate of

8 Mbytes/sec is also valid for multiple channel operation.

This fast operation is possible because of the pipelined architecture of the SAB 82258 that allows the different function units to work in parallel.



The ADMA supports two address spaces, memory space and I/O space, each with a maximum address range of 16 Mbytes. In addition, the maximum

block length (byte count) is also 16 Mbytes to support applications where large blocks of data have to be transferred (e.g. graphics).

As source or as destination, four parameters can be independently selected:

- Address Space (memory or I/O)
- Physical Bus Width (8 bit or 16 bit),
- Logical Bus Width (same as physical bus width or 8 bit on a 16 bit physical bus)
 and
- Transfer Direction (increasing, decreasing, fixed pointer or constant value).

If the physical bus width of source or destination does not meet the logical bus width an automatic byte/word assembly (word/byte disassembly) takes place if this minimizes the necessary transfers. The same is true if the logical bus widths of source and destination are different.

Transfers between different address spaces can be performed within one cycle or in two cycles, transfers within one address space can be performed only in two cycles.

The transfers can be executed free running or externally synchronized via DRQ where source or destination synchronization is possible.

In summary, this very symmetrical operation of SAB 82258 gives the user a great amount of design flexibility.

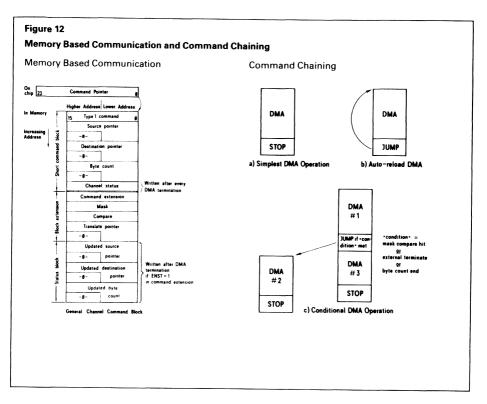
Adaptive Bus Interface

As shown in figure 5 the SAB 82258 bus interface has two basic timing modes: the 286 mode and the 186 mode. In 286 mode SAB 82258 is directly coupled to an SAB 80286, in 186 mode to an SAB 80186 or SAB 80188. For each of these two modes a slightly different variation exists:

- For the 286 mode, the Remote Mode, where the ADMA operates as a bus master on the system bus without being directly coupled to a processor. In this mode SAB 82258 can dispose of its own local bus and the communication with the main processor is done via the system bus. To enable access to ADMA registers by the main processor, SAB 82258 must release its local bus. This "local bus arbitration" in remote mode is done via the CS and BREL lines.
- For the 186 mode the variation is the 8086 mode where the SAB 82258 supports the RQ/GT protocol and thus can be directly coupled to an SAB 8086 or SAB 8088.

Memory Based Communication

The normal communication between the ADMA and the processor is memory based. This means that all necessary data for a transfer is contained in a command block in memory accessible for CPU and SAB 82258 (see figure 12). To start the transfer the CPU loads one of the command pointer registers of SAB 82258 with the address of the command block and then gives a "start channel command". Getting the command SAB 82258 loads the entire command block from memory into its on-chip channel registers and executes it. On completing the operation, channel status information is written back by SAB 82258 into the channel status word contained in the command block in memory. If desired the actual contents of the channel registers, i.e. source pointer, destination pointer and byte count is transferred into the Channel Status Block. The Channel Status Block immediately follows the Command Block in memory (see figure 12).



Command Chaining

Command blocks for any channel can be chained for sequential execution (see figure 12). When SAB 82258 comes to an end with one command, it automatically starts to fetch and execute the next command block until a stop command is found. As a result a chain of command blocks can be executed by the ADMA without any CPU intervention. Due to conditional and unconditional STOP and JUMP commands, quite complex sequences of DMA can be executed by SAB 82258.

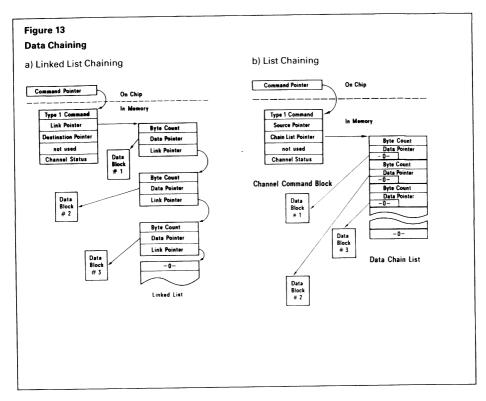
Data Chaining

Data chaining permits an automatic, dynamic linking of data blocks scattered in memory. There are two types: list and linked-list data chaining.

If for a DMA the source blocks are to be dynamically linked during DMA it is called source chaining and the effect is that of gathering data blocks and sending them out effectively as one block.

If one source block is dynamically broken-up into multiple destination blocks, it is called destination chaining. This results in scattering of a block.

This dynamic linking and un-linking of data blocks makes the logical sequencing of data independent of its physical sequencing in memory.



In the case of linked list chaining (see figure 13 a) each data block has a descriptor containing information on position of data block in memory, length of data block, and a pointer to the next description.

During data transfer the data block 1 is sent out first, then 2 and so on till a 0 is encountered in the byte count field.

The second type of data chaining is List Chaining (figure 13 b).

Unlike linked list chaining, here the data block descriptors are continuous in a block and thus determine the sequence of data blocks. The flexibility lost in terms of predefined sequence is gained in terms of linking time.

"On-The-Fly" Operations

A normal DMA controller blindly transfers data from source to destination without looking at the data. In case of the ADMA on-the-fly operations are executed during the DMA transfer and allow inspection and/or operation on the transferred data. There are three on-the-fly operations possible:

- Mask/Compare,
- Translate and
- Verify

During a mask/compare operation each byte/word transferred is compared to a given pattern. One or more bits can be masked and thus do not contribute to the result of the compare operation. The result can be used by subsequent conditional stop or jump operations.

For translate operation the byte (no word possible) that is fetched from source is added to a translate pointer to build the effective source pointer. The byte pointed to by this pointer is then fetched and sent out to the destination. Of course a mask/compare operation is possible on the byte sent out.

The verify operation is a type of block compare operation to compare each byte/word of data read from a peripheral with that in a data block in memory. There are three options:

- 1. Verify with no termination on mismatch (2-cycle transfer only)
- 2. Verify with termination on mismatch (2-cycle transfer only).
- Verify and save (single cycle transfer only).
 Here an actual transfer with compare takes place.
 The transfer is not stopped on mismatch.

Multiplexer Channel

When programmed to multiplexer mode channel 3 (supported by a multiplexer logic) can be used to service up to 32 subchannel request lines (see figure 14). Thus it is ideally suited to service a large number of relatively slow equipment like CRT terminals, line printers etc. Since multiple subchannels are processed with the resource of one DMA channel, the overhead of subchannel switching, of course, decreases the total effective throughput on the multiplexer channel.

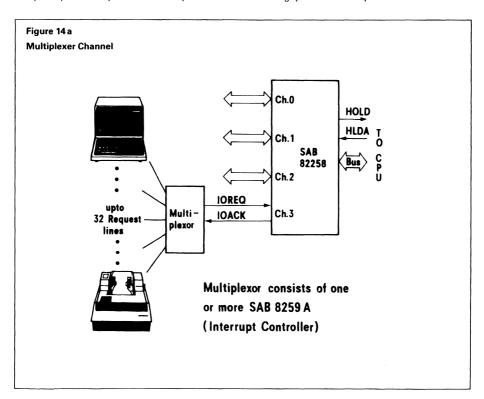


Figure 14b) Structure of Multiplexer Table Multiplexor Table Pointer On Chip Requests from Devices Multiplexor Table In Memory Subchannel 0 Command Chain SAB 8259 A Subch.#0 Pointer Type 1 Command 8 Bytes -0per Subchannel Subch.#0 Mask Type 1 Command -0-Pointer Stop and Mask Intr. Command Subch.#1 8 Bit Vector Pointer Subchannel 1 Command Chain (Device Number) -0-Subch.#1 Mask Type 1 -0-Pointer Type 2 Subch.#2 Type 1 Subch.#2 Stop and Mask Intr. Command Mask Pointer Type 1 Type 1 Type 1 Stop and Mask Intr. Command The mask pointer is the address of the appropriate SAB 8259A mask register.

Operating the SAB 82258

Reset

When activating the reset input, SAB 82258 is forced into its initial state. All channels and bus activities are stopped, tristate lines are tristated and the others enter the inactive state.

While the reset input is active line A23/AREADY and HLDA must be forced to the appropriate levels to select the desired bus interface mode (see figures 5 and 36).

After deactivating reset the inactive state is maintained, in addition the state of SAB 82258 registers is as follows:

- General Mode Register, General Burst Register, General Delay Register, General Status Register and the four Channel Status Registers are set to zero,
- the Vector Not Valid bit of the Multiplexer Interrupt Vector Register is set to 1,
- all other registers and bits are undefined.

Note that the General Mode Register (GMR) should be loaded first to select the mode of operation before any other activity is started on the ADMA.

DMA Interface

The DMA interface consists of three lines:

- DRQ DMA request,
- DACK DMA acknowledge and
- EOD end of DMA

The first two lines work as request and acknowledge lines to control synchronized DMA transfers as known from conventional DMA controllers.

A special feature of SAB 82258 are the bidirectional EOD lines. First they can be used as inputs to receive an asynchronous external terminate signal to terminate a running DMA. Second, as an output, they can be used to send out a pulse which interrupts the CPU and/or signals to the peripheral a specific status (e.g. transfer aborted or end of a block or send/receive next block.)

The EOD output signal can be generated synchronously to a transfer (during the last transfer) or asynchronously to the transfers by a specific command.

In addition the EOD output of channel 2 can be used as a collective interrupt output for all DMA channels while the other three retain their normal function.

Slave Interface

The slave interface is used to access SAB 82258 internal registers. Although nearly all of the communication between CPU and ADMA is done

via memory based data blocks, some direct accesses to ADMA registers are necessary. For example during the initialization phase the general mode registers must be written, or to start a channel the command pointer register and the general command register must be loaded. Also during the debugging phase it is of great benefit to have access to all of the SAB 82258 internal registers.

The slave interface is enabled by the \overline{CS} input and consists of the following lines:

- RD, WR Control Lines (inputs)
- A0−A7 Register Address (inputs)
- D0-D15 Data Lines (inputs/outputs) and
- AD0-AD15-Address/Data Lines (inputs/outputs) for synchronous access in 186 mode

Note, that all of these lines are outputs if SAB 82258 is an active bus master.

In 186 mode and 286 mode two types of accesses are possible:

- Synchronous access by means of the status lines.
 Processor and SAB 82258 are directly coupled and must use the same clock.
- Asynchronous access by using the control lines RD and WR (processor and ADMA may have different clocks).

In all modes except the synchronous access in 186 mode the register address must be supplied on address pins A0–A7. Using synchronous access in 186 mode the address information is expected at address/data lines AD0–AD7.

In remote mode only the asynchronous access is possible because SAB 82258 first has to release its local bus to enable the register access. On receiving an access request (activation of $\overline{\text{CS}}$ input) SAB 82258 releases its local bus as soon as possible and signals this by activating the BREL line. Now the CPU can accomplish its access.

Register Set

Figure 15 shows the user visible registers of SAB 82258. A set of 5 registers, called the general registers, is used for all the 4 channels. The mode register is written first after reset and it describes the SAB 82258 environment – bus widths, priorities etc. The General Command Register (GCR) is used to start and stop the DMA transfer on different channels. General Status Register (GSR) shows the status of all the 4 channels; if the channel is running, if interrupt is pending etc. General Burst Register (GBR) and General Delay Register (GDR) are used to specify the bus load which is permissible for SAB 82258.

There is a set of channel registers for each of the 4 channels. Most channel registers serve as cache registers and need to be accessed only for debugging. During normal operation they are automatically loaded by SAB 82258 (see next paragraph).

The layout of register addresses is shown in figure 16. All register lie at even addresses. Locations not designated in figure 16 are reserved.

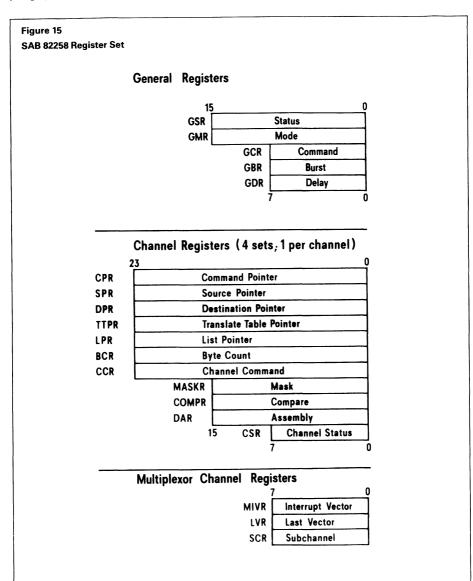


Figure 16 Layout of Register Addresses

Address Bits	Address Bits 7,6					
0 - 5	00	01	10	11		
0	GCR					
2	SCR					
4	GSR					
6				† — — — — — — — — — — — — — — — — — — —		
8	GMR					
Α	GBR					
С	GDR			1		
E						
10	CSRø	CSR ₁	CSR ₂	CSR ₃		
12	DARø	DAR ₁	DAR ₂	DAR ₃		
14	MASKRø	MASKR ₁	MASKR ₂	MASKR ₃		
16	COMPRø	COMPR ₁	COMPR ₂	COMPR ₃		
18				MIVR		
1A				LVR		
1C						
1E						
20	CPRLØ	CPR _{L1}	CPR _{L2}	CPR _{L3}		
22	CPRHØ	CPR _{H1}	CPR _{H2}	CPR H3		
24	SPRLØ	SPR _{L1}	SPR _{L2}	SPR L3		
26	SPRHØ	SPR _{H1}	SPR H2	SPR H3		
28	DPRLØ	DPR 11	DPR L2	DPR L3		
2 A	DPRHØ	DPR _{H1}	DPR H2	DPR H3		
2C	TTPRLØ	TTPR _{L1}	TTPR _{L2}	TTPR L3		
2E	TTPRHØ	TTPR _{H1}	TTPR _{H2}	TTPR H3		
30	LPR _{IØ}	LPR _{L1}	LPR _{L2}	LPR _{L3} /MTPR _L		
32	LPRHØ	LPR _{H1}	LPR _{H2}	LPR _{H3} /MTPR _H		
34				110		
36						
38	BCRLØ	BCR _{L1}	BCR _{L2}	BCR _{L 3}		
3A	BCRHO	BCR _{H1}	BCR _{H2}	BCR _{H3}		
3C	CCRIØ	CCR _I 1	CCR _{1.2}	CCR ₁₃		
3E	CCRHØ	CCR _{H1}	CCR _{H2}	CCR _{H3}		

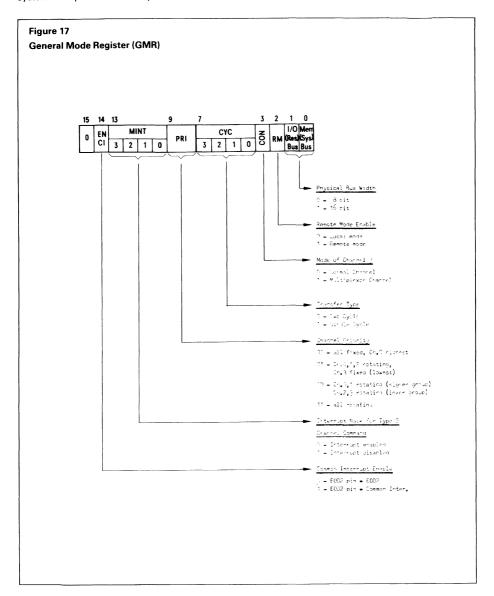
GCR	= General Command Register	MIVR	= Multiplexor Interrupt Vector Register
SCR	= Subchannel Register	LVR	= Last Vector Register
GSR	= General Status Register	CPR	= Command Pointer Register
GMR	= General Mode Register	SPR	= Source Pointer Register
GBR	= General Burst Register	DPR	= Destination Pointer Register
GDR	= General Delay Register	TTPR	= Translate Table Pointer Register
CSR	= Channel Status Register	LPR	= List Pointer Register
DAR	= Data Assembly Register	MTPR	= Multiplexer Table Pointer Register
MASKR	= Mask Register	BCR	= Byte Count Register
COMPR	= Compare Register	CCR	= Channel Command Register

Register Description

General Mode Register

In the General Mode Register GMR (figure 17) the system wide parameters are specified.

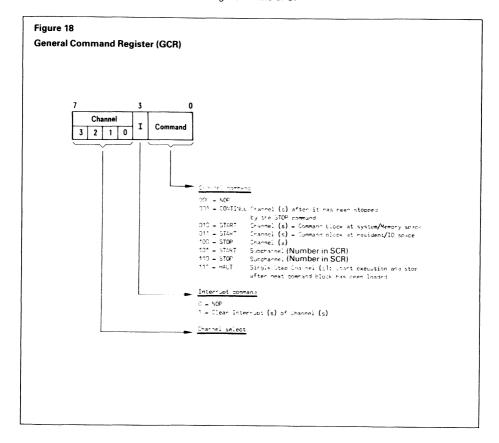
This register should be programmed first after reset.



General Command Register

Individual channels are started and stopped by a command written to the General Command Register

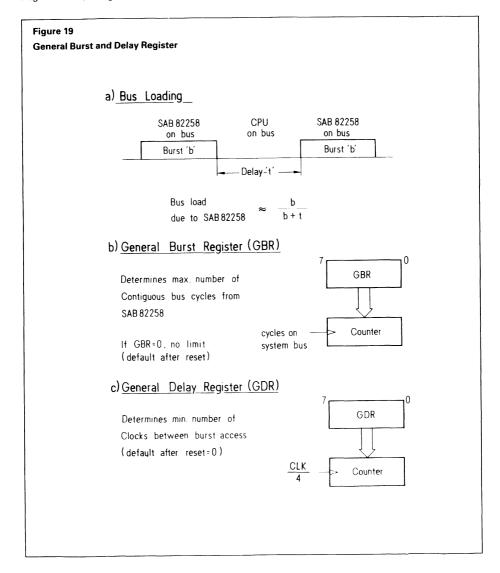
GCR (figure 18). The GCR is directly loaded by the CPU.



General Burst and Delay Register

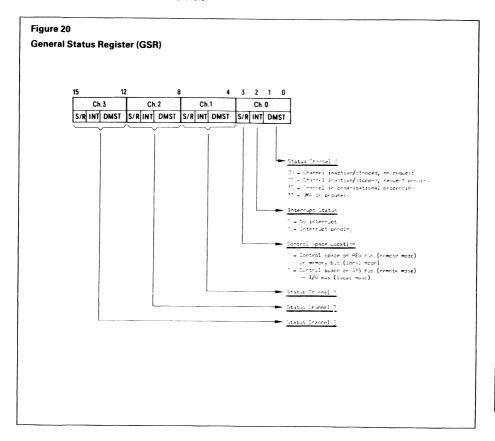
It is possible to restrict the bus load generated by SAB 82258 on the CPU bus by programming the burst and the delay register. The bus load is defined by the formula given in figure 19a. The factor b (burst) is programmed in the General Burst Register GBR, t (delay time) in the General Delay Register GDR (see figure 19b and c).

Since SAB 82258 can also execute locked bus cycles, the maximum burst length consists of b+3 (8 bit bus) or b+2 (16 bit bus) bus cycles. GBR and GDR must be directly loaded by the CPU. Loading GBR with 0 leads to no bus load limitations for SAB 82258 (default after reset).



General Status Register

The General Status Register GSR (figure 20) shows the current states of all the channels.



Channel Commands

The channel commands are contained in the channel command block (figure 12). Up to 22 bits are used to specify the command. There are two types of channel commands:

- Type 1: for data movement
- Type 2: for command chaining control

The command block for a Type 1 command is in general 26 bytes long (see figure 12).

For certain type 1 transfers which, for example, do not use "on-the-fly" match, translate or verify feature, the command is only 16 bits long and only a short command block is necessary (see figure 12).

The Type 1 command fields (see figures 21 and 22) contain information on:

- a. Bus width of source and destination
- b. If source and/or destination address should be incremented or decremented or kept constant during the transfer
- c. If source/destination is in memory or I/O space (local mode) or in system or I/O space (remote mode)
- d. If data chaining (list or linked-list) is to be performed
- e. If the data transfer is synchronized (source or destination)
- f. If an "on-the-fly" match operation and/or translate operation has to be performed
- g. If a verify operation has to be performed.

Type 2 command blocks are 6 bytes long (see figure 23) of which the first 2 bytes form the command and the rest is either a relative displacement or an absolute address for the JUMP operation. There are 2 basic type 2 commands (figure 23):

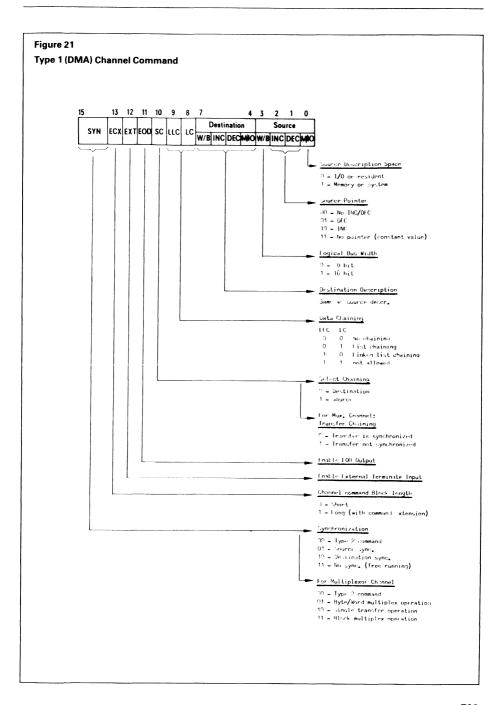
a. JUMP – conditional and non-conditional b. STOP – conditional and non-conditional

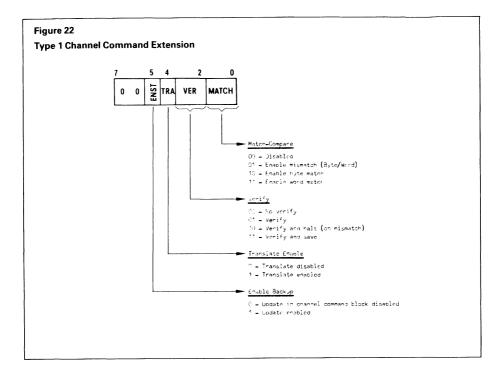
The conditional case tests for either of the 4 condition bits which are altered at the termination of any DMA operation:

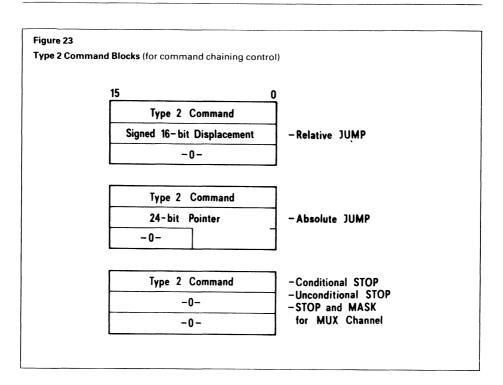
- Termination due to byte count end
- Termination due to mask-compare
- Termination due to external terminate
- Verify operation resulting in mismatch.

It is thus possible to JUMP or STOP further execution of commands based on any of these conditions and optionally generate EOD or interrupt signal

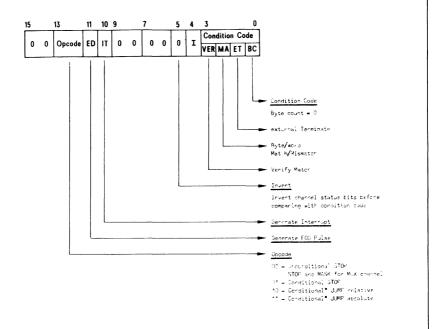
The combination of type 1 and 2 commands gives SAB 82258 a high degree of "programmability". It can thus execute quite complex algorithms with a fairly low demand for CPU service.







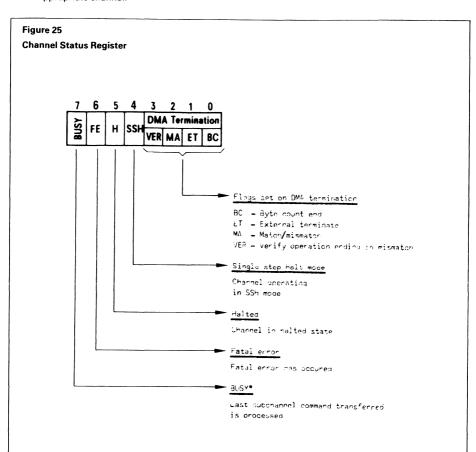




*) Unconditional JUMP when all condition code bits are set 1.

Channel Status Register

For each channel exists a Channel Status Register (see figure 25). This register shows the current state of the appropriate channel.



^{*)} Valid only for channel 3 in multiplexer mode. In all other cases 0 is returned.

Multiplexer Channel Registers

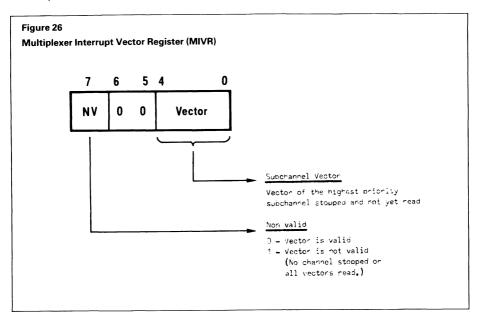
These registers are valid only for channel 3 if programmed as multiplexer channel.

Multiplexer Table Pointer Register (MTPR)

This 24 bit register is used to reference the multiplexer table in memory (see figure 14b). It must be loaded by the CPU. Physically the List Pointer Register is used, since data chaining is not allowed for multiplexer channel.

Multiplexer Interrupt Vector Register

This 8 bit register is read by the CPU to determine which channels are stopped. The vectors of the stopped subchannels are output on subsequent read operations in order of their priority (0 has highest priority).



Last Vector Register (LVR)

This 8 bit register holds the last vector read by SAB 82258 (from SAB 8259A). In case of a stop caused by a fatal error on channel 3, LVR determines the failing subchannel.

Subchannel Register

This 8 bit register must be loaded by the CPU with the desired subchannel number before a subchannel command is written into GCR.

Timings

The bus timings in 286 and Remote mode are identical to that for SAB 80286, in the 186 and 8086 mode the timings are identical to that for SAB 80186. For exact timings see timing diagrams of A.C. Characteristics.

Asynchronous control inputs are specified with setup and hold times which are only meaningful to determine whether the SAB 82258 responds to the signal in the current cycle or the next cycle.

Absolute Maximum Ratings¹⁾

Temperature Under Bias 0 to 70° C Storage Temperature -65 to $+150^{\circ}$ C Voltage on Any Pin with Respect to Ground -1 to +7V Power Dissipation 3.6W

D.C. Characteristics²⁾

 $TA = 0 \text{ to } 70^{\circ}\text{C}; VCC = +5 \pm 10\%$

Symbol	Parameter	Lim	Limit Values		Test Conditions
		Min.	Max.		
VIL	Input Low Voltage (except CLK)	-0.5	+0.8		
VIH	Input High Voltage (except CLK)	2.0	VCC+0.5	V	-
VOL	Output Low Voltage	-	0.45		IOL = 3.0 mA
VOH	Output High Voltage	2.4	_		$IOH = -400 \mu A$
ICC	Power Supply Current		450	mA	TA = 25°C, all outputs open
ILI	Input Leakage Current				0V ≤ VIN ≤ VCC
	SO, S1, S2, BHE, RD, WR, M/IO		-200	μΑ	
	HOLD (RQ/GT mode), EOD		- 1.5	mA	
	other pins		10		
ILO	Output Leakage Current		± 10	μΑ	0.45V ≤ VOUT ≤ VCC
VCL	Clock Input Low Voltage	-0.5	+0.6	.,	
VCH	Clock Input High Voltage	3.8	VCC+1.0	V	-
CIN	Capacitance of Inputs (except CLK)		10		
СО	Capacitance of I/O or Outputs	_	20	pF	fc = 1 MHz
CCLK	Capacitance of CLK Input		12		

¹⁾ Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

²⁾ Clock must be applied.

A.C. Characteristics

TA = 0 to +70°C; VCC = $+5V \pm 10\%$ Any output timing is measured at 1.5V.

Symbol	Parameter	Lim	nit Values	Units	Test Conditions
		Min.	Max.		
1	CLK Cycle Period	62.5	250		_
2	CLK Low Time	15	230		at 0.6V
3	CLK High Time	20	235		at 3.2V
4	Output Delay	0	60		CL = 125 pF
5	Output Delay	U	40	}	CL = 125 pr
6	DATA Setup Time	10		7	
7	DATA Hold Time	5			_
8	READY Setup Time	38.5			
9	READY Hold Time	25]-		
10	Input Setup Time	20		ns	
11	Input Hold Time	20			
12	Address Set Up	2.5			
13	Output Delay	0	50]	
14	Delay to Float	-	60		
15	Chip Select Set Up	60		7	
16	Command Length	290			0 MUI- O
17	Data Set Up	165	_		at 8 MHz Operation
18	Address Set Up	80			-
19	Command Inactive	290			at 8 MHz Operation
19a	Access Time	-	320	7	at 6 Winz Operation

A.C. Characteristics (continued)

Symbol	Parameter	Limit	Values	Units	Test Conditions
		Min.	Max.		

CLK Timing for 186 Mode

20	CLK Period	125	125 500		
21	CLK Low Time	55			-
22	CLK High Time	33		ns	
23	CLK Rise Time		15	7	1.0 to 3.5V
24	CLK Fall Time		13		3.5 to 1.0V

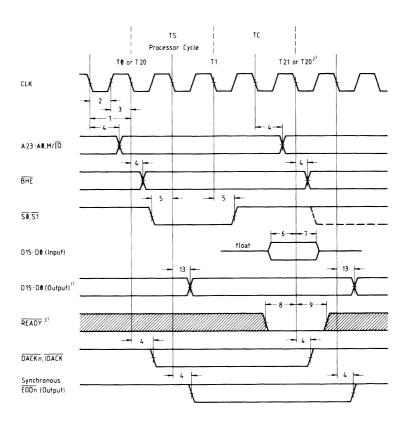
Ready Timing for 186 Mode

25	Ready Active Set Up Time	20			_
26	Ready Hold Time	10			
27	Ready Inactive Set Up Time	35			
28	Set Up Time	20			
29	Hold Time	0		ns	
30	Data Delay	10	50		
31	Status Delay		55		
32	Delay to Float		50		

Asynchronous inputs are specified with setup and hold times which are only intended for determination of whether the SAB 82258 responds to the signal in the current cycle or the next cycle.

Waveforms

Figure 27
Timing of an Active Bus Cycle (286 mode)



Note 1: D15-DØ floats during Single Cycle Transfer like a Read Cycle.

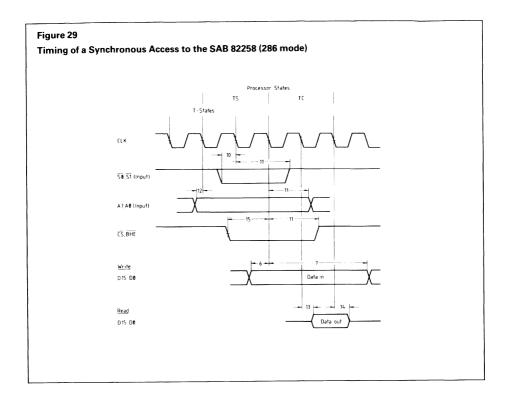
Note 2: T2 will be repeated, if READY is inactive.

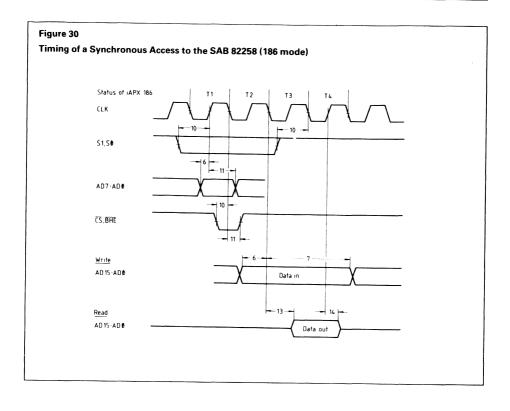
n *** T**3⁴⁾ Т1 CLK ALE 31 -l 31 |-\$2, \$1, \$Ø -30 H AD19/S6-AD16/S3 Address S6-S3 - 30 |-BHE -30 -- 321 - 6 -AD15 - ADØ Address Datain DT/R Read Bus Cycle DEN RD (out) 30 ⊦ AD15 ~ ADØ 31 X Address Data out 461-Write DEN 31 Bus Cycle WR (out) - 6 AD15 - ADØ DT/R IOACK Bus Cycle DEN IOACK DACKn Synchronous EODn (Output)

Figure 28
Timing of an Active Bus Cycle (186 mode)

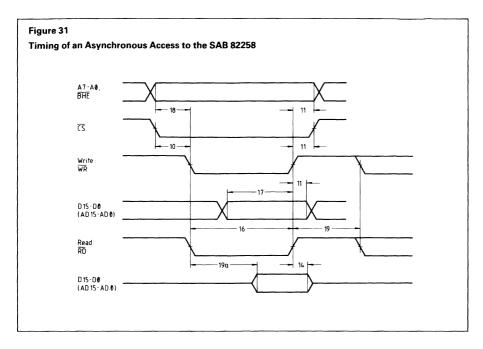
Note 3: For a Single Cycle Transfer the timing of AD15-AD0, $\overline{\text{DEN}}$ and DT/ $\overline{\text{R}}$ is the same as in a Read Bus Cycle.

Note 4: Additional T3 cycles will be inserted if bus is not ready (see fig. 32).





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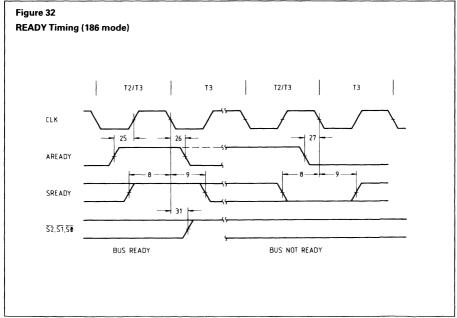
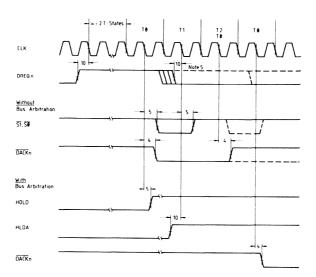
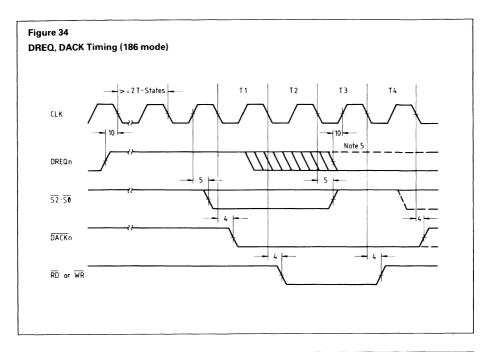


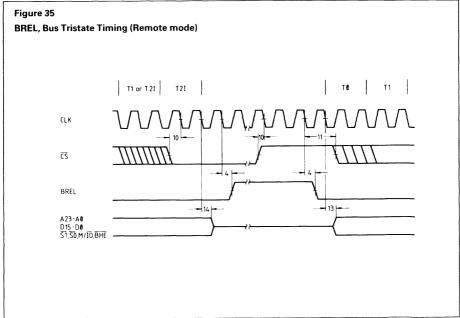
Figure 33
DREQ, DACK Timing (286 mode)

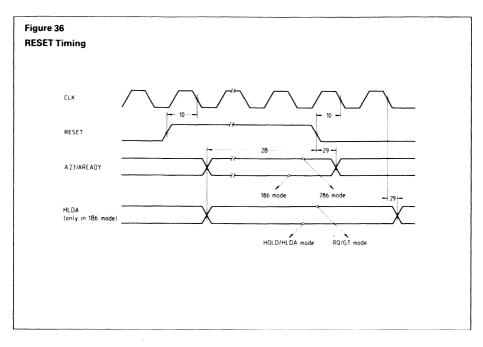


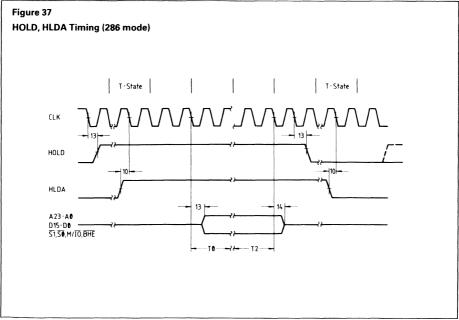
Note 5: The trailing edge of DREQn, as specified in this diagram, is necessary if only one bus cycle should be executed.

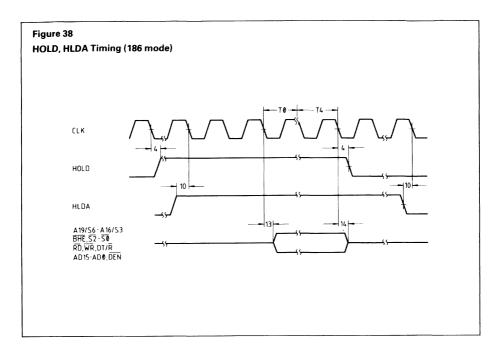
A later trailing edge may cause an additional bus cycle (continuous DREQ), if no READY-wait-states are inserted.

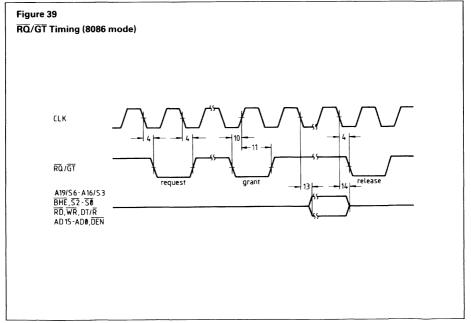


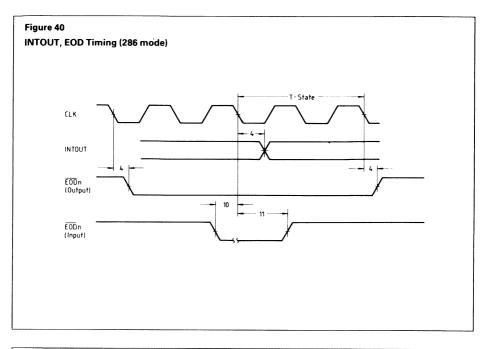


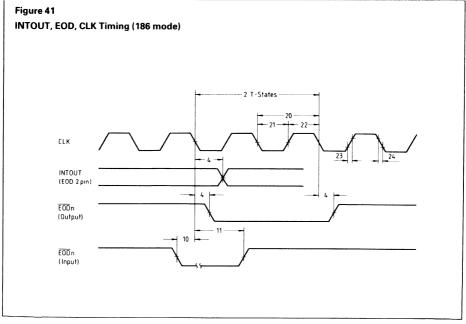




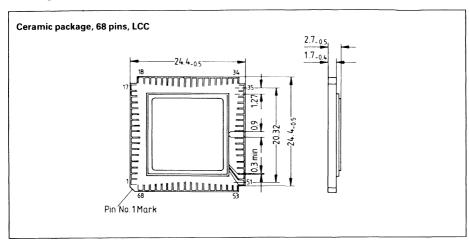








Package Outline



SAB 82258 is packaged in a 68-pin, leadless JEDEC type A hermetic chip carrier.

Ordering Information

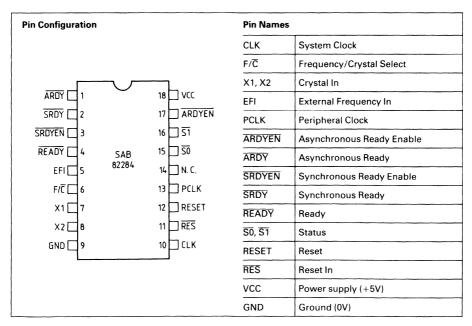
Туре	Description	Ordering code
SAB 82258-C	Advanced DMA Controller	Q67120-P122

Preliminary

SAB 82284 Clock Generator and Ready Interface for SAB 80286 Processors

SAB 82284 up to 16 MHz

- Generates system clock for SAB 80286 processors
- Uses crystal or TTL signal for frequency source
- Provides local READY and multimaster system bus READY synchronization
- 18-pin package
- Single +5V power supply
- Generates system reset output from Schmitt-trigger input



The SAB 82284 is a bipolar clock generator/driver which provides clock signals for SAB 80286 processors and support components. It also contains logic to supply READY to the CPU from either

asynchronous or synchronous sources and synchronous RESET from an asynchronous input with hysteresis.

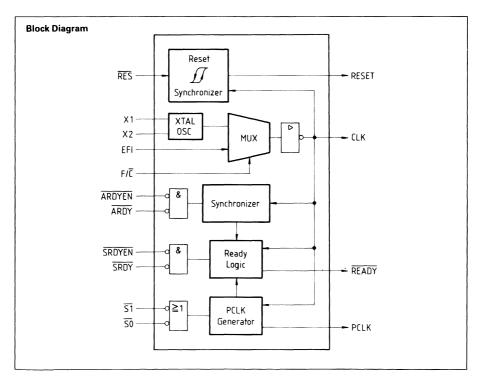
1.85

Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function		
ARDY	1	I	ASYNCHRONOUS READY is an active low input used to terminate the current bus cycle. The ARDY input is qualified by ARDYEN. Inputs to ARDY may be applied asynchronously to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs.		
SRDY	2	1	SYNCHRONOUS READY is an active low input used to terminate the current bus cycle. The SRDY input is qualified by the SRDYEN input. Setup and hold times must be satisfied for proper operation.		
SRDYEN	3	ı	SYNCHRONOUS READY ENABLE is an active low input which qualifies SRDY. SRDYEN selects SRDY as the source for READY to the CPU for the current bus cycle. Setup and hold times must be satisfied for proper operation.		
READY	4	0	READY is an active low output which signals the current bus cycle is to be completed. The SRDY, SRDYEN, ARDY, ARDYEN, S1, S0 and RES inputs control READY as explained later in the READY generator section. READY is an open collector output requiring an external 300 ohm pullup resistor.		
EFI	5	1	EXTERNAL FREQUENCY IN drives CLK when the F/C input is strapped high. The EFI input frequency must be twice the desired internal processor clock frequency.		
F/C	6	ı	FREQUENCY/CRYSTAL SELECT is a strapping option to select the source for the CLK output. When F/C is strapped low, the internal crystal oscillator drives CLK. When F/C is strapped high, the EFI input drives the CLK output.		
X1, X2	7, 8	ı	CRYSTAL IN are the pins to which a parallel resonant fundamental mode crystal is attached for the internal oscillator. When F/\overline{C} is low, the internal oscillator will drive the CLK output at the crystal frequency. The crystal frequency must be twice the desired internal processor clock frequency.		
CLK	10	0	SYSTEM CLOCK is the signal used by the processor and support devices which must be synchronous with the processor. The frequency of the CLK output has twice the desired internal processor clock frequency. CLK can drive both TTL and MOS level inputs.		
RES	11	1	RESET IN is an active low input which generates the syster reset signal RESET. Signals to RES may be applied asynchronously to CLK. A Schmitt-trigger input is provided RES, so that an RC circuit can be used to provide a time desetup and hold times are given to assure a guaranteed response to synchronous inputs.		
RESET	12	0	RESET is an active high output which is derived from the RES input. RESET is used to force the system into an initial state. When RESET is active, READY will be active (low).		

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
PCLK	13	0	PERIPHERAL CLOCK is an output which provides a 50% duty cycle clock with 1/2 the frequency of CLK. PLCK will be in phase with the internal processor clock following the first bus cycle after the processor has been reset.
S0, S1	15,16	l	STATUS inputs prepare the SAB 82284 for a subsequent bus cycle. \$\overline{SO}\$ and \$\overline{ST}\$ synchronize PCLK to the internal processor clock and control \$\overline{READY}\$. These inputs have pullup resistors to keep them high if nothing is driving them. Setup and hold times must be satisfied for proper operation.
ARDYEN	17		ASYNCHRONOUS READY ENABLE is an active low input which qualifies the ARDY input. ARDYEN selects ARDY as the source of ready for the current bus cycle. Inputs to ARDYEN may be applied asynchronously to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs.
VCC	18	-	POWER SUPPLY (+5V)
GND	9	-	GROUND (0 V)



Functional Description

Introduction

The SAB 82284 generates the clock, ready, and reset signals required for SAB 80286 processors and support components. The SAB 82284 is packaged in an 18-pin DIP package and contains a crystal-controlled oscillator, MOS clock generator, peripheral clock generator, Multibus ready synchronization logic, and system reset generation logic.

Clock generator

The CLK output provides the basic timing control for an SAB 80286 system. CLK has output characteristics sufficient to drive MOS devices. CLK is generated by either an internal crystal oscillator or an external source as selected by the F/\overline{C} strapping option. When F/\overline{C} is low, the crystal oscillator drives the CLK output. When F/\overline{C} is high, the EFI input drives the CLK output. The SAB 82284 provides a second clock output (PCLK) for peripheral devices. PCLK is CLK divided by two. PCLK has a duty cycle of 50% and TTL output drive characteristics. PCLK is normally synchronized to the internal processor clock. After reset, the PCLK signal may be out of phase with the internal processor clock. The $\overline{S1}$ and $\overline{S0}$ signals of the first bus cycle are used to synchronize PCLK to the internal processor clock. The phase of the PCLK output changes by extending its high time beyond one system clock (see waveforms). PCLK is

forced high whenever either $\overline{S0}$ or $\overline{S1}$ were active (low) for the two previous CLK cycles. PCLK continues to oscillate when both $\overline{S0}$ and $\overline{S1}$ are high.

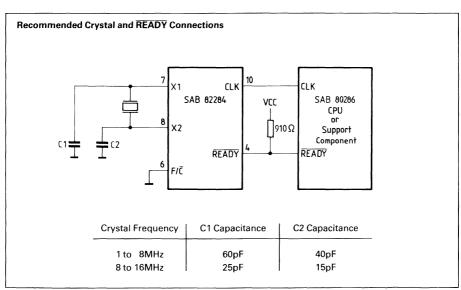
Since the phase of the internal processor clock will not change except during reset, the phase of PCLK will not change except during the first bus cycle after reset.

Oscillator

The oscillator circuit of the SAB 82284 is a linear Pierce oscillator which requires an external, parallel, resonant, fundamental-mode crystal. The output of the oscillator is internally buffered. The crystal frequency chosen should be twice the required internal processor clock frequency. The crystal should have a typical load capacitance of 32 pF.

X1 and X2 are the oscillator crystal connections. For stable operation of the oscillator, two loading capacitors are recommended, as shown in the figure below. The sum of the board capacitance and loading capacitance should equal the values shown. It is advisable to limit stray board capacitances (not including the effect of the loading capacitors or crystal capacitance) to less than 10pF between the X1 and X2 pins.

Decouple VCC and GND as close to the SAB 82284 as possible.



Reset Operation

The reset logic provides the RESET output to force the system into a known initial state. When the $\overline{\text{RES}}$ input is active (low), the RESET output becomes active (high). $\overline{\text{RES}}$ is synchronized internally at the falling edge of CLK before generating the RESET output (see waveforms). Synchronization of the $\overline{\text{RES}}$ input introduces a one or two CLK delay before affecting the RESET output.

At power up, a system does not have a stable VCC and CLK. To prevent spurious activity, RES should be asserted until VCC and CLK stabilize at their operating values. SAB 80286 processors and support components also require their RESET inputs be high a minimum number of CLK cycles. An RC network, as shown below, will keep RES low long enough to satisfy both needs.

A Schmitt-trigger input with hysteresis on RES assures a single transition of RESET with an RC circuit on RES. The hysteresis separates the input voltage level at which the circuit output switches from high to low from the input voltage level at which the circuit output switches from low to high. The RES high to low input transition voltage is lower than the RES low to high input transition voltage. As long as the slope of the RES input voltage remains in the same direction (increasing or decreasing) around the RES input transition voltage, the RESET output will make a single transition.

Ready Operation

The SAB 82284 accepts two ready sources for the system ready signal which terminates the current bus cycle. Either a synchronous (SRDY) or asynchronous ready (ARDY) source may be used. Each ready input has an enable (SRDYEN and ARDYEN) for selecting the type of ready source

required to terminate the current bus cycle. An address decoder would normally select one of the enable inputs.

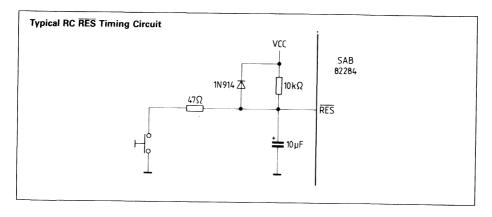
The figure on synchronous ready mode illustrates the operation of SRDY and SRDYEN. These inputs are sampled on the falling edge of CLK when \$1 and \$0 are inactive and PCLK is high. READY is forced active when both \$RDY and \$RDYEN are sampled as low.

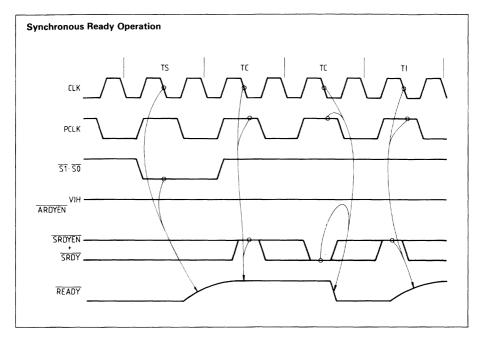
The figure on asynchronous ready mode shows the operation of ARDY and ARDYEN. These inputs are sampled by an internal synchronizer at each falling edge of CLK. The output of the synchronizer is then sampled when PCLK is high. If the synchronizer resolved both the ARDY and ARDYEN inputs to have been active (low), READY becomes active (low) and the SRDY and SRDYEN inputs are ignored.

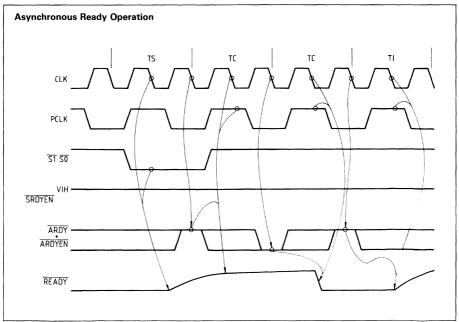
READY remains active until either \$\overline{51}\$ or \$\overline{50}\$ is sampled low, or the ready inputs are sampled as inactive

READY is enabled (low), if either SRDY + SRDYEN = 0 or ARDY + ARDYEN = 0 when sampled by the SAB 82284 READY generation logic. READY will remain active for at least two CLK cycles.

The READY output has an open-collector driver allowing other ready circuits to be wire-ORed with it. The READY signal of an SAB 80286 system requires an external 300 ohm pullup resistor. To force the READY signal inactive (high) at the start of a bus cycle, the READY output floats when either \$\overline{3}\$T or \$\overline{3}\$0 are sampled low at the falling edge of CLK. Two system clock periods are allowed for the pullup resistor to pull the READY signal to VIH. When RESET is active, READY is forced active one CLK later (see waveforms).







Absolute Maximum Ratings 1)

Temperature under bias	0 to 70°C
Storage temperature	-65 to +150°C
All output and supply voltages	−0.5 to +7V
All input voltages	-1.0 to +5.5V
Power dissipation	1 W

DC Characteristics

TA = 0 to $70^{\circ}C$, $VCC = 5 V \pm 10\%$

Combal	Power and a second	Limit	values	11-14	Test condition	
Symbol	Parameter	min.	max.	Unit	rest condition	
IF	Forward input current		-0.5	mA	VF = 0.45V	
IR	Reverse input current	_	50	μА	VR = VCC	
VC	Input forward clamp voltage		-1.0	v	IC = -5mA	
ICC	Power supply current		145	mA		
VIL	Input low voltage		0.8		-	
VIH	Input high voltage	2.0	-			
VOL, VCL	Output low voltage	_	0.45		IOL = 5mA (7mA at READY)	
VCH	CLK output high voltage	4.0		v	_	
VOH	Output high voltage	2.4	1		IOH = - 800 μA	
VIHR	RES input high voltage	2.6	-			
VIHR – VILR	VILR RES input hysteresis		1		fC = 1 MHz	
CI	Input capacitance	-	10	pF		

Stresses above those listed under "absolute maximum ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC Characteristics

TA = 0 to $70^{\circ}C$, $VCC = 5V \pm 10\%$

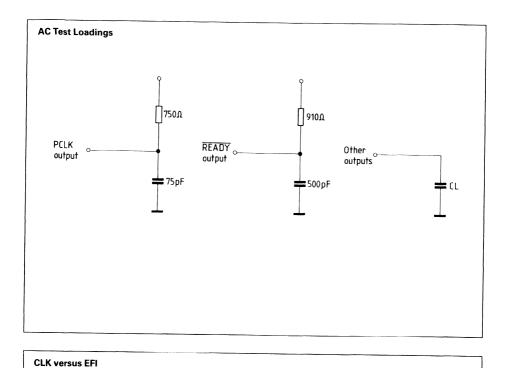
	D		Lim	it values	Unit	T
Symbol	Parameter		min.	max.	Unit	Test condition
T1	EFI to CLK delay		_	30		
T2	EFI low time	EFI low time				at 1.5 V
Т3	EFI high time		25]		CL = 150 pF IOL = 5 mA
T4	CLK period		62	500		
T5	CLK low time		15		at 1.0 V see 1)	
T6	CLK high time		25			at 3.6 V
T7	CLK rise time	_	10		from 1.0 V to 3.6 V see 2)	
T8	CLK fall time]_			from 3.6 V to 1.0 V	
T9	Status setup time		22.5			
T10	Status hold time SRDY + SRDYEN setup time		1]	ns	
T11			15			
T12	SRDY + SRDYEN hold time		0	_		at 0.8 V and 2.0 V on input and 0.8 V on CLK
T13	ARDY + ARDYEN setup time	4)				
T14	ARDY + ARDYEN hold time	4)	30			
T15	RES setup time	4)	20			
T16	RES hold time	4)	10			
T17	READY inactive delay		5			at $0.8 \text{V R} = 910 \Omega$
T18	READY active delay		0	24		CL = 150 pF IOL = 7 mA
T19	PCLK delay			45		at 0.8 V on CLK to see 3)
T20	RESET delay		5	34		0.8 V or 2.0 V on output
T21	PCLK low time	PCLK low time				at 0.6 V see 3)
T22	PCLK high time		T4- 20	-		at 2.0 V

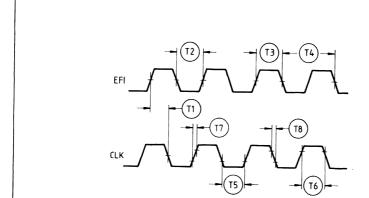
¹⁾ CL = 150 pF, IOL = 5 mA. With either the internal oscillator with the recommended crystal and load, or with the EFI input meeting specifications T2 and T3.

 $^{^{2)}}$ CL = 150 pF, IOL = 5 mA

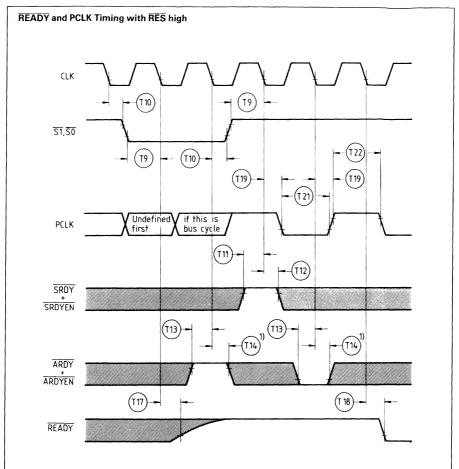
 $^{^{3)}}$ CL = 75 pF, R = 750 Ω at PCLK output

⁴⁾ This is an asynchronous input. This specification is given for testing purposes only, to assure recognition at a specific clock edge.

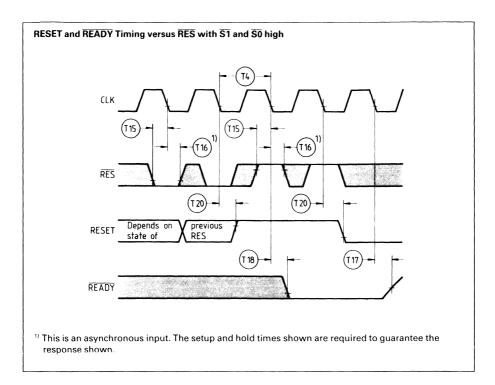




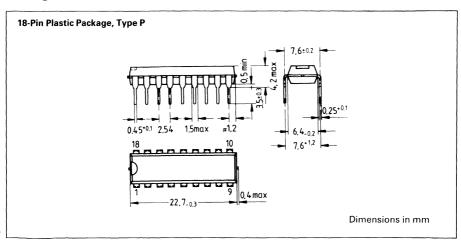
The EFI input low and high times as shown are required to guarantee the CLK low and high times shown.



¹⁾ This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.



Package Outline



SAB 82284

Ordering Information

Туре	Description	Ordering Code
SAB 82284-P	Clock generator (plastic package) up to 16 MHz	Q67020-Y162



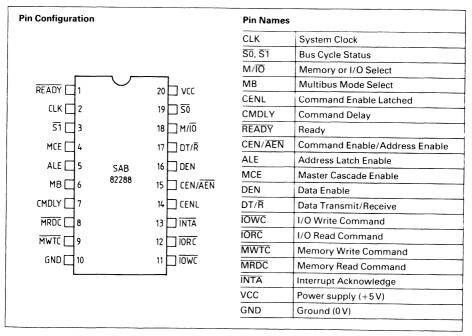
SAB 82288 Bus Controller for SAB 80286 Processors

SAB 82288 up to 16 MHz

- Provides commands and control for local and system bus
- Offers wide flexibility in system configurations
- · Flexible command timing

SAB 82288-6 up to 12 MHz

- Optimal Multibus -compatible timing
- Control drivers with 16 mA IOL and tristate command drivers with 32 mA IOL
- Single +5 V supply



The SAB 82288 bus controller is a 20-pin MYMOS component for use in SAB 80286 microsystems. The bus controller provides command and control outputs with flexible timing options. Separate command outputs are used for memory and I/O

devices. The data bus is controlled with separate data enable and direction control signals. Two modes of operation are possible via a strapping option: Multibus-compatible bus cycles, and high-speed bus cycles.

Multibus (1) is a trademark of Intel Corporation.

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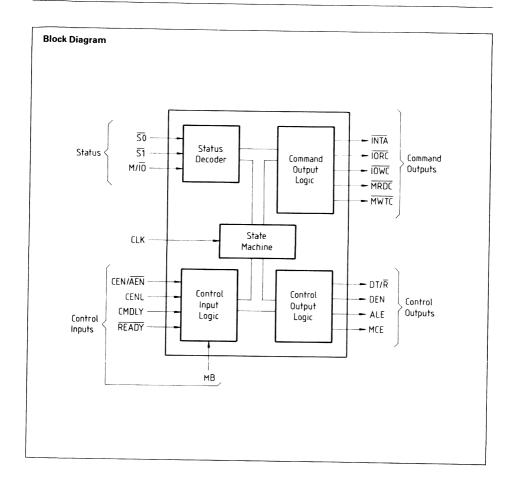
Pin Defin	itions and	Functions					
Symbol	Pin	Input (I) Output (O)	Function				
READY	1	I	READY indicates the end of the current bus cycle. READY is an active low input. Multibus mode requires at least one wait state to allow the command outputs to become active. READY must be low during reset, to force the SAB 82288 into the idle state. Setup and hold times must be met for proper operation.				
CLK	2	I	SYSTEM CLOCK provides the basic timing control for the SAB 82288 in an SAB 80286 microsystem. Its frequency is twice the internal processor clock frequency. The falling edge of this input signal establishes when inputs are sampled and control outputs change.				
S0, S1	3, 19	I	BUS CYCLE STATUS starts a bus cycle and, along with M/\overline{IO} , defines the type of bus cycle. These inputs are active low. A bus cycle is started when either $\overline{S1}$ or $\overline{S0}$ is sampled low at the falling edge of CLK. These inputs have pullups sufficient to hold them high when nothing drives them. Setup and hold times must be met for proper operation.				
			SAB 80286 bus cycle status definition				
			M I O S1 S0 Type of bus cycle				
			0 0 0 Interrupt acknowledge 0 0 1 I/O read 0 1 0 I/O write 0 1 1 None; idle 1 0 0 Halt or shutdown 1 0 1 Memory read 1 1 0 Memory write 1 1 1 None; idle				
MCE	4	0	MASTER CASCADE ENABLE signals that a cascade address from a master SAB 8259A interrupt controller may be placed onto the CPU address bus for latching by the address latches under ALE control. The CPU's address bus may then be used to broadcast the cascade address to slave interrupt controllers so only one of them will respond to the interrupt acknowledge cycle. This control output is active high. MCE is only active during interrupt acknowledge cycles and is not affected by any control input. Using MCE to enable cascade address drivers requires latches which save the cascade address on the falling edge of ALE.				
ALE	5	0	ADDRESS LATCH ENABLE controls the address latches used to hold an address stable during a bus cycle. This control output is active high. ALE will not be issued for the halt bus cycle and is not affected by any of the control inputs.				
МВ	6	I	MULTIBUS MODE SELECT determines timing of the command and control outputs. When high, the bus controller operates in Multibus mode. When low, the bus controller optimizes the command and control output timing for short bus cycles. The function of the CEN/AEN input pin is selected by this signal. This input is intended to be a strapping option and not dynamically changed. This input may be connected to VCC or GND.				

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
CMDLY	7	1	COMMAND DELAY allows delaying the start of a command. CMDLY is an active high input. If sampled high, the command output is not activated and CMDLY is again sampled at the next CLK cycle. When sampled low the selected command is enabled. If READY is detected low before the command output is activated, the SAB 82288 will terminate the bus cycle, even if no command was issued. Setup and hold times must be satisfied for proper operation. This input may be connected to GND if no delays are required before starting a command.
MRDC	8	0	MEMORY READ COMMAND instructs the memory device to place data onto the data bus. This command output is active low. The MB and CMDLY inputs control when this output becomes active. READY controls when it becomes inactive.
MWTC	9	0	MEMORY WRITE COMMAND instructs a memory device to read the data on the data bus. This command output is active low. The MB and CMDLY inputs control when this output becomes active. READY controls when it becomes inactive.
IOWC	11	0	I/O WRITE COMMAND instructs an I/O device to read the data on the data bus. This command output is active low. The MB and CMDLY inputs control when this output becomes active. READY controls when it becomes inactive.
IORC	12	0	I/O READ COMMAND instructs an I/O device to place data onto the data bus. This command output is active low. The MB and CMDLY inputs control when this output becomes active. READY controls when it becomes inactive.
INTA	13	0	INTERRUPT ACKNOWLEDGE tells an interrupting device that its interrupt request is being acknowledged. This command output is active low. The MB and CMDLY inputs control when this output becomes active. READY controls when it becomes inactive.
CENL	14	1	COMMAND ENABLE LATCHED is a bus controller select signal which enables the bus controller to respond to the current bus cycle being initiated. CENL is an active high input latched internally at the start of each bus cycle. CENL is used to select the appropriate bus controller for each bus cycle in a system where the CPU has more than one bus it can use. This input may be connected to VCC to select this SAB 82288 for all transfers. No control inputs affect CENL. Setup and hold times must be met for proper operation.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function	
CEN/ĀĒN	15		COMMAND ENABLE/ADDRESS ENABLE controls the command and DEN outputs of the bus controller. CEN/AEN inputs may be asynchronous to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs. This input may be connected to VCC or GND. When MB is high this pin has the AEN function. AEN is an active low input which indicates that the CPU has been granted use of a shared bus and the bus controller command outputs may exit tristate off and become inactive (high). AEN high indicates that the CPU does not have control of the shared bus and forces the command outputs into tristate off and DEN inactive (low). AEN would normally be controlled by an SAB 82289 bus arbiter which activates AEN when that arbiter owns the bus to which the bus controller is attached. When MB is low this pin has the CEN function. CEN is an unlatched active high input which allows the bus controller activate its command and DEN outputs. With MB low, CEN low forces the command and DEN outputs inactive but does not tristate them.	
DEN	16	0	DATA ENABLE controls when data transceivers connected to the local data bus should be enabled. DEN is an active high control output. DEN is delayed for write cycles in the Multibus mode.	
DT/R	17	0	DATA TRANSMIT/RECEIVE establishes the direction of data flow to or from the local data bus. When high, this control output indicates that a write bus cycle is being performed. A low indicates a read bus cycle. DEN is always inactive when DT/R changes states. This output is high when no bus cycle is active. DT/R is not affected by any of the control inputs.	
M/ĪŌ	18	1	MEMORY or I/O SELECT determines whether the current bu cycle is in the memory space or I/O space. When low, the current bus cycle is in the I/O space. Setup and hold times must be met for proper operation.	
VCC	20	-	POWER SUPPLY (+5V)	
GND	10	-	GROUND (0 V)	



Functional Description

Introduction

The SAB 82288 bus controller is used in SAB 80286 systems to provide address latch control, data transceiver control, and standard level-type command outputs. The command outputs are timed and have sufficient drive capabilities for large TTL buses and meet all IEEE-796 requirements for Multibus. A special Multibus mode is provided to statisfy all address/data setup and hold time requirements. Command timing may be tailored to special needs via a CMDLY input to determine the start of a command and READY to determine the end of a command.

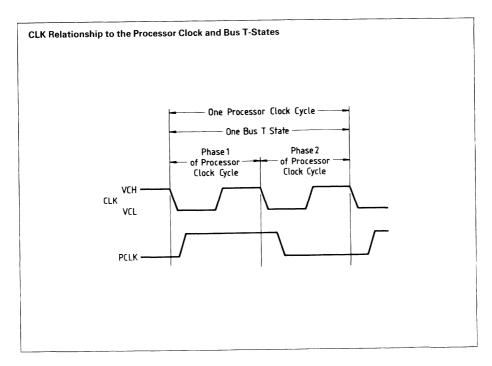
Connection to multiple buses is supported with a latched enable input (CENL). An address decoder can determine which, if any, bus controller should be enabled for the bus cycle. This input is latched to allow an address decoder to take full advantage of the pipelined timing on the SAB 80286 local bus.

Buses shared by several bus controllers are supported. An AEN input prevents the bus controller from driving the shared bus command and data signals except when enabled by an external bus arbiter such as the SAB 82289.

Separate DEN and DT/R outputs control the data transceivers for all buses. Bus contention is eliminated by disabling DEN before changing DT/R. The DEN timing allows sufficient time for tristate bus drivers to enter tristate off before enabling other drivers onto the same bus. The term CPU refers to any SAB 80286 processor or SAB 80286 support component which may become an SAB 80286 local bus master and thereby drive the SAB 82288 status inputs.

Processor Cycle Definition

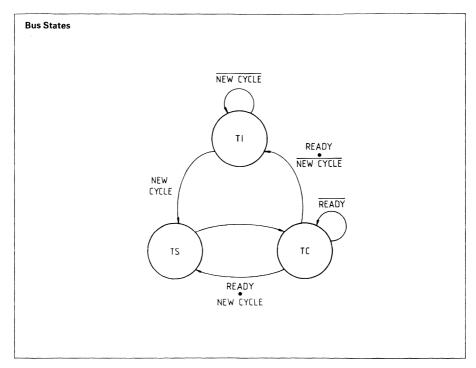
Any CPU which drives the local bus uses an internal clock which is one half the frequency of the system clock (CLK) (see figure below). Knowledge of the phase of the local bus master's internal clock is required for proper operation of the SAB 80286 local bus. The local bus master informs the bus controller of its internal clock phase when it asserts the status signals. Status signals are always asserted in phase 1 of the local bus master's internal clock.



Bus State Definition

The SAB 82288 bus controller has three bus states (see figure below): Idle (TI), Status (TS), and Command (TC). Each bus state is two CLK cycles long. Bus state phases correspond to the internal CPU processor clock phases.

The TI bus state occurs when no bus cycle is currently active on the SAB 80286 local bus. This state may be repeated indefinitely. When control of the local bus is being passed between masters, the bus remains in the TI state.



Bus Cycle Definition

The $\overline{S1}$ and $\overline{S0}$ inputs signal the start of a bus cycle. When either input becomes low, a bus cycle is started. The TS bus state is defined to be the two CLK cycles during which either $\overline{S1}$ or $\overline{S0}$ is active (see figure on bus cycle definition). These inputs are sampled by the SAB 82288 at every falling edge of CLK. When either $\overline{S1}$ or $\overline{S0}$ is sampled low, the next CLK cycle is considered the second phase of the internal CPU clock cycle.

The local bus enters the TC bus state after the TS state. The shortest bus cycle may have one TS state and one TC state. Longer bus cycles are formed by repeating TC states. A repeated TC bus state is called a wait state.

The READY input determines whether the current TC bus state is to be repeated. The READY input has the same timing and effect for all bus cycles. READY is sampled at the end of each TC bus state to see if it is active. If sampled high, the TC bus state is repeated. This is called inserting a wait state. The control and command outputs do not change during wait states.

When READY is sampled low, the current bus cycle is terminated. Note that the bus controller may enter the TS bus state directly from TC if the status lines are sampled active at the next falling edge of CLK.

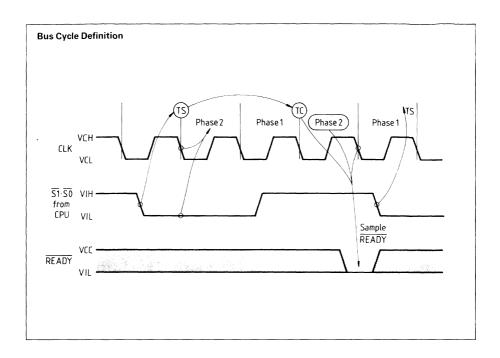


Table 2 Command and Control Output for Each Type of Bus Cycle

Type of bus cycle	M/IO	S1	<u>50</u>	Command activated	DT/R̄ state	ALE, DEN issued?	MCE issued?
Interrupt acknowledge	0	0	0	INTA	low	yes	yes
I/O read	0	0	1	IORC	low	yes	no
I/O write	0	1	0	IOWC	high	yes	no
None; idle	0	1	1	none	high	no	no
Halt/shutdown	1	0	0	none	high	no	no
Memory read	1	0	1	MRDC	low	yes	no
Memory write	1	1	0	MWTC	high	yes	no
None; idle	1	1	1	none	high	no	no

Operating Modes

Two types of buses are supported by the SAB 82288: Multibus and non-Multibus. When the MB input is strapped high, Multibus timing is used. In Multibus mode, the SAB 82288 delays command and data activation to meet IEEE-796 requirements on address to command active and write data to command active setup timing. Multibus mode requires at least one wait state in the bus cycle since the command outputs are delayed. The non-Multibus mode does not delay any outputs and does not require wait states. The MB input affects the timing of the command and DEN outputs.

Command and Control Outputs

The type of bus cycle performed by the local bus master is encoded in the M/\overline{IO} , $\overline{S1}$, and $\overline{S0}$ inputs. Different command and control outputs are activated depending on the type of bus cycle. Table 2 indicates the cycle decoding done by the SAB 82288 and the effect on command, DT/ \overline{R} , ALE, DEN, and MCE outputs.

Bus cycles come in three forms: read, write, and halt. Read bus cycles include memory read, I/O read, and interrupt acknowledge. The timing of the associated read command outputs (MRDC, IORC, and INTA), control outputs (ALE, DEN, DT/R) and control inputs (CEN/AEN, CENL, CMDLY, MB, and READY) are identical for all read bus cycles. Read cycles differ only in which command output is

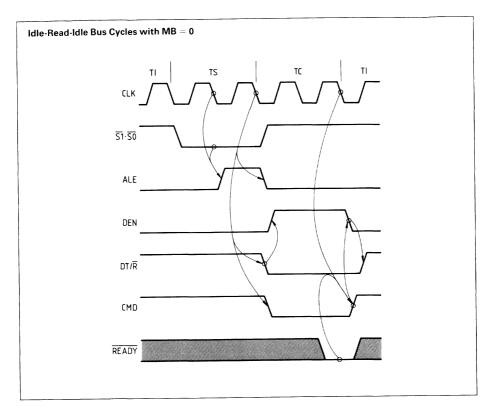
activated. The MCE control output is only asserted during interrupt acknowledge cycles.

Write bus cycles activate different control and command outputs with different timing than read bus cycles. Memory write and I/O write are write bus cycles whose timing for command outputs $(\overline{MWTC}$ and $\overline{IOWC})$, control outputs (ALE, DEN, DT/ \overline{R}) and control inputs (CEN/ \overline{AEN} , CENL, CMDLY, MB, and \overline{READY}) are identical. They differ only in which command output is activated.

Halt bus cycles are different because no command or control output is activated. All control inputs are ignored until the next bus cycle is started via $\overline{S1}$ and $\overline{S0}$.

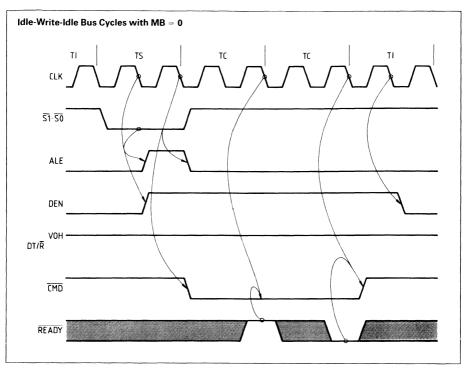
The basic command and control output timing for read and write bus cycles is shown in the next five figures. Halt bus cycles are not shown since they activate no outputs. The basic idle-read-idle and idle-write-idle bus cycles are shown. The signal label $\overline{\text{CMD}}$ represents the appropriate command output for the bus cycle. For those five figures, the CMDLY input is connected to GND and CENL to VCC. The effects of CENL and CMDLY are described later in the section on control inputs.

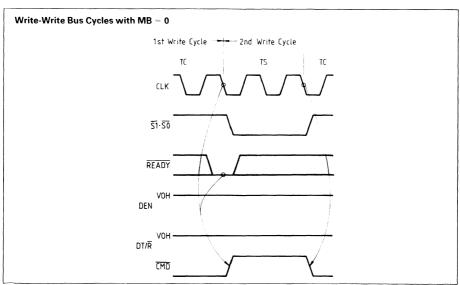
The next two figures show non-Multibus cycles. MB is connected to GND while CEN is connected to VCC. The figure on page 10 shows a read cycle with no wait states while the figure on page 11 shows a write cycle with one wait state. The READY input is shown to illustrate how wait states are added.

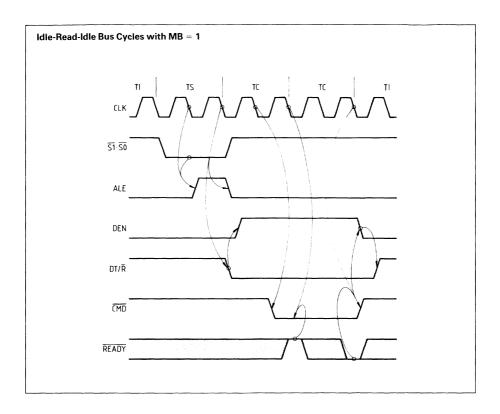


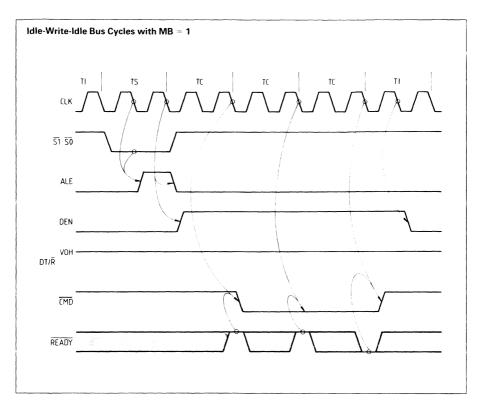
Bus cycles can occur back-to-back with no TI bus states between TC and TS. Back-to-back cycles do not affect the timing of the command and control outputs. Command and control outputs always reach the states shown for the same clock edge (within TS, TC, or following bus state) of a bus cycle. A special case in control timing occurs for back-to-back write cycles with MB = 0. In this case, DT/ \bar{R} and DEN remain high between the bus cycles (see respective idle-read-idle cycle diagram). The command and ALE output timing does not change.

The figures on pages 12 and 13 show a Multibus cycle with MB = 1. \overline{AEN} and CMDLY are connected to GND. The effects of CMDLY and \overline{AEN} are described later in the section on control inputs. The top figure shows a read cycle with one wait state and the figure below shows a write cycle with two wait states. The second wait state of the write cycle is shown only for example purposes and is not required. The \overline{READY} input is shown to illustrate how wait states are added.









The MB control input affects the timing of the command and DEN outputs. These outputs are automatically delayed in Multibus mode to satisfy three requirements:

- 1) 50 ns minimum setup time for valid address before any command output becomes active.
- 50 ns minimum setup time for valid write data before any write command output becomes active.
- 3) 65 ns maximum time from when any read command becomes inactive until the slave's read data drivers reach tristate off.

Three signal transitions are delayed by MB = 1 as compared to MB = 0:

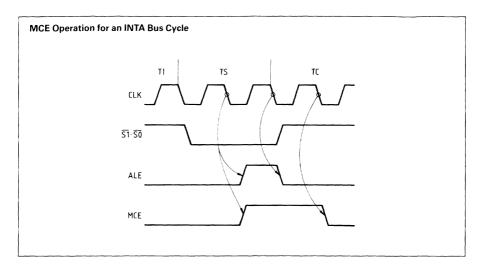
- The high to low transition of the read command outputs (IORC, MRDC, and INTA) is delayed one CLK cycle.
- The high to low transition of the write command outputs (IOWC and MWTC) is delayed two CLK cycles.

The low to high transition of DEN for write cycles is delayed one CLK cycle.

Back-to-back bus cycles with MB = 1 do not change the timing of any of the command or control outputs. DEN always becomes inactive between bus cycles with MB = 1.

Except for a halt or shutdown bus cycle, ALE will be issued during the second half of TS for any bus cycle. ALE becomes inactive at the end of the TS to allow latching the address to keep it stable during the entire bus cycle. The address outputs may change during phase 2 of any TC bus state. ALE is not affected by any control input.

The following figure shows how MCE is timed during interrupt acknowledge (INTA) bus cycles. MCE is one CLK cycle longer than ALE to hold the cascade address from a master SAB 8259A valid after the falling edge of ALE. With the exception of the MCE control output, an INTA bus cycle is identical in timing with a read bus cycle. MCE is not affected by any control input.



Control Inputs

The control inputs can alter the basic timing of command outputs, allow interfacing to multiple buses, and share a bus between different masters. For many SAB 80286 systems, each CPU will have more than one bus which may be used to perform a bus cycle. Normally, a CPU will only have one bus controller active for each bus cycle. Some buses may be shared by more than one CPU (i.e. Multibus) requiring only one of them use the bus at a time.

Systems with multiple and shared buses use two control input signals of the SAB 82288 bus controller, CENL and \overline{AEN} (see figure on system use of those signals). CENL enables the bus controller to control the current bus cycle. The \overline{AEN} input prevents a bus controller from driving its command outputs. \overline{AEN} high means that another bus controller may be driving the shared bus.

In the figure on the AEN and CENL signal, two buses are shown: a local bus and a Multibus. Only one bus is used for each CPU bus cycle. The CENL inputs of the bus controllers select which bus controller is to perform the bus cycle. An address decoder determines which bus to use for each bus cycle. The SAB 82288 connected to the shared Multibus must be selected by CENL and be given access to the Multibus by AEN before it will begin a Multibus operation.

CENL must be sampled high at the end of the TS bus state (see waveforms) to enable the bus controller to activate its command and control outputs. If sampled low the commands and DEN

will not go active and DT/ \overline{R} will remain high. The bus controller will ignore the CMDLY, CEN, and \overline{READY} inputs until another bus cycle is started via $\overline{S1}$ and $\overline{S0}$. Since an address decoder is commonly used to identify which bus is required for each bus cycle, CENL is latched to avoid the need for latching its input.

The CENL input can affect the DEN control output. When MB = 0, DEN normally becomes active during phase 2 of TS in write bus cycles. This transition occurs before CENL is sampled. If CENL is sampled low, the DEN output will be forced low during TC as shown in the timing waveforms.

When MB = 1, CEN/ĀEN becomes ĀEN , ĀEN controls when the bus controller command outputs enter and exit tristate off. $\overline{\text{AEN}}$ is intended to be driven by a bus arbiter, like the SAB 82289, which assures only one bus controller is driving the shared bus at any time. When $\overline{\text{AEN}}$ makes a low to high transition, the command outputs immediately enter tristate off and DEN is forced inactive. An inactive DEN should force the local data transceivers connected to the shared data bus into tristate off (see next figure). The low to high transition of $\overline{\text{AEN}}$ should only occur during TI or TS bus states.

The high-to-low transition of AEN signals that the bus controller may now drive the shared bus command signals. Since a bus cycle may be active or be in the process of starting, AEN can become active during any T-state. AEN low immediately allows DEN to go to the appropriate state. Three CLK

edges later, the command outputs will go active (see timing waveforms). The Multibus requires this delay for the address and data to be valid on the bus before the commands become active.

When MB = 0, CEN/ $\overline{\text{AEN}}$ becomes CEN. CEN is an asynchronous input which immediately affects the command and DEN outputs. When CEN makes a high-to-low transition, the commands and DEN are immediately forced inactive. When CEN makes a low-to-high transition, the commands and DEN outputs immediately go to the appropriate state (see timing waveforms). $\overline{\text{READY}}$ must still become active to terminate a bus cycle if CEN remains low for a selected bus controller (CENL was latched high).

Some memory or I/O systems may require more address or write data setup time to command active than provided by the basic command output timing. To provide flexible command timing, the CMDLY input can delay the activation of command outputs. The CMDLY input must be sampled low to activate the command outputs. CMDLY does not affect the control outputs ALE, MCE, DEN, and DT/R.

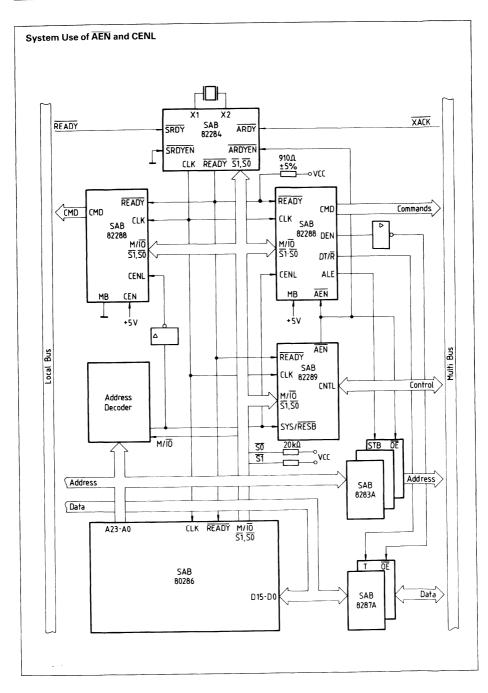
CMDLY is first sampled on the falling edge of the CLK ending TS. If sampled high, the command output is not activated, and CMDLY is again sampled on the next falling edge of CLK. Once sampled low, the proper command output becomes active immediately if MB=0. If MB=1, the proper command goes active no earlier than shown in the figures on pages 12 and 13.

READY can terminate a bus cycle before CMDLY allows a command to be issued. In this case no commands are issued and the bus controller will deactivate DEN and DT/R in the same manner as if a command had been issued.

Waveforms

The waveforms show the timing relationships of inputs and outputs and do not show all possible transitions of all signals in all modes. Instead, all signal timing relationships are shown via the general cases. Special cases are shown when needed. The waveforms provide some functional descriptions of the SAB 82288; however, most functional descriptions are provided in the figures of section Functional Description.

To find the timing specification for a signal transition in a particular mode, first look for a special case in the waveforms. If no special case applies, then use a timing specification for the same or related function in another mode.



Absolute Maximum Ratings 1)

Ambient temperature under bias $0 \text{ to } 70^{\circ}\text{C}$ Storage temperature $-65 \text{ to } +150^{\circ}\text{C}$ Voltage on any pin with respect to GND -0.5 to +7VPower dissipation 1 W

DC Characteristics

TA = 0 to $70^{\circ}C$, $VCC = 5V \pm 10\%$

Symbol	Parameter	Limit	values	Unit	Test condition	
Syllibol	raiametei	min.	max.	Unit	rest condition	
ICC	Power supply current		100			
IF	Input current (\$\overline{S0}, \$\overline{S1}, M/\overline{IO})		-0.5	mA	VF = 0.45 V	
ILI	Input leakage current (all other)	-	±10	uА	0 V ≤ VIN ≤ VCC	
ILO	Output leakage current		± 10		0.45 V ≤ VOUT ≤ VCC	
VOL	Low output voltage Command outputs Control outputs		0.45		IOL = 32 mA IOL = 16 mA	
VOH	High output voltage Command outputs Control outputs	2.4	_		IOH = -5 mA IOH = -1 mA	
VIL	Low input voltage	-0.5	0.8	\ \		
VCL	CLK low input voltage	0.5	0.6			
VIH	High input voltage	2.0	VCC	1	-	
VCH	CLK high input voltage	3.9	+0.5			
CCLK	CLK input capacitance	_	12	pF	fC = 1 MHz	
CI	Input capacitance		10	1 10	IC - TIVITZ	

¹⁾ Stresses above those listed under "absolute maximum ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC Characteristics SAB 82288

 $TA = 0 \text{ to } 70^{\circ}\text{C}, VCC = 5 \text{ V} \pm 10\%$

Symbol	Parameter		Lim	it values	Unit	Test condition
			min.	max.	Unit	
T1	CLK period		62	250		_
T2	CLK high time		20	235		at 3.6 V
Т3	CLK low time		15	230		at 1.0 V
T4	CLK fall time		_	10		3.6 to 1.0 V
T5	CLK rise time					1.0 to 3.6 V
Т6	M/IO and status setup time		22			from 0.8 or 2.0 V on input to 0.8 V on CLK
Т7	M/IO and status hold time		0			
T8	CENL setup time		20			
T9	CENL hold time		0			
T10	READY setup time		38			
T11	READY hold time		25			
T12	CMDLY setup time		20		ns	
T13	CMDLY hold time		0			
T14	AEN setup time	1)	20			
T15	AEN hold time	1)	0			
T16	ALE, MCE active delay		3	20		from 0.8 V on CLK to 0.8 or 2.0 V on output IOL = 16 mA IOH = -1 mA CL = 150 pF
T17	ALE, MCE inactive delay			20		
T18	DEN (WRITE) inactive from CENL		_	35		
T19	DT/R low from CLK			25		
T20	DEN (read) active from DT/R		5	35		
T21	DEN (read) inactive delay		3	35		
T22	DT/R high from DEN inactive		5	35		
T23	DEN (write) active delay		-	30		
T24	DEN (write) inactive delay		3	30		
T25	DEN inactive from CEN			25		
T26	DEN active from CEN			30		
T27	DT/R high from CLK and CEN	2)	_	35		
T28	DEN active from AEN			30		

Notes see next page

AC Characteristics SAB 82288 (cont'd)

Symbol	Parameter	Limit values		Unit	-	
	rarameter	min.	max.	Unit	Test condition	
T29	Command active delay	3	25		IOL = 32 mA	
T30	Command inactive delay	3	25		IOH = -5 mA CL = 300 pF	
T31	Command inactive from CEN		25	1	from 0.8 V on CLK	
T32	Command active from CEN		25	ns	to 0.8 or 2.0 V on output	
T33	Command inactive enable from AEN	-	40			
T34	Command float time		40			

¹⁾ AEN is an asynchronous input. AEN setup and hold times are specified to guarantee the response shown in the waveforms.

²⁾ T27 only applies to bus cycles where MB = 0, the SAB 82288 was selected, and DEN = 0 when the cycle terminated (because CEN = 0).

AC Characteristics SAB 82288-6

 $TA = 0 \text{ to } 70^{\circ}\text{C}, VCC = 5V \pm 10\%$

Complete	Devementar		Lim	it values	Unit	Tost condition	
Symbol	Parameter		min.	max.	Unit	Test condition	
T1	CLK period		83	250		_	
T2	CLK high time		25	235		at 3.6 V	
T3	CLK low time		20	225		at 1.0 V	
T4	CLK fall time			10		3.6 to 1.0 V	
T5	CLK rise time					1.0 to 3.6 V	
T6	M/IO and status setup time		28				
T7	M/IO and status hold time		0				
T8	CENL setup time		30				
Т9	CENL hold time		0			from 0.8 or	
T10	READY setup time		50			to 0.8 V on CLK	
T11	READY hold time		35				
T12	CMDLY setup time		25		ns		
T13	CMDLY hold time		0				
T14	AEN setup time	1)	25			1)	
T15	AEN hold time	1)	0				
T16	ALE, MCE active delay		3	25			
T17	ALE, MCE inactive delay			35			
T18	DEN (write) inactive from CENL		_	35			
T19	DT/R low from CLK			40			
T20	DEN (read) active from DT/\overline{R}		5	50		from 0.8 V on CLK	
T21	DEN (read) inactive delay		3	40		from 0.8 or 2.0 V on input to 0.8 V on CLK 1) from 0.8 V on CLK to 0.8 or 2.0 V on output IOL = 16 mA IOH = -1 mA CL = 150 pF	
T22	DT/R high from DEN inactive		5	45		1	
T23	DEN (write) active delay		-	35			
T24	DEN (write) inactive delay		3				
T25	DEN inactive from CEN			40			
T26	DEN active from CEN		_	35			
T27	DT/R high from CLK and CEN	2)		50		2)	
T28	DEN active from AEN			35			

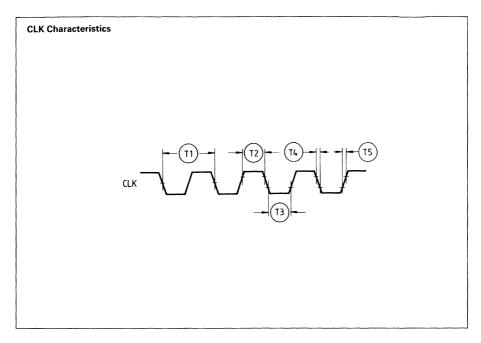
Notes see next page

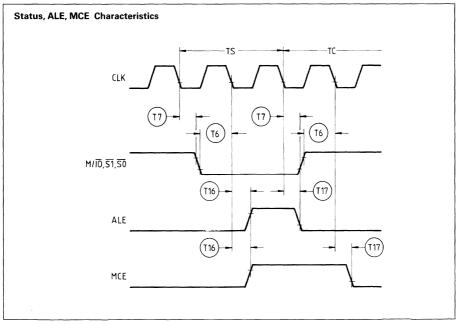
AC Characteristics SAB 82288-6 (cont'd)

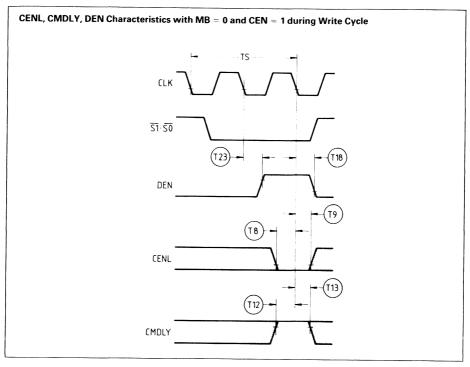
Symbol	Parameter	Limi	t values	11	
	· Grameter	min.	max.	Unit	Test condition
T29	Command active delay	3	40		IOL = 32 mA
T30	Command inactive delay	3	30		IOH = -5 mA CL = 300 pF
T31	Command inactive from CEN		35		from 0.8 V on CLK
T32	Command active from CEN		45	ns	to 0.8 or 2.0 V on output
T33	Command inactive enable from AEN	_	40	1	
T34	Command float time		40		

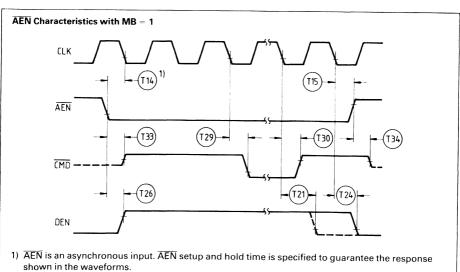
¹⁾ $\overline{\text{AEN}}$ is an asynchronous input. $\overline{\text{AEN}}$ setup and hold times are specified to guarantee the response shown in the waveforms.

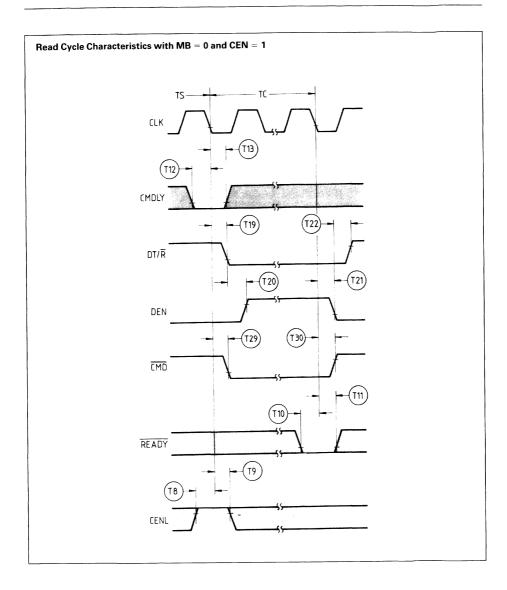
²⁾ T27 only applies to bus cycles where MB=0, the SAB 82288 was selected, and DEN=0 when the cycle terminated (because CEN=0).

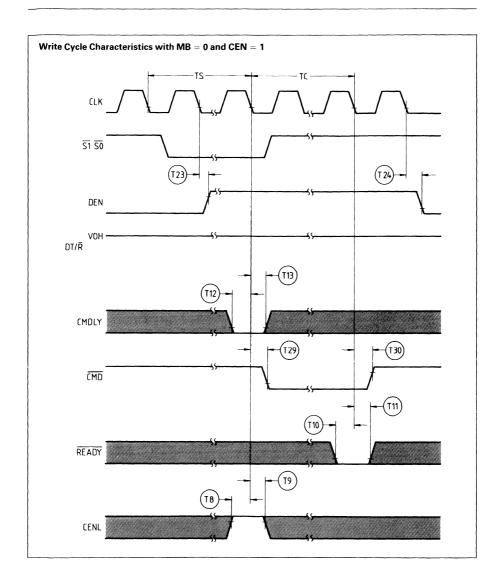


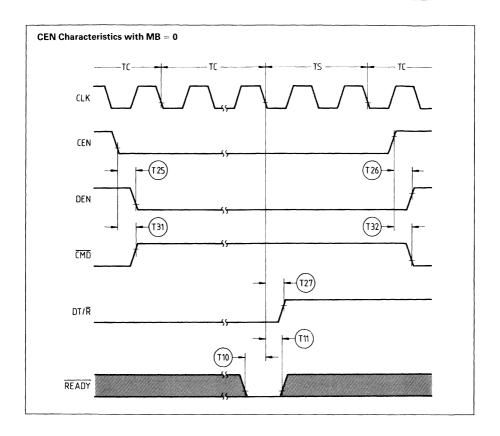




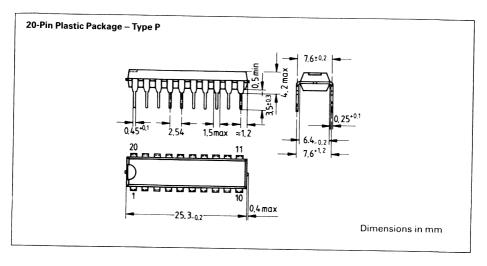








Package Outline



SAB 82288

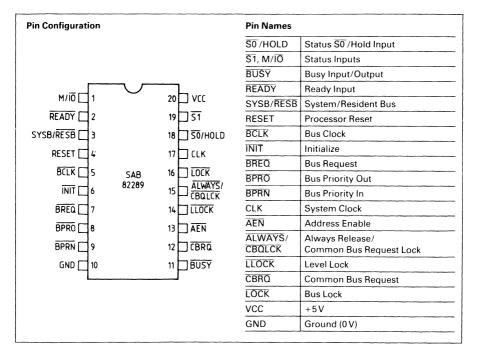
Ordering Information

Туре	Description	Ordering Code
SAB 82288-P	Bus controller (plastic package) up to 16 MHz	Q67120-Y75
SAB 82288-6-P	Bus controller (plastic package) up to 12 MHz	Q67120-Y110



SAB 82289 Bus Arbiter for SAB 80286 Processor Family

- Supports multimaster system bus arbitration protocol
- Synchronizes SAB 80286 processor with multimaster bus
- Compatible with IEEE 796 standard bus (Multibus *)
- Three modes of bus release operation for flexible system configuration
- Supports parallel, serial and rotating priority resolving schemes



The SAB 82289 Bus Arbiter is a 5 V, 20-pin MYMOS component for use in multiple bus master SAB 80286 systems. The SAB 82289 provides a compact solution to system bus arbitration for the SAB 80286 CPU.

The complete IEEE 796 Standard bus arbitration protocol is supported. Three modes of bus release operation support a number of bus usage models.

^{*)} Multibus is a registered trademark of Intel Corporation.

Pin Definitions and Functions

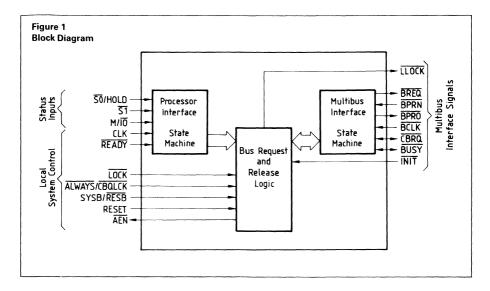
Symbol	Pin	Input (I) Output (O)	Function						
M/ĪŌ, S1	1, 19	I	STATUS INPUTS are the status input signal pins from the SAB 80286 processor. The arbiter decodes these inputs together with the \$\overline{SO}\$ /HOLD input to initiate bus request and surrender actions. A bus cycle is started when either \$\overline{SI}\$ or \$\overline{SI}\$ is sampled low at the falling edge of CLK. The SAB 80286's \$\overline{SI}\$ and \$M/IO\$ pins meet the setup and hold time requirements of these pins. SAB 80286 Bus Cycle Status Encoding						
			M/IO	S1	S0/HOLD	Type of Bus Cycle			
			S1 and	M/ĪŌ pir		Interrupt acknowledge I/O read I/O write None, bus idle Halt or shutdown Memory read Memory write None, bus idle utput of another bus master, the			
READY	2	1	READY is an active-low signal which indicates the end of the bus cycle. The SAB 80286 halt or shutdown cycle does not require READY to terminate the bus cycle. Setup and hold times for this pin must be met for proper operation.						
SYSB/RESB	3		SYSTEM BUS/RESIDENT BUS is an input signal which determines whether the multimaster system bus is required for the current bus cycle. The signal can originate from address mapping circuitry such as a decoder or PROM attached to the processor address and status pins. The arbiter will request or retain control of the multimaster system bus when the SYSB/RESB pin is sampled high at the end of the TS bus state. During an interrupt acknowledge cycle, this input is sampled on every falling edge of CLK starting at the end of the TS state until either SYSB/RESB is sampled high or the bus cycle is terminated by the READY signal. Setup and hold times for this pin must be met for proper operation.						
RESET	4	ı	PROCESSOR RESET is an active-high input synchronous to the system clock (CLK). RESET is the processor initialization and an indication to the arbiter to release the multimaster bus and clear any pending request.						
BCLK	5	1	the mul	timaster		r system bus clock to which signals are synchronized. CLK.			
INIT	6	ı	INITIALIZE is an active-low Multibus signal used to reset all arbiters on the Multibus system. It will cause the release of the multimaster bus, but will not clear the pending bus master request so that the arbiter can again request the multimaster bus. No arbiters have the use of the multimaster bus immediately after initialization. INIT is an asynchronous signal to CLK.						

Pin Definitions and Functions (continued)

Symbol	Pin	Input (I) Output (O)	Function
BREQ	7	0	BUS REQUEST is an active-low output signal used in the parallel and rotating priority resolving schemes. The arbiter activates BREQ to request the use of the multimaster system bus. The arbiter holds BREQ active as long as it is requesting or has possession of the multimaster system bus.
BPRO	8	0	BUS PRIORITY OUT is an active-low output signal used in serial priority resolving scheme. BPRO is connected to BPRN of the next lower priority arbiter to grant or revoke priority from that arbiter.
BPRN	9	1	BUS PRIORITY IN is an active-low input indicating that this arbiter has the highest priority of any arbiter requesting the system bus. BPRN high signals the arbiter that a higher priority arbiter is requesting or has possession of the system bus. Setup and hold times for this pin must be met for proper operation.
BUSY	11	I/O (open- drain)	BUSY is a Multibus signal which is asserted when the system bus is in use. BUSY is an open drain input/output requiring an external pullup resistor. As an input BUSY asserted indicates when the Multibus is in use. Setup and hold times must be met for proper operation. As an output BUSY is asserted to signal when this arbiter has taken control of the Multibus.
CBRO	12	I/O (open- drain)	COMMON BUS REQUEST is a Multibus signal that indicates when an arbiter is requesting the Multibus. This pin is an open-drain input/output requiring an external pullup resistor. As an input CBRQ indicates that another arbiter is requesting the multimaster system bus. The input function of this pin is enabled by the CBQLCK signal. Setup and hold times for this pin must be met for proper operation. As an output CBRQ is asserted to indicate that this arbiter is requesting the Multibus. The arbiter pulls CBRQ low when it issues BREQ. The arbiter releases CBRQ when it obtains the Multibus.
AEN	13	0	ADDRESS ENABLE is the output of the arbiter which goes directly to the processor's address latches, the SAB 82288 bus controller and the SAB 82284 clock generator. AEN asserted causes the bus controller and address latches to enable their output drivers. AEN also drives the clock generator's ARDYEN input to enable its asynchronous ready input (ARDY). AEN can also be used as an active-low hold acknowledge to a bus master other than the SAB 80286. It signals to the bus master that control of the system bus has been relinquished when AEN is inactive (high). Note that AEN goes active relative to BCLK and goes inactive
			enable their output drivers. AEN also drives to generator's ARDYEN input to enable its asyn input (ARDY). AEN can also be used as an active-low hold at to a bus master other than the SAB 80286. It is master that control of the system bus has been when AEN is inactive (high).

Pin Definitions and Functions (continued)

Symbol	Pin	Input (I) Output (O)	Function
LLOCK	14	0	LEVEL LOCK is an active-low output signal decoded from the processor LOCK signal. LLOCK can be used as Multibus LOCK when buffered with a tri-state buffer enabled by the AEN signal. LLOCK will be cleared by RESET but not by INIT.
ALWAYS/ CBQLCK	15		ALWAYS RELEASE or COMMON BUS REQUEST LOCK can be programmed at processor reset to be either the ALWAYS RELEASE (ALWAYS) strapping option or the COMMON BUS REQUEST LOCK (CBQLCK) control input. Setup and hold times for this pin must be met for proper programming. When this pin is low during the falling edge of processor
			reset (ALWAYS option) the arbiter is programmed to surrender the multimaster system bus after each bus transfer cycle. The SAB 82289 will remain in the ALWAYS RELEASE mode until it is reprogrammed during the next processor reset.
			The bus arbiter is programmed to support the COMMON BUS REQUEST LOCK function by forcing this input pin high during the falling edge of the processor reset.
			CBOLCK itself is an active-low signal which when active prevents the arbiter from surrendering the multimaster system bus to a common bus request through the CBRO input pin.
LOCK	16	1	LOCK is a processor-generated signal which when asserted (low) prevents the arbiter from surrendering the multi-master system bus to any other bus arbiter, regardless of its priority. LOCK is sampled by the arbiter at the end of the TS (status) bus state. Setup and hold times for this pin must be met for proper operation.
CLK	17	1	SYSTEM CLOCK accepts the CLK signal from the SAB 82284 clock generator chip as the timing reference for the bus arbiter and processor interface signals.
S0/HOLD	18	1	STATUS INPUT \$\overline{S0}\$ or HOLD is either the \$\overline{S0}\$ status signal from the SAB 80286 or the HOLD signal from some other bus master. The function of this input is established during the processor reset of the SAB 82289 bus arbiter. The SAB 80286 \$\overline{S0}\$ pin meets the setup and hold time requirements of this pin.
			The \$\overline{S0}\$ pin function is selected by forcing this input high during the falling edge of processor reset if the SAB 82289 is used to support an SAB 80286 processor, the \$\overline{S0}\$ output of the processor will be high during reset.
			In supporting the SAB 80286 processor, the SAB 82289 decodes the \$\overline{S0}\$ pin together with the other status input \$\overline{S1}\$ and M/IO to determine the beginning of a processor bus cycle and initiate bus request and surrender actions.
			The HOLD function of the \$\overline{S0}\$/HOLD pin is selected by holding this input low during the falling edge of processor reset. When supporting a bus master other than SAB 80286 the SAB 82289 monitors the HOLD signal to initiate bus request and surrender actions.
VCC	20		POWER SUPPLY (+5V)
GND	10	_	GROUND (0 V)



Functional Description

The SAB 82289 bus arbiter in conjunction with the SAB 82288 bus controller and the SAB 82284 clock generator interfaces the SAB 80286 processor or some other bus master to a multimaster system bus. The arbiter multiplexes a processor to a multimaster system bus. It avoids contention with other bus masters.

The SAB 82289 has two separate state machines which communicate through bus request and release logic. The processor interface state machine is synchronous with the local system clock (CLK) and the multimaster system bus interface state machine is synchronous with the bus clock (BCLK).

The SAB 82289 performs all signaling to request, obtain, and release the system bus. External logic is used to determine which bus cycles require the system bus and to resolve priorities of simultaneous requests for control of the system bus.

SAB 82289 with SAB 80286

In a SAB 80286 system using a SAB 82289 bus arbiter, the SAB 80286 processor is unaware of the arbiter's existence and issues commands as though it had exclusive use of a multimaster system bus, such as Multibus. If the processor cycle requires Multibus access, the arbiter requests control of the Multibus. Until the request is granted the SAB 82289 keeps AEN disabled to prevent the SAB 82288 bus controller and the address latches from accessing

the Multibus. AEN inactive also disasserts the asynchronous ready enable (ARDYEN) input of the SAB 82284 clock chip so that the system bus will appear as "NOT READY" to the SAB 80286 processor.

Once the SAB 82289 bus arbiter has acquired the bus, it will assert ĀEN allowing the SAB 82288 bus controller and the address latches to access the system bus and asserting the ĀRDYEN input of the SAB 82284 clock chip.

Typically, once the data transfer command has been issued by the SAB 82288 and the data transfer has taken place, a transfer acknowledge (XACK) signal is returned to the processor on the multimaster system bus to indicate "READY" from the accessed slave device. The processor remains in a series of "wait states" (repeated TC states) until the addressed device responds with XACK asserted signal to the SAB 82284's ARDY input and the SAB 82284 asserts READY to the processor. The processor then completes its bus cycle.

SAB 82289 with Other Bus Masters

When supporting other bus masters, the $\overline{S0}/HOLD$ and \overline{READY} pins of the bus arbiter can be connected to the "hold" pin of that master. The inverted \overline{AEN} signal from the SAB 82289 can be used as the hold acknowledge (HLDA) input for the other bus master.

The bus master sends a HOLD signal to the bus arbiter when it needs the system bus for a memory access. If the arbiter currently controls the system bus, $\overline{\text{AEN}}$ will be active. Otherwise $\overline{\text{AEN}}$ will be inactive and the arbiter will request control of the system bus. The bus master will have to wait until the SAB 82289 has asserted $\overline{\text{AEN}}$ (low) before it starts its bus cycle.

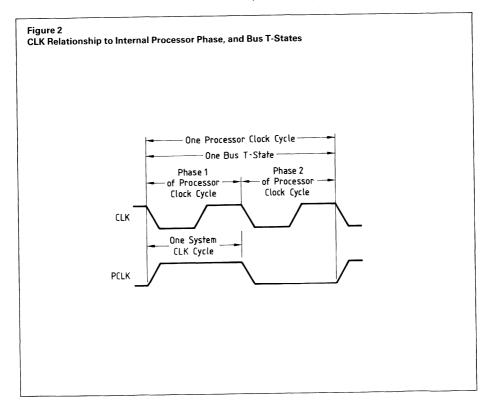
When the bus master no longer requires the Multibus it will have to inactivate the HOLD signal. The arbiter interprets the Multibus access as a single bus cycle which is terminated by HOLD going inactive (low). Thus the arbiter will not release the Multibus to any other bus master during a bus access cycle.

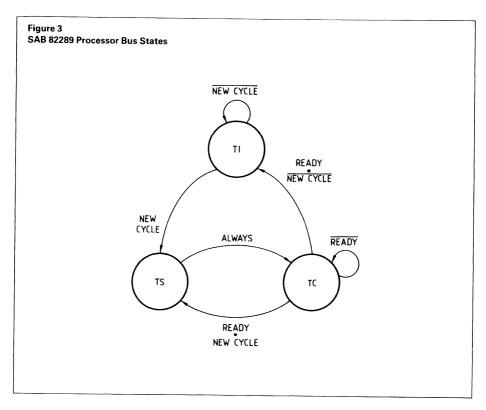
Processor Cycle Definition

Any SAB 80286 system which gains access to the Multibus through the SAB 82289 bus arbiter uses an internal clock which is one half the frequency of the system clock (CLK) (see figure 2). Knowledge of the phase of the local bus master internal clock is required for proper SAB 82289 control of the SAB 80286 interface to Multibus. The local bus master informs the bus arbiter of its internal clock phase when it asserts the status signals. The SAB 80286's \$\overline{50}\$ and \$\overline{51}\$ status signals are always first asserted in phase 1 of the local bus master's internal clock.

Bus State Definition

The SAB 82289 bus arbiter has three processor bus states (see figure 3): idle (TI), status (TS), command (TC). Each bus state is two CLK cycles long. Bus state phases correspond to the internal CPU clock phases.





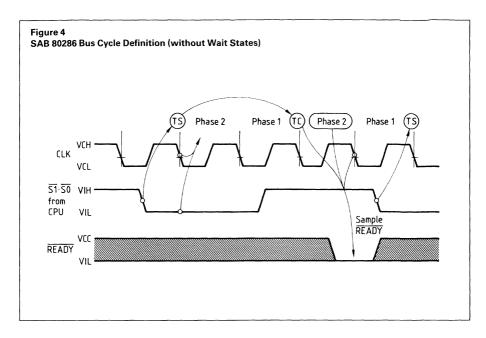
Bus Cycle Definition

The $\overline{S1}$ and $\overline{S0}$ status inputs are sampled by the SAB 82289 on the falling edge of CLK and signal the start of a bus cycle by going active (low). The TS bus state is defined to be the two CLK cycles during which either $\overline{S1}$ or $\overline{S0}$ is active (see figure 4). When either $\overline{S1}$ or $\overline{S0}$ is sampled low, the next CLK cycle is considered the second phase of the associated processor clock cycle.

The arbiter enters the TC bus state after the TS state. The shortest bus cycle may have one TS state and one TC state. Longer bus cycles are formed by repeating TC states. A repeated TC bus state is called a wait state.

The READY input determines whether the current TC bus state is to be repeated. The READY input has the same timing and effect for all bus cycles. READY is sampled at the end of each TC bus state to see if it is active. If sampled high, the TC bus state is repeated. This is called inserting a wait state.

When READY is sampled low, the current bus cycle is terminated. Note that the bus arbiter may enter the TS bus state directly from TC if the status lines are sampled active (low) at the next falling edge of CLK (see figure 4). If neither of the status lines is sampled active at that time the SAB 82289 will enter the TI bus state. The TI bus state will be repeated until the status inputs are sampled active.



Arbitration between Bus Masters

The Multibus protocol allows multiple processing elements to compete with each other to access common system resources. Since the local SAB 80286 processor does not have exclusive use of the system bus, if the Multibus is "BUSY" the SAB 80286 processor will have to wait before it can access the system bus.

The SAB 82289 bus arbiter provides an integrated solution for controlling access to a multimaster system bus. The bus arbiter allows both higher and lower priority bus masters to acquire the system bus depending on which release mode is used. In general higher priority masters obtain the bus immediately after any lower priority master completes its present transfer cycle. Lower priority bus masters obtain the bus when a higher priority master is not accessing the system bus or the proper surrender conditions exist. The SAB 82289 handles this arbitration in a manner completely transparent to the bus master (e.g. SAB 80286 processor).

At the end of each transfer, the arbiter may retain or release the system bus. This decision is controlled by the processor state, bus arbitration inputs and arbiter strapping options (see releasing the Multibus, ahead).

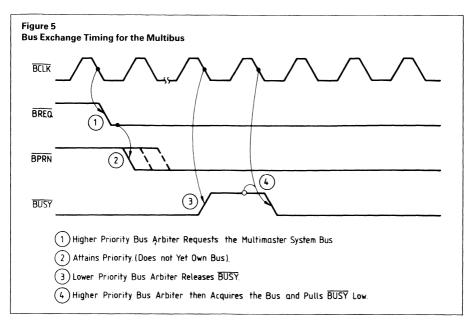
Priority Resolving Techniques

Some means of resolving priority between bus masters requesting the multimaster bus simultaneously must be provided. The SAB 82289 bus arbiter supports parallel, serial and rotating system bus priority resolving techniques. All of these techniques are based on the concept that, at a given time, one bus master will have priority above all the others.

An individual arbiter is the highest priority arbiter requesting the Multibus when its BPRN input is asserted (low). The highest priority requesting arbiter cannot immediately seize the system bus. It must wait until the present bus transaction is completed. Upon completing its current transaction the present bus owner surrenders the bus by releasing BUSY.

BUSY is an active-low "wired OR" Multibus signal connecting all bus arbiters on the system bus. When BUSY goes inactive, the arbiter which has requested the system bus and presently has bus priority (BPRN low), seizes the bus by pulling BUSY low (see waveform in figure 5).

The generation of a multimaster bus request (BREQ) is controlled by the type of bus cycle and the SYSB/RESB input. Whenever the processor signals the status for memory read, memory write, I/O read,

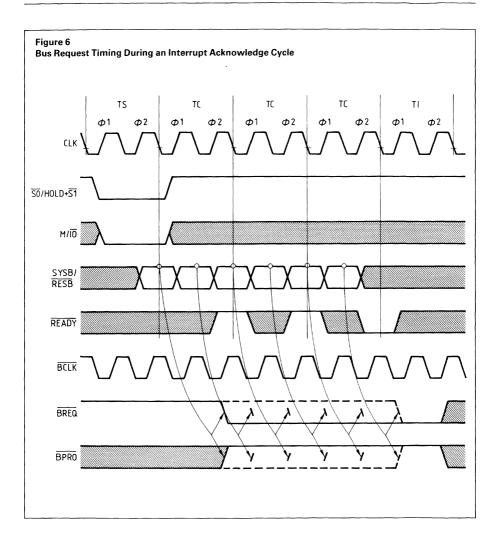


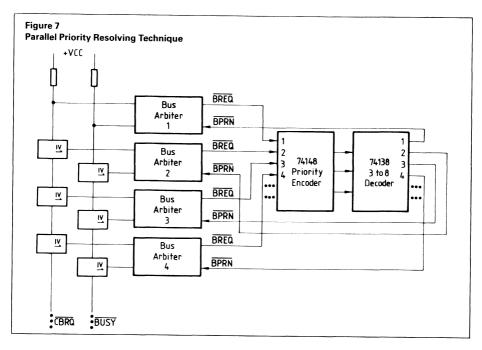
I/O write or interrupt acknowledge cycle, and SYSB/ $\overline{\text{RESB}}$ is high at the end of TS, a bus request is generated.

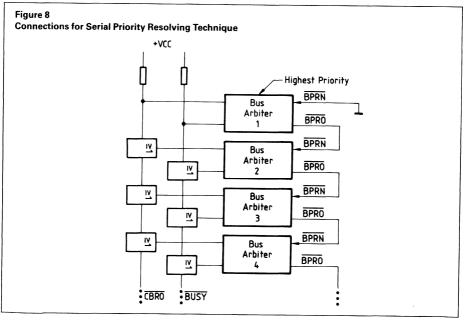
When the status inputs indicate an interrupt acknowledge bus cycle, the arbiter allows external logic to decide (through the SYSB/RESB input) whether the interrupt acknowledge cycle should use the Multibus.

Figure 6 shows how SYSB/RESB is repeatedly sampled until it is sampled high or the bus cycle is terminated. If the bus cycle is completed (READY is sampled low) before SYSB/RESB is sampled high, the arbiter will not request the Multibus.

The SAB 82289 bus arbiter does not generate a separate BREQ for each bus cycle. Instead the SAB 82289 generates BREQ when it requests the bus and holds BREQ active during the time that it has possession of the bus. Note that all multimaster system bus requests (via BREQ) are synchronized to the system bus clock (BCLK).







Parallel Priority Resolving Technique

The parallel priority resolving technique requires a separate bus request line (\overline{BREQ}) for each arbiter on the multimaster system bus (see figure 7). Each \overline{BREQ} line enters a priority encoder which generates the binary address of the highest priority \overline{BREQ} line currently active. The binary address is decoded to select the \overline{BPRN} line corresponding to the highest priority arbiter requesting the bus. In a parallel scheme, the \overline{BPRO} output is not used.

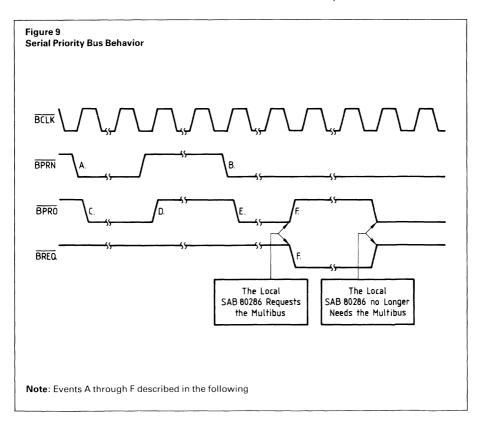
The arbiter receiving priority (BPRN low) then allows its associated bus master onto the multimaster system bus as soon as the bus becomes available (i.e. the bus is no longer busy). Any number of bus masters may be accommodated in this way, limited only by the complexity of the external priority resolving circuitry. Such circuitry must resolve the priority within one BCLK period.

Serial Priority Resolving Technique

The serial priority resolving technique eliminates the need for the priority circuitry of the parallel technique by daisy-chaining the bus arbiters together, that is, connecting the higher priority arbiter's BPRO output to the BPRN of the next lower priority arbiter (see figure 8). The highest priority bus arbiter would have its BPRN tied low in this configuration, signifying to the arbiter that it always has the highest priority when requesting the system bus. In a serial scheme, the BREQ output is not used. Since arbitration must be resolved within one BCLK period the number of arbiters connected together in the serial priority is limited by the arbiter's BPRN to BPRO propagation delay (18ns). For a 10 MHz Multibus BCLK, five SAB 82289 bus arbiters may be

connected in serial configuration.

BPRN to BPRO delay



When using the serial priority resolving scheme, a higher priority arbiter (for example, arbiter 2, figure 8) passes priority to the next lower priority arbiter (arbiter 3) by asserting its BPRO signal (low). This asserts BPRN of next arbiter (arbiter 3) as shown in figure 9 event A and event B. An arbiter's BPRO is asserted if the arbiter has priority (BPRN is asserted) but is not accessing or requesting the system bus (as indicated by BREQ inactive as shown in figure 9 event C and event E for arbiter 3). Whenever a higher priority arbiter (arbiter 3) issues a bus request its BPRO goes inactive causing the next lower priority arbiter (arbiter 4) to lose its bus priority (figure 9 event F). Any arbiter (arbiter 3) will also bring its BPRO inactive if its BPRN goes inactive (from arbiter 2), thereby passing the loss of bus priority on to the lower priority arbiters (e.g. arbiter 4) as shown in figure 9 event D.

Rotating Priority Resolving Technique

The rotating priority resolving technique is similar to the parallel priority resolving technique except that priority is dynamically re-assigned. The priority encoder is replaced by a more complex circuitry which rotates priority between requesting arbiters, thus allowing each arbiter an equal chance to use the multimaster system bus over a given period of time.

Selecting the Appropriate Priority Resolving Technique

The choice of a priority resolving technique involves a trade-off between external logic complexity and ease of Multibus access for the different bus masters in the system. The rotating priority resolving technique requires a substantial amount of external logic, but guarantees all the bus masters an equal opportunity to access the system bus. The serial priority resolving technique uses no external logic but has fixed bus master priority levels and can accomodate only a limited number of bus arbiters.

The parallel priority resolving technique is in general a compromise between the other two techniques (for example parallel priority configuration in the following figure allows up to eight arbiters to be present on the Multibus, with fixed priority levels, while not requiring a large amount of complex external logic to implement).

Releasing the Multibus

Following a data transfer cycle on the Multibus, the SAB 82289 bus arbiter can either retain control of the system bus or release the bus for use by some other bus master. The SAB 82289 can operate in one of three modes, defining different conditions under which the arbiter relinquishes control of the multimaster system bus. These release modes are described in the table below.

If the arbiter was programmed to operate in Always Release Mode (mode 1) during the previous reset, it will surrender the Multibus after each complete transfer cycle. If the arbiter is not in Always Release Mode, it will not surrender the bus until the local SAB 80286 processor enters a halt state, the arbiter is forced off the bus by the loss of \overline{BPRN} (mode 2 or 3), or by a common bus request when the \overline{CBRQ} input is enabled by the \overline{CBQLCK} input (mode 2).

CBRQ can save the bus exchange overhead in many cases. If CBRQ is high, it indicates to the bus master that no other master is requesting the bus and therefore the present bus master can retain the bus. Without CBRQ, only BPRN indicates whether or not another master is requesting the bus and that only if the other master is of higher priority. Between its bus transfer cycles the master must give up the bus in order to allow lower priority masters to take the bus if they need it. At it. 2 start of the master's next transfer cycle, the bus must be regained. If no other master has the bus, this can take approximately two BCLK periods. To avoid this overhead of unnecessarily giving up and regaining the bus when no other masters needs it. CBRQ is

SAB 82289 Release Modes

Release Mode	Conditions under which the bus arbiter releases the system bus (unless cycles are LOCKed)
Mode 1	The bus arbiter always releases the bus at the end of each transfer cycle
Mode 2	The bus arbiter ratains the bus until: • a higher-priority bus master requests the bus, driving BPRN high • a lower-priority bus master requests the bus by pulling CBRQ low
Mode 3	The bus arbiter retains the bus until: • a higher-priority bus master requests the bus, driving BPRN high (CBRQ low ignored)

extremely useful. Any master that wants but does not have the bus, must assert CBRQ (low). If CBRQ line is not asserted the bus does not have to be released, thereby eliminating the delay of regaining the bus at the start of the next cycle.

The \overline{LOCK} input to the arbiter can be used to override any of the conditions shown in the table before. While \overline{LOCK} is asserted, the arbiter will not surrender control of the Multibus to any other requesting arbiter. Note that the arbiter will surrender the Multibus (synchronous to \overline{BCLK}) either in response to RESET or \overline{INIT} signals independent of the current release mode or the state of the arbiter inputs.

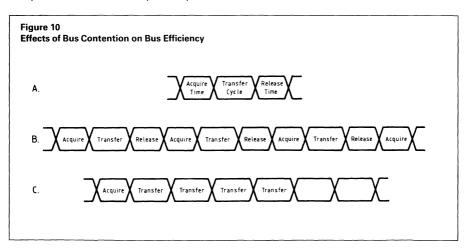
The three bus release modes have the same operation when supporting either the SAB 80286 processor or some other bus master.

Selecting the Appropriate Release Mode

The choice of which release mode to use may affect the bus utilization of the individual subsystems, and the system as a whole. Mode-dependent performance variations are due to the bus acquisition/ release overhead. The effect of these acquire and release times on system bus efficiency is illustrated in figure 10.

An isolated transfer on the multimaster system bus is depicted in figure 10-A. Figure 10-B shows utilization for the bus arbiter operation in mode 1. The arbiter must request and release the system bus for each transfer cycle. Lower priority arbiters have easy access to the system bus, but overall bus efficiency is low. Bus utilization for a bus arbiter operating in mode 2 or 3 is shown in the figure 10-C. In this situation the arbiter acquires the bus once for a sequence of transfers. The arbiter retains the bus until forced off by another bus master's request as defined in table before.

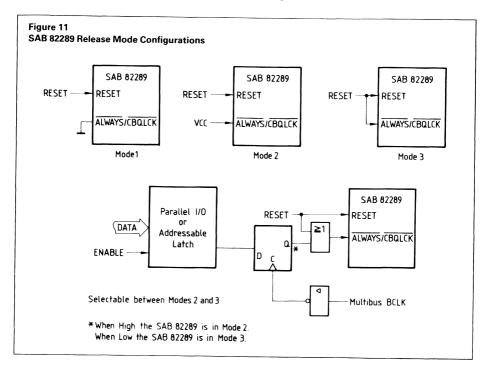
The three release modes of the SAB 82289 allow the designer to optimize the system use of the Multibus.

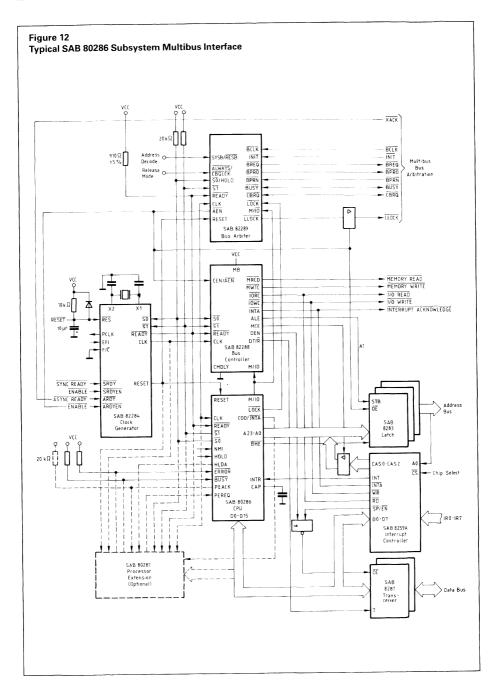


Configuring the SAB 82289 Release Mode

The SAB 82289 bus arbiter can be configured in any of its three bus release modes without additional hardware. It can also be configured to switch between mode 2 and mode 3 under software

control of the SAB 80286 processor, requiring that a parallel port or addressable latch be used to drive the ALWAYS/CBQLCK input pin of the SAB 82289 (see figure below).





Asserting the LOCK Signal

Independent of the particular release mode of the SAB 82289 bus arbiter, the SAB 80286 processor can assert a \overline{LOCK} signal synchronously to CLK to prevent the arbiter from releasing the Multibus. This software-controlled \overline{LOCK} signal prevents the SAB 82289 from surrendering the system bus to any other bus master, whether that bus master is of higher or lower priority. The \overline{LOCK} signal is typically used for implementing software semaphores for shared resources or for critical processes that must run in real-time.

The SAB 82289 LLOCK output is the Multibus timing-compatible signal asserted during all bus cycles which are locked together. The LLOCK is set or reset depending on processor LOCK at the end of the TS cycle. LLOCK will delay going inactive until the termination of the current transfer cycle.

The SAB 82289 will continue to assert the LLOCK signal retaining control of the Multibus until the end of the first "unLOCKed" SAB 80286 bus cycle (SAB 80286 disables its LOCK output on the last bus cycle indicating that no future locked cycles are needed). While the LOCK signal will force the arbiter presently in control to hold the system bus, it cannot force another arbiter to surrender the bus any earlier than it normally would.

The LLOCK signal from the SAB 82289 must be connected to a tri-state buffer in order to drive the Multibus LOCK signal. This tri-state buffer should be enabled by the AEN signal from the arbiter going active.

SAB 82289 Reset and Initialization

The SAB 82289 bus arbiter provides the RESET and INIT pins for initialization. RESET is a CLK synchronous signal from the SAB 82284 clock generator and INIT is an asynchronous signal on the multimaster system bus. By having RESET pin high or INIT pin low the BREQ, BUSY and AEN output pins will all become inactive. RESET will also deactivate the LLOCK signal. Unlike RESET, INIT will not clear any pending bus request, the bus request would be asserted after the INIT signal goes inactive.

Note that when the SAB 82289 is initialized by the RESET input it does not wait until the end of the current bus cycle to reset. Any bus cycle in process when RESET goes active will be aborted by the arbiter. Although the INIT signal will also interrupt an active bus cycle, the arbiter can request the Multibus and complete the bus cycle when INIT goes inactive.

As mentioned in the pin description and figure 11 the functions of the SO/HOLD pin and the release mode (ALWAYS/CBOLCK pin) are programmed at the falling edge of RESET.

Absolute Maximum Ratings 1)

DC Characteristics

TA = 0 to 70°C, VCC = $5V \pm 5\%$

C	Parameter	Limi	t values	Unit	Test condition	
Symbol	Parameter	min.	max.	Onit	rest condition	
VIL	Input low Voltage	-0.5	8			
VIH	Input High Voltage	2.0	VCC+0.5			
VILC	CLK Input Low Voltage	-0.5	6	v		
VIHC	CLK Input High Voltage	3.8	VCC+1.0	•		
VOL	Output Low Voltage: BUSY, CBRQ BPRO, BREQ, AEN LLOCK	_	45		IOL = 32mA IOL = 16 mA IOL = 5mA	
VOH	Output High Voltage	2.4	-		IOH = 400 μA	
ILI	Input Leakage Current		±10 ±1	μA mA	0.45 V ≤VIN ≤VCC 0 V ≤VIN <0.45 V	
ILO	Output Leakage Current		±10	μΑ	0.45 V ≤VOUT ≤VCC	
ICC	Power Supply Current	_	120	mA	_	
CCLK	CLK, BCLK Input Capacitance		12			
CIN	Input Capacitance		10	pF	fC = 1 MHz	
СО	Input/Output Capacitance		20			

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC Characteristics SAB 82289

TA = 0 to 70°C, VCC = 5V $\pm 5\%$ AC timings are referenced to 0.8 and 2.0 V points of signals as illustrated in data sheet waveforms, unless otherwise noted.

Symbol	Parameter		values * MHz	Unit	Test condition	Shown in
		min.	max.			Figure
1	CLK Cycle Period	62	t 5 + 50		_	
2	CLK Low Time	15	230		at 1.0 V	
3	CLK High Time	20	235		at 3.6V	
4	CLK Rise/Fall Time	-	10	1	1.0 to 3.6V	
5	BCLK Cycle Time	100	œ			13
6	BCLK High/Low Time	30		1		
7	\$0/HOLD, \$1, M/IO Setup	22				
8	S0/HOLD, S1, M/IO Hold	1	1	ns		
9	READY Setup	38	1			
10	READY Hold Time	25			_	
11	LOCK, SYSB/RESB Setup Time	20	1			10.10
12	LOCK, SYSB/RESB Hold Time	1	1			13, 18
13	RESET Setup Time	20	1			
14	RESET Hold Time	1	1-			19
15	RESET Active Pulse Width	16	1	CLKs	1	
16	INIT Setup Time	45	1		9)	
17	INIT Hold Time	1	1		(9)	20
18	INIT Active Pulse Width	3 (t1) +3(t14)				
19	BUSY, BPRN, CBRQ, CBQLCK/ALWAYS Setup to BCLK (or to RESET)	20		ns	_	13,15,21
20	BUSY, BPRN, CBRQ, CBQLCK/ALWAYS Hold to BCLK (or to RESET)	1				
21	BCLK to BREQ Delay		30		1)	13, 14
22	BCLK to BPRO Delay	_	35		2)	1,7
23	BPRN to BPRO Delay	1	25		2)	17
24	BCLK to BUSY Active Delay	1	60	1	3)	13

For notes see next page.

AC Characteristics SAB 82289 (continued)

Symbol	Parameter		Limit values * 8 MHz		Test condition	Shown in
		min.	max.			Figure
25	BCLK to BUSY Float Delay		35		4)	13, 14
26	BCLK to CBRQ Active Delay]-	55]	5)	13
27	BCLK to CBRQ Float Delay		35]	4)	13, 20
28	BCLK to AEN Active Delay	1	25	ns	6)	13
29	CLK to AEN Inactive Delay	3		1115	0,	13, 14
30	CLK to LLOCK Delay	-	20	1	7)	18
31	RESET to LLOCK Delay		35		''	19
32	CLK to BCLK Setup Time	38	-]	8)	13,16, 20

- *) Preliminary
- 1) \overline{BREQ} load CL = 60 pF
- 2) BPRO load CL = 60 pF
- 3) BUSY load CL = 300 pF
- 4) Float condition occurs when output current is less than ILO in magnitude
- 5) \overline{CBRQ} load CL = 300 pF
- 6) \overline{AEN} load CL = 150 pF
- 7) $\overline{\text{LLOCK}}$ load CL = 60 pF
- 8) In actual use, CLK and BCLK are usually asynchronous to each other. However, for component testing purposes this specification is required to assure signal recognition at specific CLK and BCLK edges.
- 9) INIT is asynchronous to CLK and to BCLK. However, for component testing purposes, this specification is required to assure signal recognition at specific CLK and BCLK edges.

AC Characteristics SAB 82289-6

TA = 0 to 70°C, VCC = 5V $\pm 5\%$

AC timings are referenced to 0.8 and 2.0 V points of \approx ignals as illustrated in data sheet waveforms, unless otherwise noted.

Symbol	Parameter		values * MHz	Unit	Test condition	Shown in
		min.	max.			Figure
1	CLK Cycle Period	83	t5+50		_	
2	CLK Low Time	20	225		at 1.0 V	
3	CLK High Time	25	230		at 3.6 V	
4	CLK Rise/Fall Time	-	10		1.0 to 3.6 V	
5	BCLK Cycle Time	100	x			13
6	BCLK High/Low Time	30				
7	S0/HOLD, S1, M/IO Setup	28		ns		
8	\$0/HOLD, \$1, M/IO Hold	1		115		
9	READY Setup	50				
10	READY Hold Time	35			_	
11	LOCK, SYSB/RESB Setup Time	28				10.10
12	LOCK, SYSB/RESB Hold Time	1				13, 18
13	RESET Setup Time	28				
14	RESET Hold Time	1	-			19
15	RESET Active Pulse Width	16		CLKs		
16	INIT Setup Time	45			9)	
17	INIT Hold Time	1			3)	20
18	INIT Active Pulse Width	3 (t1) +3(t14)				
19	BUSY, BPRN, CBRQ, CBQLCK/ALWAYS Setup to BCLK (or to RESET)	20		ns	_	13,15, 21
20	BUSY, BPRN CBRQ, CBQLCK/ALWAYS Hold to BCLK (or to RESET)	1				
21	BCLK to BREQ Delay		30		1)	13, 14
22	BCLK to BPRO Delay	_	35	1	2)	17
23	BPRN to BPRO Delay		25	1	2)	17
24	BCLK to BUSY Active Delay	1	60	1	3)	13

For notes see next page.

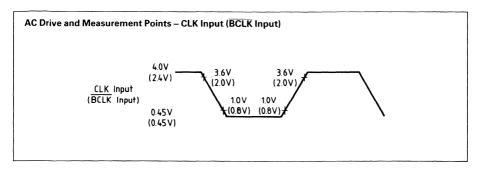
AC Characteristics SAB 82289-6 (continued)

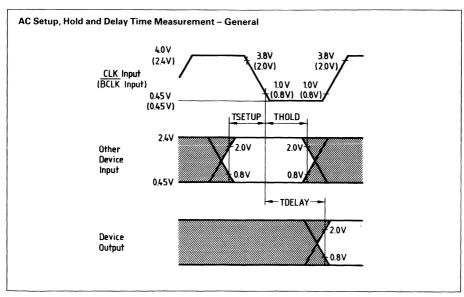
Symbol	Parameter	Limit values * 6 MHz		Unit	Test condition	Shown in
		min.	max.			Figure
25	BCLK to BUSY Float Delay		35		4)	13, 14
26	BCLK to CBRQ Active Delay]_	55		5)	13
27	BCLK to CBRQ Float Delay	1	35		4)	13, 20
28	BCLK to AEN Active Delay	1	25	ns	6)	13
29	CLK to AEN Inactive Delay	3				13, 14
30	CLK to LLOCK Delay	-	20		7)	18
31	RESET to LLOCK Delay		35		//	19
32	CLK to BCLK Setup Time	38	_		8)	13,16, 20

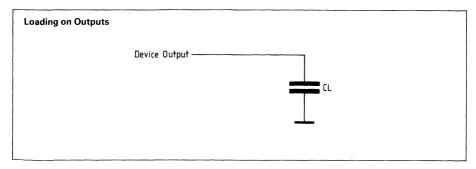
^{*)} Preliminary

- 1) BREQ load CL = 60 pF
- 2) BPRO load CL = 60 pF
- 3) BUSY load CL = 300 pF
- 4) Float condition occurs when output current is less than ILO in magnitude
- 5) CBRQ load CL = 300 pF
- 6) \overline{AEN} load CL = 150 pF
- 7) $\overline{\text{LLOCK}}$ load CL = 60 pF
- 8) In actual use, CLK and BCLK are usually asynchronous to each other. However, for component testing purposes this specification is required to assure signal recognition at specific CLK and BCLK edges.
- 9) INIT is asynchronous to CLK and to BCLK. However, for component testing purposes, this specification is required to assure signal recognition at specific CLK and BCLK edges.

AC Testing Waveforms







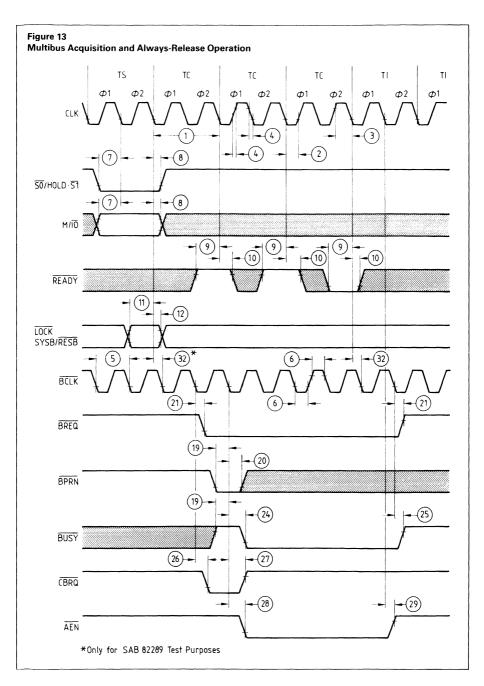
Waveforms

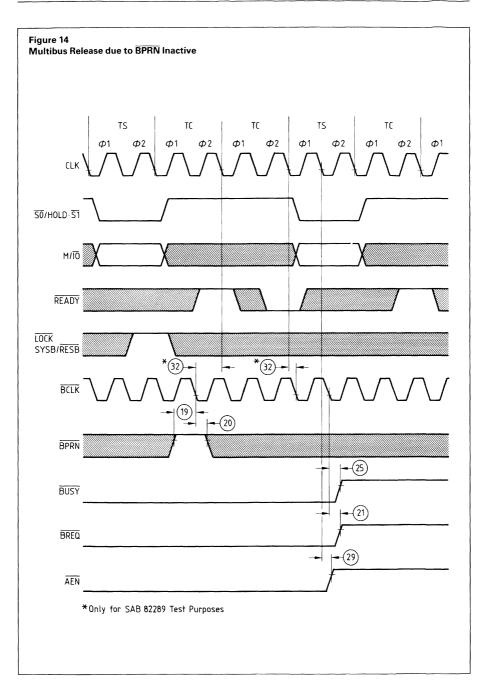
The waveforms (figures 13 to 21) show the timing relationships of the inputs and the outputs and do not show all possible transitions of all signals in all modes. Instead, all signal timing relationships are shown via the general cases. Special cases are shown when needed.

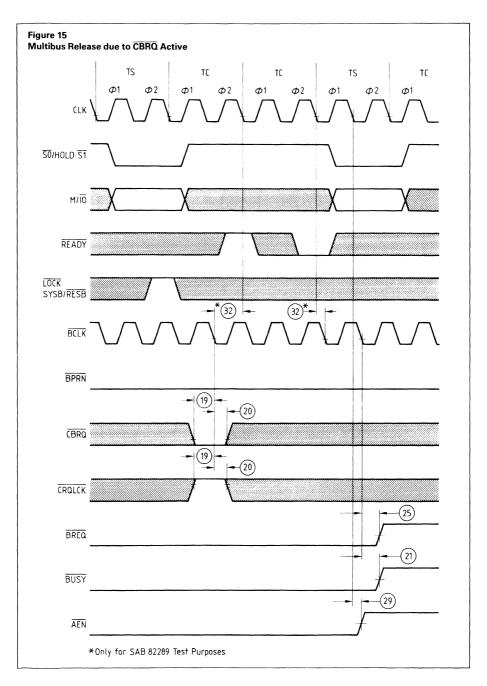
To find the timing specification for a signal transition in a particular mode, first look for a special case in the waveforms. If no special case applies, then use a timing specification for the same or related function in another mode.

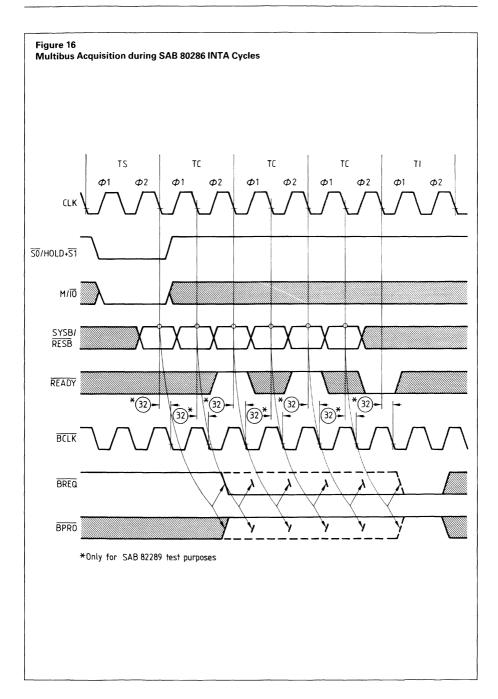
The SAB 82289 bus arbiter serves as an interface between the SAB 80286 subsystem which operates synchronously to the CLK signal and Multibus which operates synchronously to BCLK signal. CLK and BCLK generally operate asynchronously to each other and at different frequencies. Thus, the exact clock period in which an input synchronous to one clock will cause a response synchronous to the other clock depends on the relative phase and frequency of CLK and BCLK at the time the input is sensed.

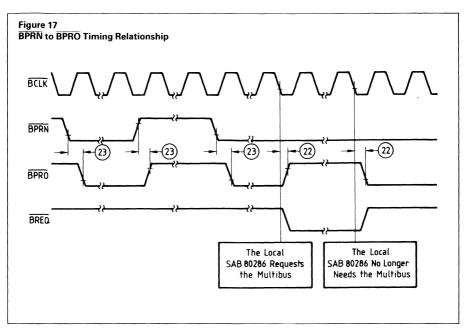
One strict relation between CLK and BCLK must be maintained for proper Multibus arbitration. If the CLK period is too long relative to BCLK period (t1 greater than t5 +50 ns), another arbiter could gain control of the system bus before this arbiter has released AEN synchronously to its CLK. This situation arises since the release of AEN is synchronous to the next falling CLK edge after the processor cycle ends but the release of BREO and BUSY is synchronous to the next falling BCLK edge after the processor cycle ends. In practice, any CLK frequency greater than 6.66 MHz (i.e. SAB 80286 processor speeds greater than 3.33 MHz) will avoid conflict with a 10 MHz BCLK. Therefore all SAB 80286 speed selections are Multibus compatible.

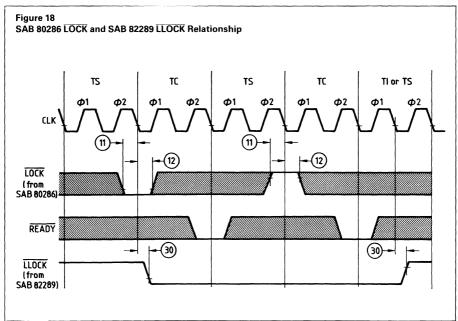


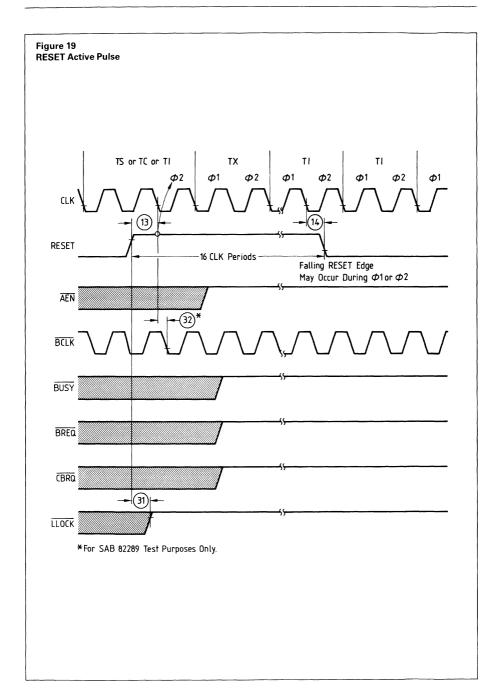


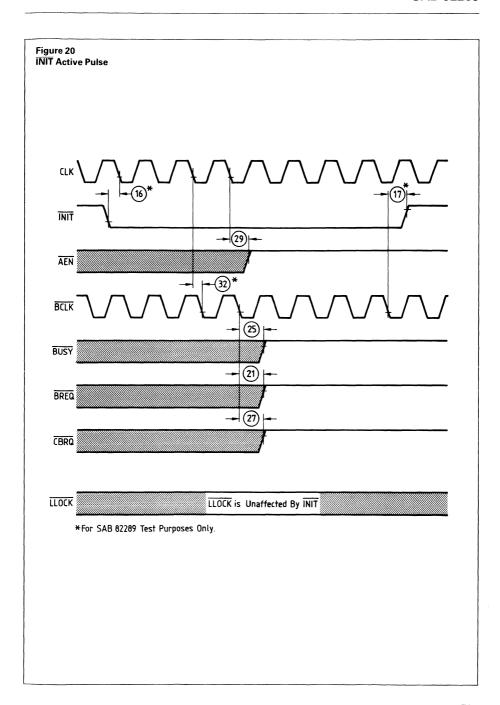


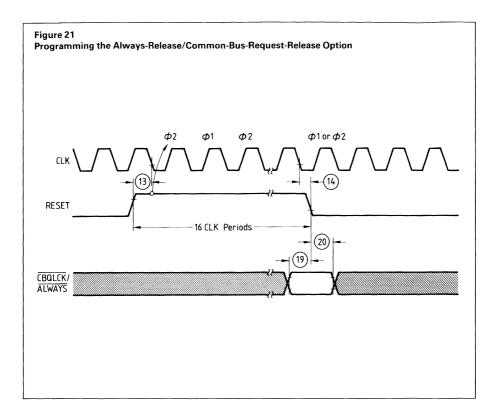




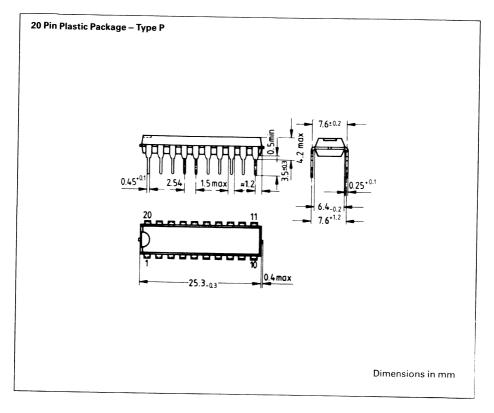








Package Outline



SAB 82289

Ordering Information

Туре	Description	Ordering code		
SAB 82289-P	Bus Arbiter 16 MHz (plastic)	Q67020-Y77		
SAB 82289-6-P	Bus Arbiter 12 MHz (plastic)	Q67120-Y111		

Advance Information

SAB 82520 High-Level Serial Communications Controller (HSCC)

- Two independent HDLC channels
- Implementation of the X.25 LAPB/LAPD protocol
- Programmable timeout and retry conditions
- FIFO buffer for efficient transfer of data packets
- Oscillator and DPLL for each channel
- Different modes for clock recovery and data encoding
- High-speed data rate (up to 4 MHz)

- Support of bus configuration by collision resolution
- Receive and transmit time slots
- 8-bit parallel micro interface
- CMOS technology and low power consumption
- Power-down mode with less than 2 mW
- Single +5V power supply

Pin configurat	tion		Pin name:	S
			AD0-7	Address Data Bus
			RTSA	Ready to Send, Channel A
AD4 🗖 1		28 🗀 AD3	CTSA	Clear to Send, Channel A
AD5 🗖 2		27 🗖 AD2	RxDA	Serial Data Receive, Channel A
AD6 □ 3		26 AD1	TxDA	Serial Data Transmit, Channel A
AD7 74		25 AD0	TxDB	Serial Data Transmit, Channel B
			RxDB	Serial Data Receive, Channel B
RTSA 5		24 🗀 RD	CTSB	Clear to Send, Channel B
CTSA 🗆 6		23 🗀 WR	RTSB	Ready to Send, Channel B
RxDA ☐ 7	SAB	22 🗀 VCC	RES	General Reset
TxDA □ 8	82520	21 🗖 RXCKA	INT	Interrupt, Open drain Output
TxDB 🖂 9		20 RXCKB	ALE	Address Latch Enable
RXDB 7 10		19 TxCKA	CS	Chip Select
CTSB [11			TxCKB	Transmit Clock, Channel B
7		18 TxCKB	TxCKA	Transmit Clock, Channel A
RTSB 🖂 12		17 🗀 CS	RxCKB	Receive Clock, Channel B
RES 🖂 13		16 🗀 ALE	RxCKA	Receive Clock, Channel A
GND 🗖 14		15 🗀 ĪNT	WR	Write Strobe
<u> </u>			RD	Read Strobe
			GND	Ground 0 V
			VCC	Power Supply +5V

The Siemens SAB 82520 High-Level Serial Communications Controller (HSCC) is designed to interface high-speed communications lines in point-to-point or point-to-multipoint configurations using HDLC protocols. It can be employed in X.25 LAPB or ISDN LAPD applications as well. Most of

the HDLC procedures are handled by the controller independently of the microprocessor.

The HSCC is a 28-pin DIL device fabricated using Siemens high-performance CMOS technology with low power consumption and power-down mode with less than 2 mW.

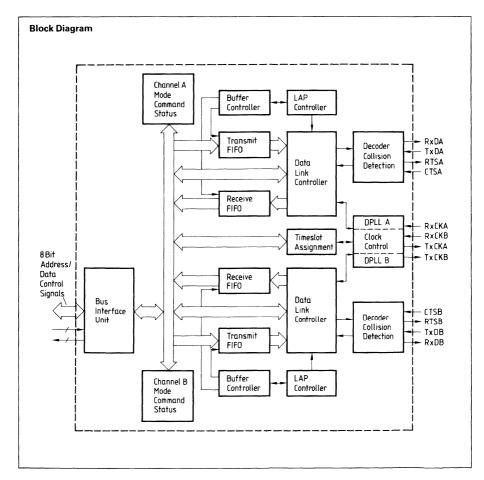
Functional Description

The HSCC SAB 82520 is designed to reduce software overhead of network communication and of high-speed communications lines (up to 4 MHz). The device is a X.25 LAPB/LAPD controller which handles most of the layer 2 communication procedures autonomously without microprocessor support. Both full-duplex serial HDLC channels are completely independent. The on-chip oscillator and digital phase locked loop (DPLL) circuitry drastically reduce the need of external clock recovery logic.

The HSCC supports point-to-point (combined stations) and point (primary)-to-multipoint (secondaries) connections. In a special mode data packets can be transmitted and received in programmable

time slots; therefore the HSCC is suitable for packetswitched networks. Specially for these applications the built-in collision resolution mechanism can be used in PCM highways.

The host interface of the HSCC is an 8-bit multiplexed address/data bus. For efficient transfer of messages FIFO buffers with 64 bytes per direction and channel are used. Due to the overlapping input/output modes the maximum message length is unlimited. Two short consecutive messages can be stored by the FIFO. Interrupt status registers inform the microprocessor about the status of the transmit and/or FIFO. Serial line diagnostics and general information are supported as well.



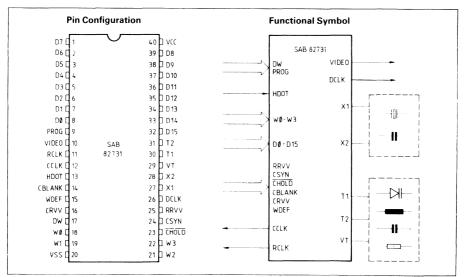


SAB 82731 Dot Rate Generator

A complete video interface between CRT Controller and CRT Display

SAB 82731 - 50 MHz SAB 82731-2 - 80 MHz

- Dot shift rates up to 80 MHz (SAB 82731-2).
- · Character length up to 16 dots
- Proportional character spacing supported
- Half dot shifts for character rounding
- Character attribute processing
- Single 5V power supply
- 40 pin DIP package
- Interface optimized for next generation of CRT controllers



The SAB 82731 is a general purpose video interface, which generates a video signal output for the CRT monitor from parallel character and attribute information coming from the character generator and the CRT controller. The SAB 82731

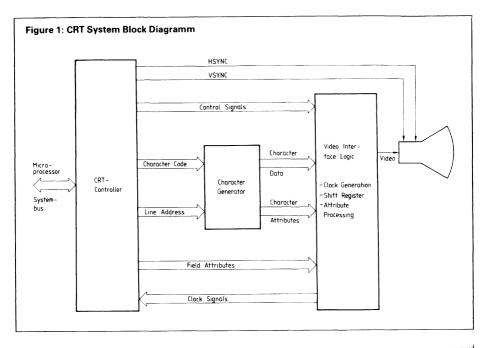
together with minimal hardware, comprises a complete video interface system for the CRT controller and the CRT monitor. The device is fabricated in a fast bipolar ASBC (Advanced Standard Buried Collector) process of Siemens.

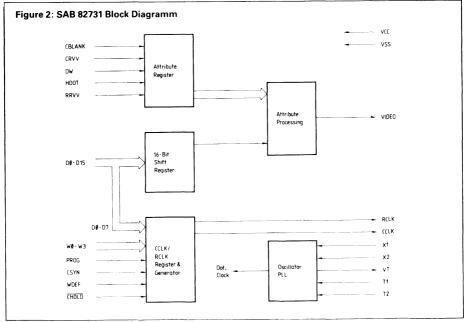
Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function				
DØ-D15	1-8, 32-39	1	Character data parallel inputs				
PROG	9	I	Program control input; used to program default width value of CCLK and width of RCLK; the default width value of CCLK and the width of RCLK are latched into the SAB 82731 via D0-D7 at the rising edge of CCLK (PROG is active high)				
VIDEO	10	0	Video output; provides the dot information clocked by the internal dot clock				
RCLK	11	0	Reference clock output; used to generate the timing for th screen columns for data formatting. The period of RCLK is programmable from 6 to 21 times the period of the interndot clock				
CCLK	12	0	Character clock output; used to clock character and attribut information out of the CRT controller. The period of CCLK is programmable from 3 to 18 times the period of the internal dot clock				
HDOT	13	ı	Half dot shift input; the video signal at the video output will be delayed by half dot clock for character rounding (active high)				
CBLANK	14	I	Character blank attribute input; the video output is blanked (active high)				
WDEF	15	1	Width defeat attribute input; the CCLK period is set to a preprogrammed default value (active high)				
CRVV	16	ı	Character reverse video attribute input; inverts the characte data from DØ-D15 (active high)				

Pin Definitions and Functions (continued)

Symbol	Number	Input (I) Output (O)	Function
DW 17 I		I	Double width attribute input; the internal dot clock frequency and the CCLK frequency are divided by two (active high). The RCLK frequency remains unchanged
WØ-W3	18, 19 21, 22	ı	Clock width inputs; they are used for programming the CCLK clock width on a character by character base
CHOLD	23	1	CCLK inhibit input; this signal suppresses the CCLK generation and is used for TAB function (active low)
CSYN	24	I	CCLK synchronization input; CCLK will be synchronized to RCLK and the video output signal is defined by RRVV (active high)
RRVV	25	1	Field reverse video input; the video signal at the video output will be inverted (active high)
DCLK	26	0	Dot clock output; ECL-level signal intended for test purposes only. Must be grounded via a 3.3k resistor if used
X1-X2	27, 28	1	Inputs for fundamental mode crystal; its frequency must be 1/8 of the required dot clock frequency
VT	29	0	Tuning voltage for PLL-VCO; this output is used to tune the LC-circuit and thus controls the oscillator frequency of the internal dot clock
T1-T2	30, 31	1	LC-circuit inputs for PLL-VCO. T1 can be used to provide the SAB 82731 with an external clock
VCC	40	-	+5V power supply
VSS	20	_	Ground (0V)





General Description

The dot rate generator, SAB 82731, in a typical CRT system shown in figure 1, interfaces the CRT controller to the CRT video terminal (Video Interface Logic). It receives the parallel data along with the attribute and control information from the CRT controller, processes it into a serial video signal which can be fed to a video CRT terminal. It also generates the basic dot clock (DCLK), character clock (CCLK) and reference clock (RCLK) signals. CCLK and RCLK are required by the CRT controller.

CRT terminals requiring very high resolution, extremely stable and absolutely flicker-free pictures, place special demands on the dot rate generator. In such applications very high dot rates up to 80 MHz are necessary. This leaves very little time per dot (pixel) to convert the data, attribute, and control information into serial form for the video terminal.

The functions of SAB 82731 are largely determined by the complexity and the demands of the CRT controller it supports. Figure 2 shows the block diagram of the dot rate generator. The dot clock is generated by a voltage controlled LC circuit connected at T1 and T2. Another clock is generated which is crystal controlled and has a frequency 1/8 of the dot clock. This is used to stabilize the dot clock using an on-chip phase locked loop (PLL). This two-oscillator concept enables the use of low cost, fundamental mode crystals.

The 16 bit shift register receives parallel inputs from pins D0-D15. This allows a maximum character width of 16 dots. The minimum width can be 3 dots. The character width is programmable on a character to character base through pins W0-W3 for proportional character spacing. This also determines the character clock (CCLK) frequency. Programming of the default character width and the reference clock (RCLK) is done through inputs D0-D7 and PROG. Signal WDEF can be used to switch between the default character width and the one specified dynamically through the lines WØ-W3. A special problem is encountered when using variable character width. For example, when tables are formatted on the screen it is essential that every entry in a column starts at the same dot distance (and not the character distance) from the start of line. This is directly supported by SAB 82731 providing a tabulator function using CHOLD signal.

It is possible to shift every line of characters by half a dot using the HDOT signal. This feature, known as character rounding, further enhances the quality of high resolution character display. Other features, like blinking of characters, reverse video which improves the readability of text on screen, are directly supported by SAB 82731 using signals CRVV and RRVV from the CRT controller, processing them and effecting the final video signal to show the characters with the desired attributes.

Functional Description

Clock Generation

The most fundamental clock required to run the CRT display is the dot clock which provides the reference for the dot data to be shifted serially to the CRT. In addition, it is basis for the character clock CCLK and the reference clock RCLK required by the CRT controllers.

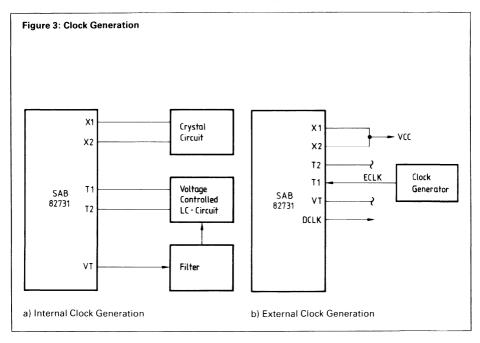
Dot Clock

The dot clock is derived from on-chip oscillator (T1, T2). Its frequency is determined by an external voltage controlled LC-circuit that has a center

frequency of about two times the desired dot clock frequency. Via the VT pin, the on-chip PLL circuit causes this oscillator to be locked to the 16th harmonic of the on-chip crystal oscillator (X1, X2) which is running at 1/8 of the dot clock frequency (see figure 3a).

Alternatively, the SAB 82731 can be supplied with an external TTL-level clock via T1 that must be two times the dot clock rate (see figure 3b).

The SAB 82731 provides the dot clock at the DCLK output. It is an ECL-level output and is intended for testing and adjustment purposes only.



Designing the Oscillator Circuit

The whole external oscillator circuit consists of three parts

- the crystal circuit,
- the voltage controlled LC-circuit and
- the loop filter for the PLL.

Figure 4a shows the general crystal circuit. The crystal must be a fundamental mode series resonant type with a resonant frequency of 1/8 of the desired dot clock frequency. The capacitor Cx is necessary if a fine adjustment of the dot clock rate must be done. Figure 4b shows as example how the dot clock frequency can vary with different values of Cx. The capacitors C1 and C2 may be necessary to suppress overtone oscillations if the crystal frequency is below 6 MHz. The exact values depend on the used crystal and must be determined in an empiric way. The recommended ranges are 1 to 10 nF for C1 and 0 to 100 pF for C2.

The voltage controlled LC-circuit is shown in figure 4c. The effective oscillating LC-circuit consists of the inductance L, the capacitance CD of the varactor diode, and the parasitic capacitance CP. Its resonant frequency is

$$fR = \frac{1}{2\pi \sqrt{L \cdot (CD + CP)}}$$

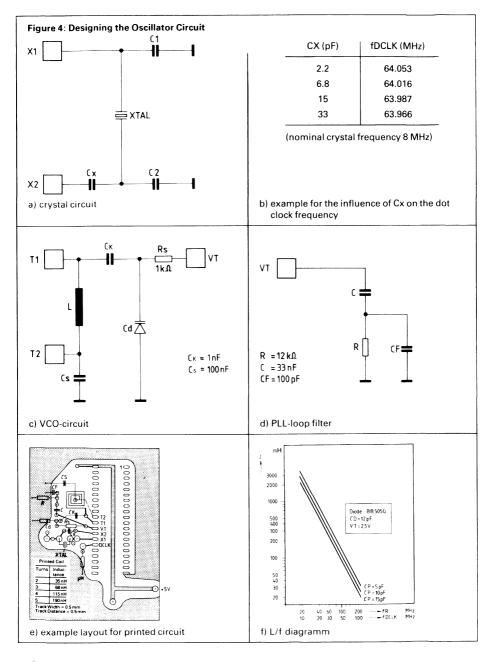
where fR must be 2 \times fDCLK. The value of CP depends on many factors (e.g. layout, single/multi-layer board ...), thus it changes from application to application. However a value of about 5 to 15 pF seems to be a good approximation.

The value of CD (capacitive diode) should be determined at a control voltage of 2.5V to get the lock-in-range as wide as possible. The variation of VT ranges from 1V to VCC-1 which results in a minimum frequency shift of about 6-8% with respect to the center frequency at 2.5V.

The value of the inductance L must be determined in such a way that the resulting center frequency lies as near as possible to the needed frequency fR = $2 \times fDCLK$ to guarantee a stable dot clock under all operation conditions. Figure 4f shows a diagram that will help you find the required inductance L. It is based on the use of the capacitive diode BB 505G that has a capacitance of 12 pF at a control voltage of 2.5V. The use of other diodes will, of course, lead to other diagrams.

At dot clock frequencies higher than 50 MHz the needed inductance becomes lower than 100 nH. In these cases, it is favorable to integrate the inductance into the board layout. Figure 4e shows a possible layout for the external oscillator circuit and approximate (measured) values of the inductance of the printed coil (track width and track distance 0.5 mm)

The loop filter converts the current pulses delivered by the PLL into the control voltage VT for the VCO. It is an essential part of the PLL and determines, for example, the lock-in-range and the control action of the PLL. A second-order filter that was found to work well under all operation conditions and over the full frequency range is shown in figure 4d.



Reference Clock (RCLK)

RCLK is the reference clock output used to generate the timing for the screen layout and to define screen columns for data formatting and tabulator locations. In addition, it is used to clock the field attribute signals into the SAB 82731. The period of RCLK is programmable from 6 to 21 times the period of the

dot clock, i.e. the RCLK high time is 3 dot clock periods and the RCLK low time is programmable from 3 to 18 dot clock periods. It is programmed via D4-D7 at the rising edge of CCLK, when PROG is active (see table and figure 5).

It is recommended to program the RCLK clock width only once after a system reset.

Programming table for the clock width of RCLK

D7	D6	D5	D4	PROG	RCLK period x dot clock period
0	0	0	0	1	16
0	0	0	1	1	17
0	0	1	0	1	18
0	0	1	1	1	19
0	1	0	0	1	20
0	1	0	1	1	21
0	1	1	0	1	6
0	1	1	1	1	7
1	0	0	0	1	8
1	0	0	1	1	9
1	0	1	0	1	10
1	0	1	1	1	11
1	1	0	0	1	12
1	1	0	1	1	13
1	1	1	0	1	14
1	1	1	1	1	15

Character Clock (CCLK)

CCLK is the fundamental character clock output used to clock character and attribute information out of the CRT controller and into the SAB 82731.

It is a rising edge triggered clock and inside the active character field its period is programmable from 3 to 18 times the period of the dot clock, i.e. the CCLK high time is 2 dot clock periods and the CCLK low time is programmable from 1 to 16 dot clock periods.

When CSYN is active (normally outside the active character field) CCLK is forced to match RCLK. In this case the CCLK high time is 3 dot clock periods instead of 2.

In order to support proportional spacing, the period of CCLK can be reprogrammed at the beginning of each CCLK cycle via the WØ-W3 inputs (i.e. at the beginning of each character) if PROG is inactive.

SAB 82731

Programming of the character width is done via the clock width inputs W0-W3 according to the programming table. The W0-W3 input data is clocked into the SAB 82731 at the rising edge of CCLK and defines the width of the currently displayed character (see figure 6).

If the width defeat attribute (WDEF) is active, the period of CCLK will be set to the programmed default value ignoring the clock width inputs W0-W3. This value is programmable from 3 to 18 times the period of the dot clock via the D0-D3 data inputs, when the PROG input is active (see figure 5).

It is recommended to programm the default CCLK clock width only once after a system reset.

The CCLK clock period will be doubled if the double width attribute (DW) is asserted.

Note:

If the width of CCLK is programmed to 17 or 18, zeros are shifted out from the internal shift register after the 16 data bits and displayed according to the attribute signal.

Programming table for the clock width of CCLK

PROG = 1	D3	D2	D1	DØ	
PROG = Ø	W3	W2	W1	WØ	CCLK clock period x dot clock period
	0	0	0	0	16
	0	0	0	1	17
	0	0	1	0	18
	0	0	1	1	3
	0	1	0	0	4
	0	1	0	1	5
	0	1	1	0	6
	0	1	1	1	7
	1	0	0	0	8
	1	0	0	1	9
	1	0	1	0	10
	1	0	1	1	11
	1	1	0	0	12
	1	1	0	1	13
	1	1	1	0	14
	1	1	1	1	15

Note:

PROG = 1: Programming the CCLK default clock width during the initialization phase via DØ-D3 at the rising edge of CCLK.

PROG = 0: Programming the clock width of the current CCLK cycle via W0-W3 at the rising edge of CCLK.

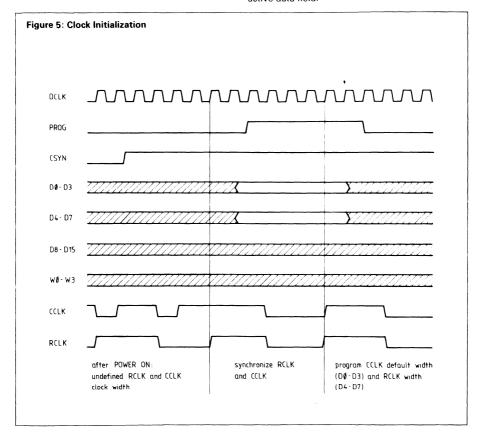
Clock Initialization Sequence (PROG)

After power on the width of RCLK is a random value between 6 and 21 and the width of CCLK is a random value between 3 and 18.

It is recommended to initialize the SAB 82731 in the following way:

- Activate the CSYN signal.
 CCLK is forced to match RCLK, which has a minimum clock width of 6 dot clock periods.
- Apply the clock width information to DØ-D3 and D4-D7 according to tables.
- Activate the PROG signal.
- The default width of CCLK and the width of RCLK are programmed at the next rising edge of CCLK (see figure 5).
- Remove the PROG signal

CSYN can be removed at the beginning of the next active data field.



Character Data Signals

The character data signals are normally provided by the character ROM and clocked into the SAB 82731 at the rising edge of CCLK.

The character data signals consist of

- the character data lines (DØ-D15),
- the character width information (WØ-W3) and
- the half dot shift signal (HDOT).

Dot Data (D0-D15)

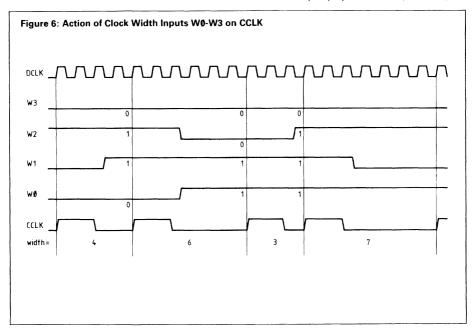
The dot data signals will be clocked into the SAB 82731 via the D0-D15 inputs at the rising edge of CCLK. The actually used inputs are defined by the

W0–W3 inputs or the internally latched default width information previously programmed. The dot data will be displayed dependent on the control signals and on the corresponding attribute information. The data are serially shifted out at the video output starting with DØ.

If CCLK width is greater than 16, zeros are shifted out for the rest of the dot clocks and displayed according to the attribute signals.

Character Width (WØ-W3)

The W0-W3 inputs are clocked into the SAB 82731 at the rising edge of CCLK and determine the width of the currently displayed character (see CCLK).



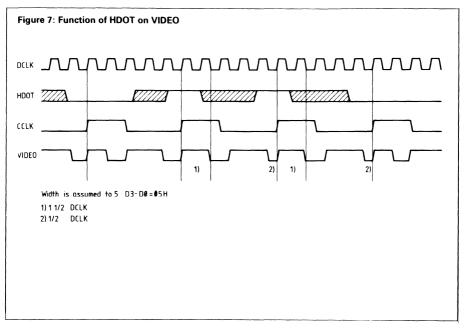
Half Dot Shift (HDOT)

The half dot shift character data signal is clocked into the SAB 82731 at the rising edge of CCLK. When the half dot shift signal is active (high), the output of the displayed data will be delayed by half a dot line. The first dot of the character dot line is transmitted during one and a half dot clock period while the last dot of this character dot line is displayed for half a dot clock period only. The remaining character dots are transmitted within one dot clock

period and thus the whole character dots are shifted by half a dot.

The HDOT signal is no character attribute signal, because it can change from dot line to dot line of a character. Thus it is reasonable to generate it from the character ROM together with the dot data and the width information.

Note that only the character dot line to which the HDOT signal is attached is effected.



Character Attribute Signals

These signals are clocked into the SAB 82731 at the rising edge of CCLK. Thus they are valid for the next character only.

The character attribute signals consist of:

character blanking
 character reverse video
 double width
 width defeat

WDEF.

Outside the active character field (which is defined by the CSYN signal) all character attribute signals are ignored.

Character Blanking (CBLANK)

The CBLANK input is clocked into the SAB 82731 at the rising edge of CCLK. If active (high), the blank attribute will produce the effect of blanking the display of the character. When the CBLANK attribute is active the corresponding dot data information D0-D15 will be as if all zeros where forced at the inputs. The video output can be inverted to all ones by simultaneously activating the CRVV attribute. Independent of these character oriented operations the video output signal is also effected by the RRVV field attribute signal.

Although the CBLANK signal is normally a character attribute, it may change from dot line to dot line of a character. Thus together with the CRVV signal one or more underlines or cursors can be generated controlled by the CRT controller.

Character Reverse Video (CRVV)

The CRVV input is clocked into the SAB 82731 at the rising edge of CCLK. It is an active high signal. In the character field, the CRVV attribute will produce the effect of reversing the polarity of the display during the transmission of the current character. CRVV is also effective together with the CBLANK attribute (see CBLANK description) and the RRVV signal.

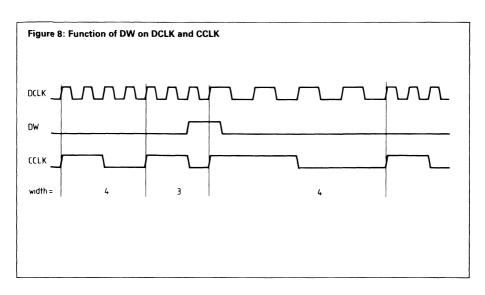
Outside the character field, the CRVV attribute is ingnored. Although the CRVV signal normally is a character attribute signal it may change from dot line to dot line of a character in order to support underlines or cursors.

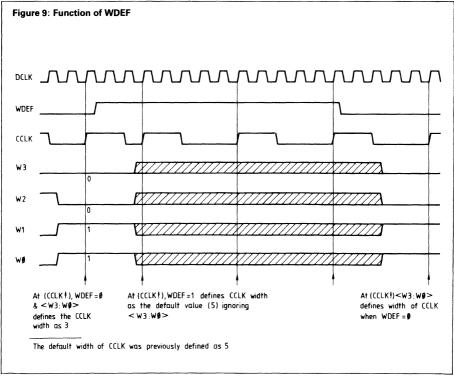
Double Width (DW)

The DW input is clocked into the SAB 82731 at the rising edge of CCLK. The dot clock frequency and the CCLK frequency will be halved when the double width attribute is active (high), producing characters that are twice as wide. The period of RCLK is not changed (see figure 8).

Width Defeat (WDEF)

The WDEF attribute signal is clocked into the SAB 82731 at the rising edge of CCLK. When the width defeat attribute is active (high), the width of CCLK will be set to a default width value previously programmed (see figure 9).





Field Attribute Signals

The field attribute signals are clocked into the SAB 82731 with the rising edge of RCLK. Thus the attributes are valid for a specific part of the screen independent of how many characters are displayed within this part.

The SAB 82731 supports two field attributes:

- field reverse video RRVV and
- clock synchronization CSYN.

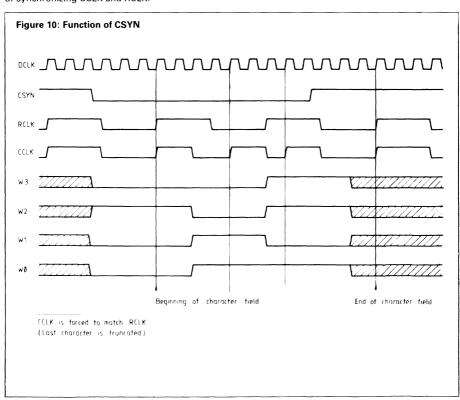
Field Reverse Video (RRVV)

The RRVV control signal is clocked into the SAB 82731 at the rising edge of RCLK. It immediately effects the display by the polarity of the video output in both the character field and the border of the display. It is an active high signal.

Clock Synchronization (CSYN)

CSYN is a field attribute signal, because it defines the active character field in addition to its function of synchronizing CCLK and RCLK. With a low level of CSYN (deactivated) clocked into the SAB 82731 with the rising edge of RCLK, the beginning of the character field area is defined (see figure 10) and the first character will be displayed. At the next rising edge of RCLK after CSYN is activated (i.e. at the end of the character field), the video output is forced to zero or, if the RRVV control signal is active, to a high level. The currently transmitted character will be truncated at this location. At the same time, CCLK will be forced to match RCLK starting with the next rising edge of RCLK (see figure 10). While CSYN is active all character attribute and data signals are ignored and only the field reverse video signal is effecting the video output.

Before the deactivation of CSYN, the data and attribute pipeline has to be filled by the CRT controller with the information of the first character.



Tabulator Function

The SAB 82731 supports tabulator functions by providing the CHOLD (character clock inhibit) input.

CCLK Inhibit (CHOLD)

When the CHOLD signal is activated (low) it inhibits the CCLK clock and thus freezes the information pipeline between CRT-controller and SAB 82731 until the next tabulator location is reached. CHOLD has to be activated simultaneously with the display of the TAB-character. If the TAB-character doesn't consist of all zeros, it must be blanked by activating CBLANK.

The width of the TAB-character can be determined by W0-W3 or by activating WDEF.

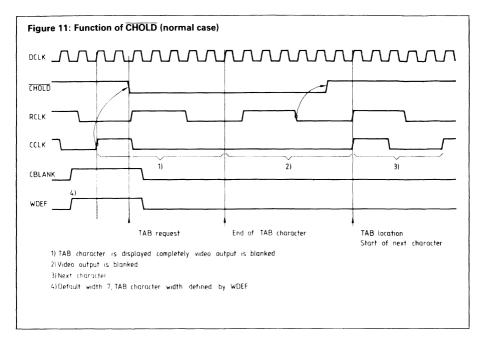
The CHOLD-signal is provided by the CRT-controller and it is assumed to be triggered with the leading edge of CCLK (figure 11). With the same edge of CCLK, the TAB-character will be latched into the SAB 82731. Thereby the attributes CBLANK and WDEF must be active if used. Thus the TAB-character will be displayed completely and the CCLK will be inhibited until reaching the specified tabulator location, which is defined by CHOLD inactive (high) at the rising edge of RCLK. In the timing diagrams it is assumed that CHOLD is deactivated by the trailing edge of RCLK. Figure 11 shows the normal case where the display of the TAB-character is finished before the deactivation of CHOLD. The gap between the TAB-location and the

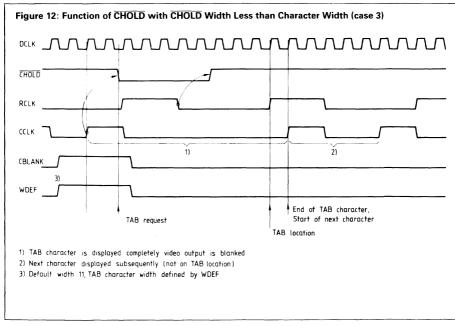
following character is normally blanked. In this scheme the TAB-character will be handled by the SAB 82731 like any other character (attribute processing is done quite normally).

In case of CHOLD active width being less than the TAB-character width the TAB-character will also be displayed completely. However, we have to distinguish three different cases:

- TAB-character is terminated before reaching TAB-location. The next character will be displayed as described before. In the gap the video output is normally blanked.
- TAB-character is finished exactly at the TABlocation. The next character will be displayed immediately without delay.
- 3) TAB-character is not terminated when reaching the TAB-location (see figure 12). The following character will be displayed subsequently after the display of the TAB-character (i.e. the start of the following character is not at the TABlocation).

If the CHOLD signal is not deactivated the video output will be continuously blanked. In the gap between the end of the TAB-character and the TAB-location all character attribute signals will have no effect on the video output signal. If the RRVV control signal is active the video output signal is inverted.

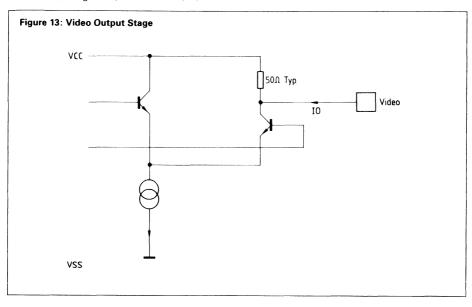


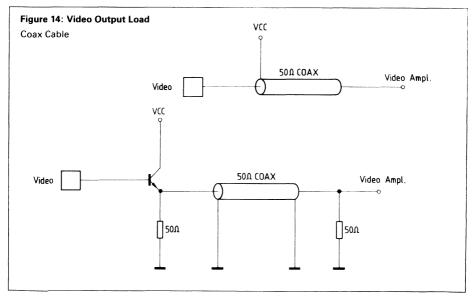


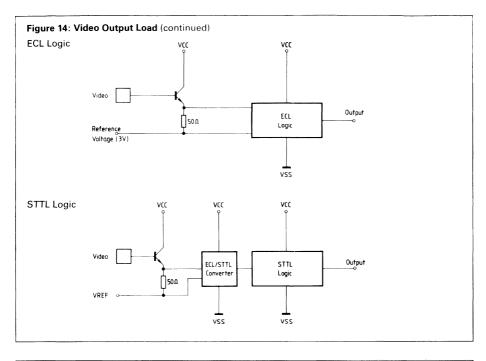
Video Output

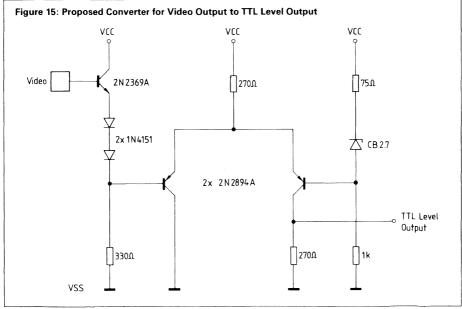
The video output provides an ECL oriented signal (see figure 13) and is matched to drive a 50 Ohm coax cable (see figure 14). In case of external

attribute processing the external logic can be ECL- or STTL-compatible.









Absolute Maximum Ratings¹)

Temperature under bias $0 \text{ to } + 70^{\circ}\text{C}$ Storage Temperature $-65 \text{ to } + 150^{\circ}\text{C}$ All output and supply voltages -0.5V to + 6VAll input voltages -0.5V to + 5.5VPower dissipation 1.5 Watts

D.C. Characteristics

TA = 0 to 70°C; VCC = $5V \pm 10\%$

Symbol	Parameter	Limit	values	Unit	Test conditions
	i didiffeter	Min.	Max.	Offic	rest conditions
VC	Input clamp voltage		-1	v	IC = -5 mA
IIL	Forward input current]-	-0.7	mA	VIL = 0.5 V
IIH	Reverse input current]-	50	μА	VIH = VCC
VOL	Output low voltage				
	CCLK		0.5	v	IOL = 8 mA
	RCLK		0.5		IOL = 4 mA
	VIDEO	VCC-1.2V	VCC-0.6V	-	IOL = 0
VOH	Output high voltage	Manager William Co.			
	CCLK, RCLK	2.4	-	v	IOH = -400 μA
	VIDEO	VCC-0.2V	vcc	-	IOL = 0
VIL	Input low voltage	-	0.8	.,	
VIH	Input high voltage	2.0	_	V	_
ICC	Power supply current	-	250	mA	2)
ZO	Output impedance VIDEO	40	70	Ohms	_
CIN	Input capacitance	-	15	pF	fc = 1 MHz

¹⁾ Stresses above those listed under "absolute maximum ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

²) All outputs open; VCC = 5V; TA = 25°C.

A.C. Characteristics

TA = 0 to 70°C; VCC = $5V \pm 10\%$

			Limit	values			
Symbol	Parameter	SAE	82731	SAB 82731-2		Unit	Test conditions
		Min.	Max.	Min.	Max.		
tDHDH	DCLK cycle period	20	125			ns	_
tCHCH	CCLK cycle period	3	18			tDHDH	
tCLCH	CCLK low time	tDHDH - 10	16 tDHDH +20				
tCHCL	CCLK high time	2 tDHDH -20	-			ns	
tRHRH	RCLK cycle period	6	21			tDHDH	
tRLRH	RCLK low time	3 tDHDH 10	18 tDHDH +20				
tRHRL	RCLK high time	3 tDHDH -20					
tDVCH	Data and attribute input set up time	30		1)			Fig. 16
tCHDX	Data and attribute input hold time	0					
tHLTE	CHOLD active before end of TABchar.	30	_			ns	
tHLHH	CHOLD pulse width	20					
tHHRH	CHOLD inactive set up before rising edge of RCLK	30					
tHLRH	CHOLD inactive hold time after rising edge of RCLK	0					

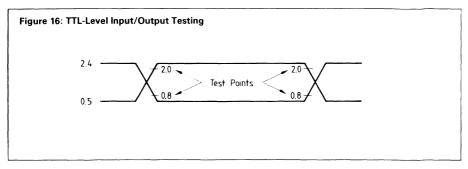
¹⁾ Not yet specified

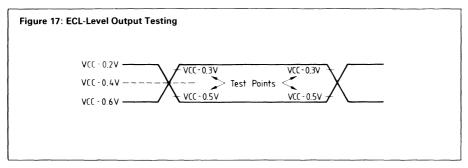
A.C. Characteristics (continued)

	Parameter		Lim	Unit	Test conditions		
Symbol		SAB 82731				SAB 82731-2	
		Min.	Max.	Min.	Max.		
tCHVV	Video output valid after rising edge of CCLK		6				_
tOLOH	TTL-output rise time	1					
tOHOL	TTL-output fall time	1-	10	1)	1)		Fig. 16
tVLVH	Video output rise time		3				Fig. 17
tVHVL	Video output fall time		3				

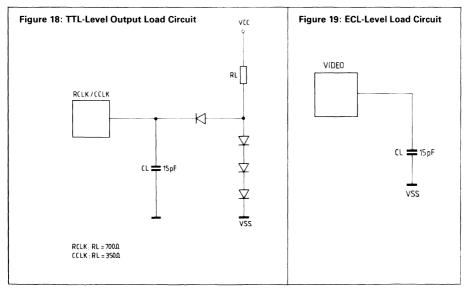
¹⁾ Not yet specified

A.C. Testing Waveforms

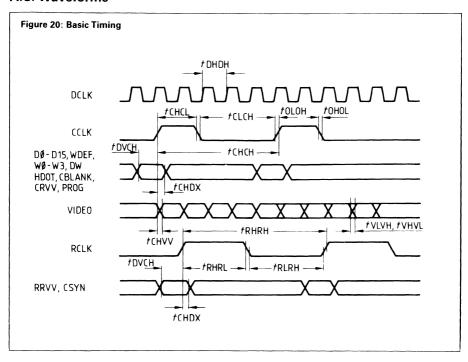


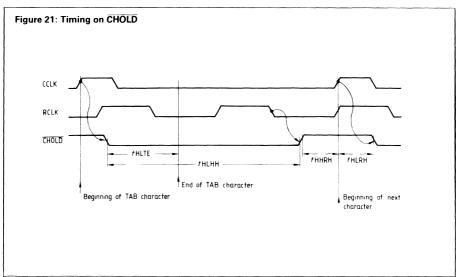


A.C. Testing Load Circuits

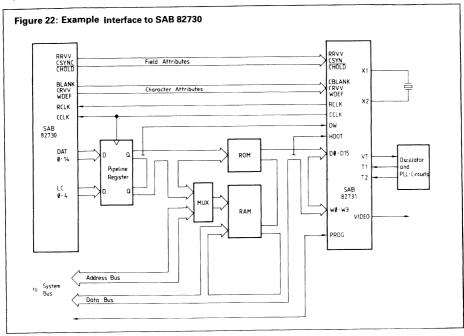


A.C. Waveforms

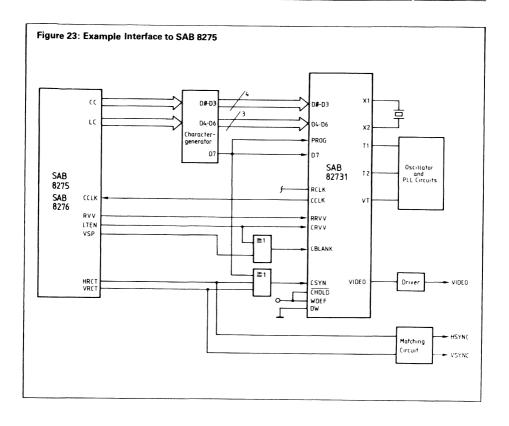




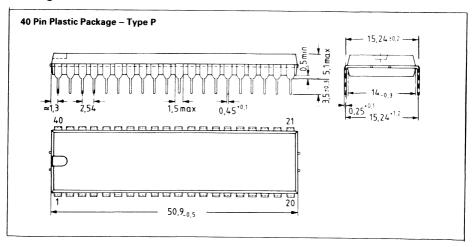
Application Examples



RAM or ROM may be selected either by addresses or by control signals. For pipeline register use positive edge triggered D-Flipflops (non-transparent latch) like SN 74374.



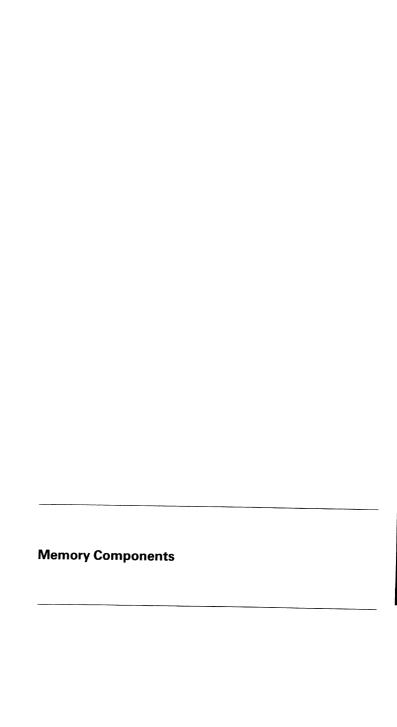
Package Outline



SAB 82731

Ordering Information

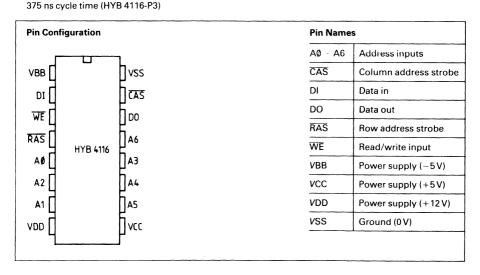
Туре	Description	Ordering code
SAB 82731-P	Dot rate generator 50 MHz; plastic package	Q67020-Y114
SAB 82731-2-P	Dot rate generator 80 MHz; plastic package	Q67020-Y118



HYB 4116-2, HYB 4116-3 16,384-Bit Dynamic Random Access Memory (RAM)

- Fully decoded,
 16,384 X1 bit organization
- · Separate data input and output
- All inputs including clocks TTL compatible
- Low power dissipation 462 mW active, 20 mW standby 150 ns access time, 320 ns cycle time (HYB 4116-P2) 200 ns access time.

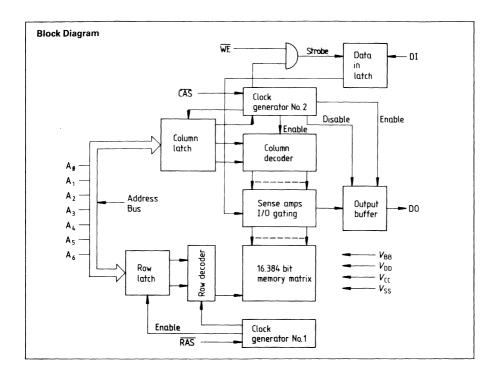
- Three-state output, 2 TTL loads
- Compatible with MK 4116
- 128 refresh cycles
- · Data output is unlatched



The HYB 4116 manufactured by Siemens is a dynamic random access memory built in N-channel silicon gate technology, using double layer polysilicon.

The dynamic one-transistor cell ensures high packing density and high speed. Moreover, multiplexing of the address signals permits the use of the space-saving 16-pin dual in-line package.

12.83



Functional Description

Addressing (AØ-A6)

For selecting one of the 16,384 memory cells, a total of 14 address bits is required which is consecutively applied via pins AØ to A6 by means of two strobes (address multiplexing). First the seven row addresses are called up and accepted with strobe RAS into the row select buffer. Following this, the seven column addresses are deposited in the column select buffer with CAS. It should be noted that the address signals are available in their steady-state condition at the time of the negative pulse edge of RAS and CAS, respectively.
RAS and CAS determine the starting point of the internal clock control.

RAS initiates row decoding and activates the read amplifier. CAS controls column decoding as well as the data input and output amplifiers.

Read write (WE)

Read and write operations are executed when the write enable signal \overline{WE} is at "H" or "L". Data input DI is disabled as long as reading takes place. The shortest write cycle time is obtained when \overline{WE} goes to logic "L" ahead of or simultaneously with \overline{CAS} ("early write"). The write data is then accepted into the input data memory by means of \overline{CAS} .

Delayed writing, read-modify-write

If writing or read-modify-write is delayed, \overline{CAS} is already at logic "L" so that the write data is transferred to the input data memory with the subsequent \overline{WE} signal.

Data input (DI)

Data can be input during a write or a read-modify-write cycle. The strobe for the data input is the last one of signals $\overline{\text{WE}}$ or $\overline{\text{CAS}}$ to make its negative transition.

Data output (DO)

The data output may assume three states (Tri-state logic) and is rated for driving two TTL loads. As against the output data the input data is not inverted.

In a read cycle the read data is available after access time tCAC referred to CAS. At the end of the read cycle, when CAS is again "H", the data output assumes again the high impedance condition. In the case of read-modify-write the data output contains the data read from the selected cell as in the read cycle. For "early write" the output pin assumes a high impedance troughout the entire cycle.

Refresh cycle

To prevent data in the dynamic memory cells from getting lost, each row address must be called up at least every two milliseconds. A total of 128 refresh cycles must be executed for all row addresses during this 2 millisecond period.

During writing or reading the data in the 128 memory cells of a row-line is automatically refreshed.

Precharge cycle

After power is applied to the device, the HYB 4116 requires several cycles before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

Absolute Maximum Ratings *)

D.C. Characteristics 1)

 $T_{A} = 0 \text{ to } 70 \, ^{\circ}\text{C}; \ V_{SS} = 0 \, \text{V}, \ V_{DD} = +12 \, \text{V} \pm 10\%, \ V_{BB} = -5 \, \text{V} \pm 10\%, \ V_{CC} = +5 \, \text{V} \pm 10\%$

	Peremeter	Limit	Limit Values		T4 C - 1'4'	
Symbol	Parameter	Min.	Max.	Units	Test Conditions	
V _{IH}	High level input voltage, (all inputs except RAS, CAS, WRITE) 2)	2.4	7.0		_	
V _{IHC}	High level input voltage (RAS, CAS, WRITE) 2)	2.4	7.0	v		
V _{IL}	Low level input voltage 2)	-1.0	0.8			
V _{OH}	Output high voltage	2.4	V _{CC}		$I_{\rm O} = -5 \mathrm{mA}$	
V _{OL}	Output low voltage	_	0.4		$I_{\rm O} = 4.2 \; {\rm mA}$	
I _{DD 1}	Average V _{DD} supply current ³⁾	_	35		_	
I _{DD 2}	Standby V _{DD} supply current	-	1.5	mA	RAS at V _{IH} CAS at V _{IH}	
I _{DD 3}	Average V _{DD} current during refresh ³⁾	-	27		RAS cycling CAS at V _{IH}	
I _{I (L)}	Input leakage current (any input) 4)	-10	10		_	
I _{O (L)}	Output leakage current	- 10	10		$\overline{\text{CAS}}$ at V_{IH} $V_{\text{O}} = V_{\text{SS}}$ to V_{CC}	
$I_{\rm CC}$	V _{CC} supply current ⁵⁾	-10	10	μΑ	CAS at V _{IH} RAS at V _{IH}	
I _{BB 1}	Average V _{BB} power supply current	-	200		_	
I _{BB 2}	Standby $V_{\rm BB}$ power supply current	-	100			

^{*)} Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

Symbol	Parameter	Limit	Limit Values			
		Min.	Max.	Units	Test Conditions	
C _{1 1}	Input capacitance ⁶⁾ (A ₀ – A ₆), DI	_	5			
C ₁₂	Input capacitance ⁶⁾ RAS, CAS, WRITE	-	10	pF	_	
Co	Output capacitance 6)	_	7	1	DO disabled	

- 1) The only requirement for the sequence of applying voltage to the device is that $V_{\rm DD}$, $V_{\rm CC}$ and $V_{\rm SS}$ should never be 0.3 V more negative than $V_{\rm BB}$.
- Over- and undershooting on input levels of 6.5 V or -2 V for a period of 30 ns will not influence function and reliability of the device.
- 3) $I_{\rm DD}$ depends on frequency of operation. Maximum current is measured at the fastest cycle rate.
- 4) All device pins at 0 V except V_{BB} at -5 V and pin under test which is at +7 V.
- 5) $V_{\rm CC}$ is connected to output buffer only.
- 6) Effective capacitance calculated from the equation

equation
$$C = \frac{I \cdot \Delta t}{\Delta V} \text{ with } \Delta V = 3 \text{ V}.$$

A.C. Characteristics 1)

 $\textit{T}_{A}=0$ to +70 °C; $\textit{V}_{SS}=$ 0V; $\textit{V}_{DD}=$ 12 V $\pm10\%$; $\textit{V}_{BB}=-5\,\text{V}$ $\pm10\%$; $\textit{V}_{CC}=+5\,\text{V}$ $\pm10\%$

Symbol	Parameter		Limit	Values		Units
Symbol	r alailletel	HYB	4116-P2	HYB	4116-P3	Jillis
		Min.	Max.	Min.	Max.	
t _{RC}	Random read or write cycle time 2)	320	_	375	-	
t _{RWC}	Read/write cycle time 2)	320	_	375	-	
t _{RMWC}	Read/modify/write cycle time 2)	320	_	405	-	
t _{RAC}	Access time from RAS 3) 4)	-	150	-	200	
t_{CAC}	Access time from CAS 3) 5)	-	100	-	135	
t _{OFF}	Output buffer turn-off delay 6)	-	40	0	50	
t _{RP}	RAS precharge time	100	-	120	-	
t _{RAS}	RAS pulse width	150	10 ⁴	200	10 ⁴	
t _{RSH}	RAS hold time	100	-	135	-	
t _{CSH}	CAS hold time	150	-	200	-	ns
t _{CAS}	CAS pulse width	100	-	135	-	
t_{RCD}	RAS to CAS delay time 7)	20	50	25	65	
t _{ASR}	Row address set-up time	0	-	0	-	
t _{RAH}	Row address hold time	20	-	25	-	
t _{ASC}	Column address set-up time	-5	-	-10	-	
t _{CAH}	Column address hold time	45	_	55	-	
t_{AR}	Column address hold time referenced to RAS	95	_	120	-	
t _T	Transition time (rise and fall)	3	35	3	50	
t _{RCS}	Read command set-up time (RMW)	0	-	0	-	
t_{RCH}	Read command hold time	0	1-	0	-	
t _{wch}	Write command hold time	45	-	55	-	
t _{wcr}	Write command hold time referenced to RAS	95	-	120	1-	
t _{wcs}	Write command set-up time 8)	-20	1-	-20	1-	

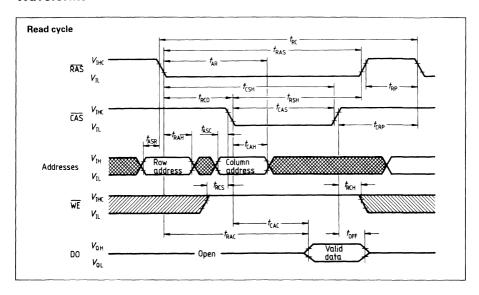
Cumbal	Parameter		Limit Values					
Symbol	rarameter	HYB 4	1116-P2	HYB 4	116-P3	Units		
		Min.	Max.	Min.	Max.			
t_{WP}	Write command pulse width	45	Ī-	55	_			
t _{RWL}	Write command to RAS lead time	50	-	70	-			
t _{CWL}	Write command to CAS lead time	50	-	70	-			
t_{DS}	Data in set-up time	0	-	0	-	ns		
t_{DH}	Data in hold time 9)	45	-	55	-	1		
t _{DHR}	Data in hold time 9) referenced to RAS	95	-	120	-			
t _{CRP}	CAS to RAS precharge time	-20	-	-20	-			
t _{RF}	Refresh period	-	2.0	-	2.0	ms		
t_{CWD}	CAS to WE delay 8)	60	-	95	-	ns		
t _{RWD}	RAS to WE delay 8)	110	_	160	-	1		

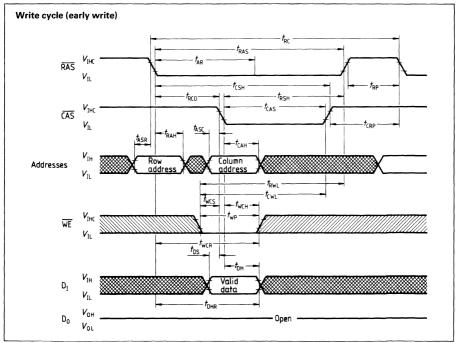
Notes:

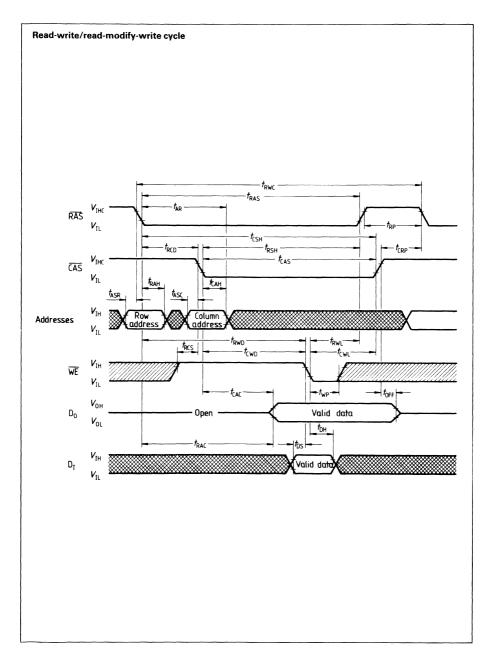
- V_{IHC (min)} or V_{IH (min)} and V_{IL (min)} are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
- The specifications for t_{RC (min)} and t_{RWC (min)} are used only to indicate cycle time at which proper operation over full temperature range (0 °C ≤ T_A ≤ 70 °C) is assured.
- 3) Measured with a load equivalent to two TTL loads and 100 pF.
- 4) Assumes that t_{RCD} ≤ t_{RCD (max)}. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
- 5) Assumes that $t_{RCD} \ge t_{RCD \text{ (max)}}$.
- 6) t_{OFF (max)} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- 7) Operation within the t_{RCD (max)} limit ensures that t_{RAC (max)} can be met. t_{RCD (max)} is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD (max)} limit, then access time is controlled exclusively by t_{CAC}.

- 8) t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If t_{WCS} ≥ t_{CWS(min)}, the cycle is an early write cycle and the data-out pin will remain open circuit (high impedance) throughout the entire cycle: if t_{CWD} ≥ t_{CWD (min)} and t_{RWD} ≥ t_{RWD (min)} the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
- 9) t_{DS} and t_{DH} are referenced to the leading edge of CAS in early write cycles, and to the leading edge of WE in delayed write or read-modify-write cycles.

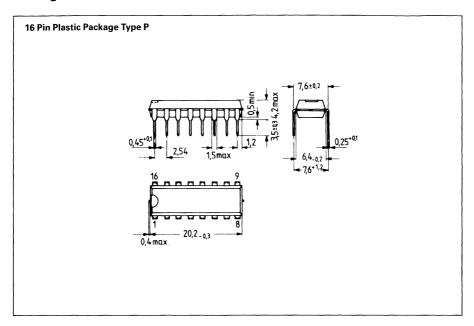
Waveforms







Package Outline



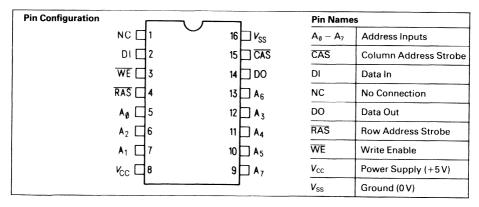
Ordering Information

Туре	Description	Ordering Code
HYB 4116-P 2	RAM (Plastic; 150 ns)	Q67100-Q308
HYB 4116-P 3	RAM (Plastic; 200 ns)	Q67100-Q306

HYB 4164-P1, HYB 4164-P2, HYB 4164-P3 65,536-Bit Dynamic Random Access Memory (RAM)

- 65,536 X1 bit organization
- Industry standard 16-pin JEDEC configuration
- Single +5 V ±10% power supply
- · Low power dissipation
 - 150 mW active (max.)
 - 20 mW standby (max.)
- 120 ns access time,
 220 ns cycle (HYB 4164-P1)
 150 ns access time,
 280 ns cycle (HYB 4164-P2)
 200 ns access time,
 330 ns cycle (HYB 4164-P3)

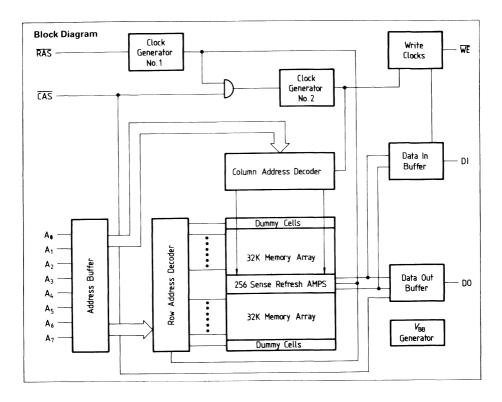
- · All inputs and outputs TTL compatible
- High over- and undershooting capability on all inputs
- · Low supply current transients
- CAS controlled output providing latched or unlatched data
- Common I/O capability using "early write" operation
- Read-Modify-Write, RAS-only refresh, hidden refresh
- 256 refresh cycles with 4 ms refresh period
- Page Mode Read and Write



The HYB 4164 is a 65536-words by 1-bit, MOS random access memory circuit fabricated with Siemens new 5-Volt only N-channel silicon gate technology, using double layer polysilicon. To protect the chip against α -radiation a Siemens proprietary chip cover is used. The HYB 4164 uses single transistor dynamic storage cells and dynamic control circuitry to achieve high speed at very low power dissipation.

Multiplexed address inputs permit the HYB 4164 to be packaged in an industry standard 16-pin dualin-line package. System oriented features include single power supply with $\pm 10\%$ tolerance, on-chip address and data latches which eliminate the need for interface registers and fully TTL compatible inputs and outputs, including clock inputs.

In addition to the usual read, write and read-modify-write cycles, the HYB 4164 is capable of early and delayed write cycles, RAS-only refresh and hidden refresh. Common I/O capability is given by using "early write" operation.



Functional Description

Adressing (A₆-A₇)

For selecting one of the 65536 memory cells, a total of 16 address bits are required. First 8 row-address bits are set-up on pins A_0 to A_7 and latched onto the row address latches by the Row Address Strobe (\$\overline{RAS}\$). Then the 8 column address bits are set-up on pins A_0 through A_7 and latched onto the column address latches by the Column Address Strobe (\$\overline{CAS}\$). All input addresses must be stable on or shortly after the falling edge of \$\overline{RAS}\$ and \$\overline{CAS}\$ respectively. \$\overline{CAS}\$ is internally gated by \$\overline{RAS}\$ to permit triggering of column address latches as soon as the Row Address Hold Time (\$t_{RAH}\$) specification has been satisfied and the address inputs have been changed from row-address to column-address.

It should be noted that \overline{RAS} is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. \overline{CAS} is used as a chip select activating the column decoder and the input and output buffers.

Write Enable (WE)

The read or write mode is selected with the \overline{WE} input. A logic high (V_{IH}) on \overline{WE} dictates read mode; logic low (V_{IL}) dictates write mode. The data input is disabled when the read mode is selected. When \overline{WE} goes low prior to \overline{CAS} , data output (DO) will remain in the high-impedance state for the entire cycle permitting common I/O operation.

Data Input (DI)

Data is written during a write or read-modify-write cycle. The falling edge of \overline{CAS} or \overline{WE} strobes data into the on-chip data latch. In an early write cycle \overline{WE} is brought low prior to \overline{CAS} and the data is strobed in by \overline{CAS} with set-up and hold times referenced to this signal. In a delayed write or read-modify-write cycle, \overline{CAS} will already be low, thus the data will be strobed in by \overline{WE} with set-up and hold times referenced to this signal.

Power On

An initial pause of 200 μ s is required after power-up followed by a minimum of eight (8) initialization cycles (any combination of cycles containing a RAS clock such as RAS-only refresh) prior to normal operation. The current requirement of the HYB 4164 during power on is, however, dependent upon the input levels RAS, CAS and the rise time of $V_{\rm CC}$, as shown in the following diagram.

Data Output (DO)

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out has the same polarity as data-in. The output is in a high impedance state until $\overline{\text{CAS}}$ is brought low. In a read cycle or read-write cycle, the output goes active after completion of t_{RAC} (starting at $\overline{\text{RAS}}$ transition) as long as t_{RCD} (min) is satisfied, or after t_{CAC} starting at $\overline{\text{CAS}}$ transition when the transition occurs after t_{RCD} (max.). $\overline{\text{CAS}}$ going high returns the output to a high-impedance state. In an early write cycle the output is always in the high-impedance state. In a delayed write or read-modify-write cycle, the output will follow the sequence of the read cycle.

Hidden Refresh

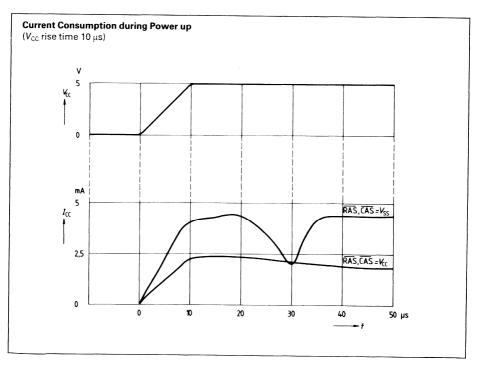
 $\overline{\text{RAS}}$ only refresh cycle may take place while maintaining valid output data. This feature is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{\text{CAS}}$ at the V_{IL} level of the previous memory read cycle.

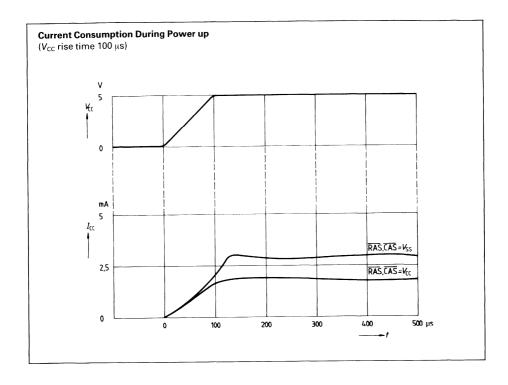
Refresh Cycle

A refresh operation must be performed at least every four milli-seconds to retain data. Since the output buffer is in the high-impedance state unless \overline{CAS} is applied, the \overline{RAS} only refresh sequence avoids any output signal during refresh. Strobing each of the 256 row addresses (A₀ through A₇) with \overline{RAS} causes all bits in each row to be refreshed. \overline{CAS} can remain high (inactive) for this refresh sequence to conserve power.

Page Mode

Page Mode operations allows a faster data transfer rate. This is achieved by maintaining the row address while strobing successive column addresses onto the chip. The time required to set-up and strobe sequential row addresses for the same page is eliminated.





Absolute Maximum Ratings 1)

Operating Temperature Range	0 to + 70 °C
Storage Temperature Range	-65 to +150 °C
Voltages on any Pin relative to V _{SS}	-1 to +7.0 V
Power Dissipation	1.0 W
Short Circuit Output Current	50 mA

A.C. Test Conditions

Input Pulse Levels		0.8 to 2.4 V
Input Rise and Fall Times	5 ns between	0.8 and 2.4 V
Input Timing Reference Levels		0.8 to 2.4 V
Output Timing Reference Levels		0.4 to 2.4 V
Output Load		Equivalent to 2 standard TTL Loads and 100 pF

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

 $T_A = 0 \text{ to } 70 \,^{\circ}\text{C}; \ V_{CC} = +5 \,\text{V} \pm 10\%$

Cumbal	Parameter	Limit	Values	Units	Test Conditions 11	
Symbol	rarameter	Min.	Min. Max.		Test Conditions	
V _{IH}	High level input voltage (all inputs) 2)	2.4	6.0		_	
V _{IL}	Low level input voltage 2)	-1.0	0.8	$]_{v}$		
V _{OH}	Output high voltage	2.4	V _{CC}] `	$I_0 = -5 \text{ mA}$	
V _{OL}	Output low voltage	-	0.4	1	$I_0 = 4.2 \text{ mA}$	
I _{CC1}	Average V _{CC} supply current ³⁾	-	27		-	
I _{CC2}	Standy V _{CC} supply current	-	3.5	mA	RAS at V _{IH} CAS at V _{IH}	
I _{CC3}	Average V _{CC} current during refresh ³⁾	-	24		RAS cycling CAS at V _{IH}	
I _{CC4}	Page mode current ³⁾	-	20	mA	RAS at V _{IL} CAS cycling	
I _{I(L)}	Input leakage current (any input) 4)	-10	10		-	
I _{O(L)}	Output leakage current	-10	10	Π μ Α	$\overline{\text{CAS}}$ at V_{IH} $V_{\text{O}} = V_{\text{SS}}$ to V_{CC}	

Capacitances 5)

Symbol	Parameter ⁶⁾	Limit Values		Units	Test Conditions	
	rarameter		Max.			
C ₁₁	Input capacitance (A ₀ -A ₇), DI	-	5		-	
C_{12}	Input capacitance RAS, CAS, WRITE	-	10	pF	-	
Co	Output capacitance	-	7		DO disabled	

Notes:

- 1) An initial pause of 200 µs is required after power-up followed by a minimum of eight initialization cycles prior to normal operation.
- 2) Over- and undershooting on input levels of 6.5 V or -2 V for a period of 30 ns will not influence function and reliability of the device.
- 3) I_{CC} depends on frequency of operation. Maximum current is measured at 260 ns cycle rate.
- 4) All device pins at 0 V and pin under test at +5.5 V.
- 5) Capacitance measured with a Boonton Meter 72 BD or effective capacitance calculated from the equation $C = \frac{I \cdot \triangle t}{\triangle V} \text{ with } \triangle V = 3 \text{ V}.$

$$C = \frac{1 + \Delta t}{A V}$$
 with $\Delta V = 3 V$

6) This parameter is periodically sampled and not 100% tested.

HYB 4164

A.C. Characteristics 1)

 $T_{A} = 0 \text{ to } +70 \,^{\circ}\text{C}; \ V_{CC} = +5 \, \text{V} \pm 10 \%$

Cumph = 1	Parameter	Limit Values						Units
Symbol	Parameter	HYB 4	1164-1	HYB 4	164-2	HYB 4	164-3	Onits
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{\rm RC}$	Random read or write cycle time 2)	220	-	280	_	330	_	
t _{RWC}	Read/write cycle time 2)	220		280	-	330	-	
t _{PC}	Page mode cycle time	125	_	170	_	225	-	
t _{RMWC}	Read/modify/write cycle time 2)	255	_	280	_	330	-	
t _{RAC}	Access time from RAS 3) 4)	_	120	-	150	-	200	
t_{CAC}	Access time from CAS 3) 5) 7)	-	80	-	100	_	135	
t _{OFF}	Output buffer turn-off delay 6)	_	35	_	40	_	50	
t _{RP}	RAS precharge time	90	_	100	-	120	_	
t _{RAS}	RAS pulse width	120	10 ⁴	150	10 ⁴	200	10 ⁴	
t _{RSH}	RAS hold time	80	-	100	-	135	_	
t _{CSH}	CAS hold time	120	-	150	-	200	_	ns
t _{CAS}	CAS pulse width	80	-	100	-	135	-	
t _{RCD}	RAS to CAS delay time 7)	25	40	30	50	35	65	
t _{ASR}	Row address set-up time	0	-	0	_	0	_	
t _{RAH}	Row address hold time	15	_	20	-	25	-	
t _{ASC}	Column address set-up time	0	-	-5	-	-5	-	
t _{CAH}	Column address hold time	40	-	45	_	55	_	
t _{AR}	Column address hold time referenced to RAS	80	_	95	_	120	-	
t _{RCS}	Read command set-up time (RMW)	0	-	0	-	0	_	
t _{RCH}	Read command hold time	0	_	0	-	0	-	
t_{WCH}	Write command hold time	40	_	45	_	55	_	

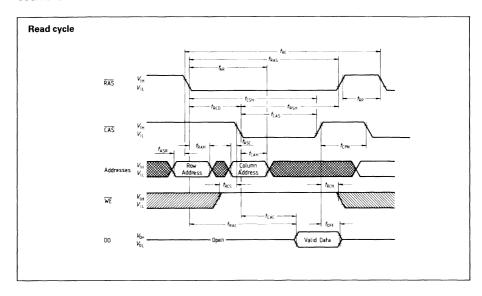
Symbol	Parameter	Limit Values						Units
Зуппоп		HYB 4164-1		HYB 4164-2		HYB 4164-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WCR}	Write command hold time referenced to RAS	95	-	110	-	120	-	
t _{wcs}	Write command set-up time 3)	-10	_	-10	-	-10	_	
t _{WP}	Write command pulse width	40	_	45	-	55	-	
t _{RWL}	Write command to RAS lead time	40	-	50	-	60	-	
t _{CWL}	Write command to CAS lead time	40	-	50	-	60	-	ns
t _{DS}	Data in set-up time	0	_	0	-	0	-	
t _{DH}	Data in hold time ⁹⁾	40	-	45	-	55	-	
t _{DHR}	Data in hold time ⁹⁾ reference to RAS	95	-	110	_	120	_	
$t_{\sf CP}$	CAS precharge time (Page mode)	35	-	60	-	80	-	
t _{CPN}	CAS precharge time ¹⁰	40	_	50	_	60	-	
t_{RF}	Refresh peroid	-	4.0	-	4.0	-	4.0	ms
t_{CWD}	CAS to WE delay 8)	60	_	60	-	80	-	
t_{RWD}	RAS to WE delay 8)	110	-	120	-	145	-	ns
t _T	Transition time (Rise and Fall)	3	35	3	35	3	50	

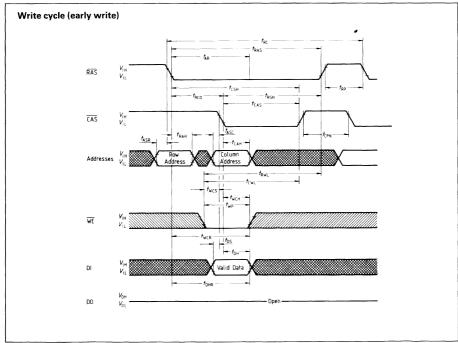
Notes:

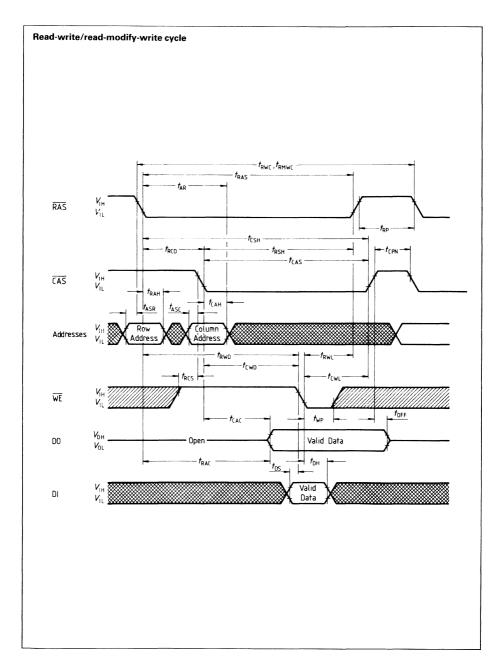
- V_{IH} and V_{IL} are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
- The specifications for t_{RC(min)} and t_{RWC(min)} are used only to indicate cycle time at which proper operation over full temperature range (0 °C ≤ T_A ≤ 70 °C) is assured
- Measured with a load equivalent to two standard TTL loads and 100 pF.
- Assumes that t_{RCD} ≤ t_{RCD(max)}. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
- 5) Assumes that $t_{RCD} \ge t_{RCD(max)}$.
- t_{OFF(max)} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

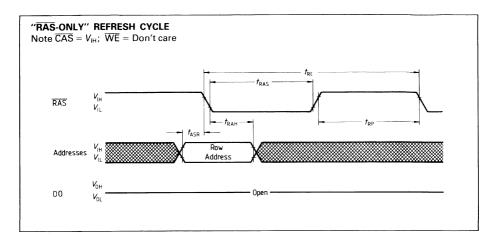
- 7) Operation within the $t_{RCD(max)}$ limit ensures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC} .
- 8) t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If t_{WCS} ≥ t_{WCS(min)}, the cycle is an early write cycle and the data-out will remain open circuit (high impedance) throughout the entire cycle: if t_{CWD} ≥ t_{CWD(min)} and t_{RWD} ≥ t_{RWD(min)} the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is met the condition of the data out (at access time) is indeterminate.
- 9) t_{DS} and t_{DH} are referenced to the leading edge of CAS in early write cycles, and to the leading edge of WE in delayed write or read-modify-write cycles.
- 10) Not for page mode.

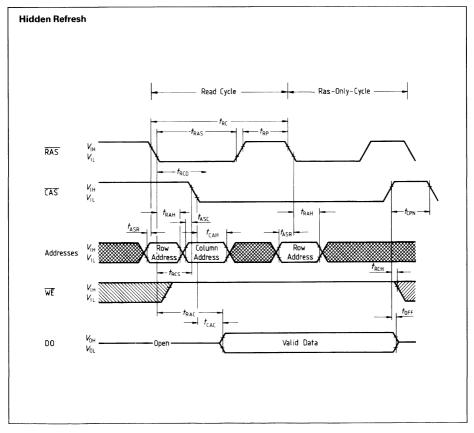
Waveforms

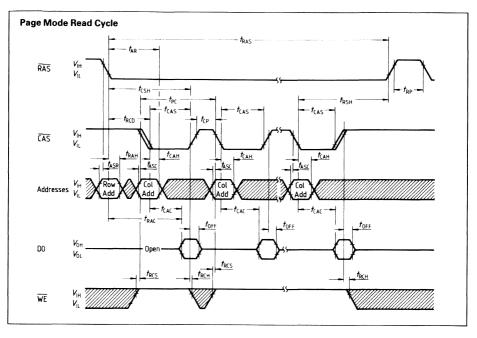


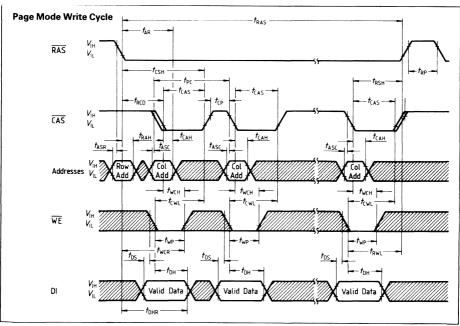






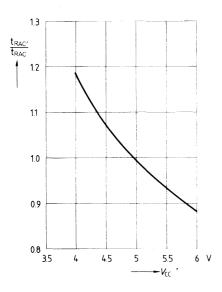




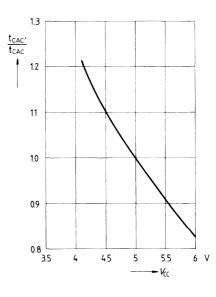


Typical Access Time Curves

RAS Access Time vs. Supply Voltage $T_A = 25$ °C

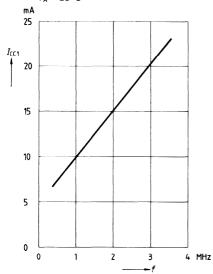


 $\overline{\text{CAS}}$ Access Time vs. Supply Voltage $T_{\text{A}} = 25\,^{\circ}\text{C}$

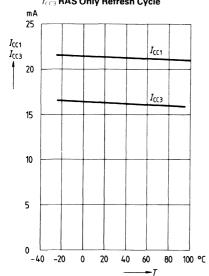


Typical Current Consumption Curves

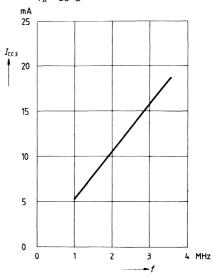




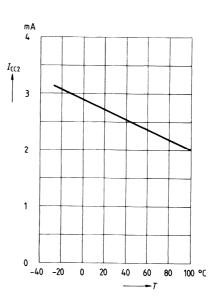
 $I_{\rm CC}$ (Average) vs. Temperature (Typ.) $V_{\rm CC} = 5.5$ V, $t_{\rm RC} = 280$ nsec $I_{\rm CC1}$ Write Cycle $I_{\rm CC3}$ RAS Only Refresh Cycle



 $I_{\rm CC3}$ (Average) vs. Cycle Rate $V_{\rm CC} = 5.5 \text{ V}$ RAS Only Refresh Cycle $T_{\rm A} = 25 \, ^{\circ}{\rm C}$



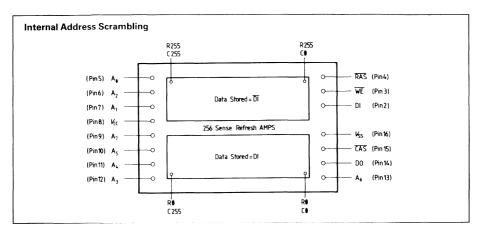
 $I_{\rm CC2}$ Standby Current vs. Temperature (Typ.) $V_{\rm CC} = 5.5~{
m V}$

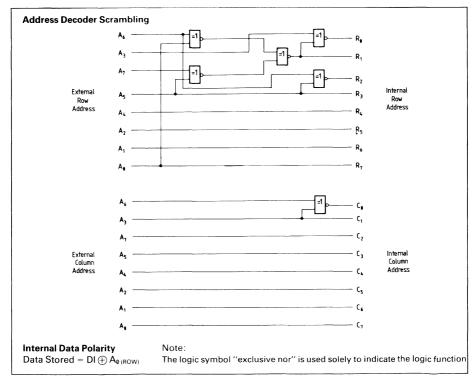


Address Decoder Scrambling

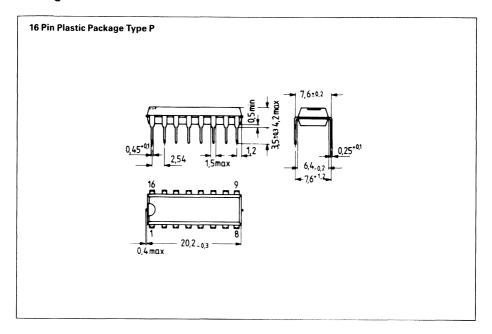
The evaluation and incoming testing of RAMs normally requires a description of the internal

address scrambling of the device in order to check the "worst case" pattern.





Package Outline



HYB 4164

Ordering Information

Туре	Description	Ordering Code
HYB 4164-P 1	RAM (Plastic; 120 ns)	Q67100-Q339
HYB 4164-P 2	RAM (Plastic; 150 ns)	Q 67100 - Q 325
HYB 4164-P 3	RAM (Plastic; 200 ns)	Q 67100 - Q 326

Advance history

HYB 41256-12/-15/-20 262,144-Bit Dynamic Random Access Memory (RAM)

Pin names

VSS

- 262,144 × 1-bit organization
- Industry standard 16 pins
- Single +5V supply, ±10% tolerance
- Low power dissipation:
 - -385 mW active (max.)
 - 28 mW standby (max.)
- 120 ns access time
 - 220 ns cycle time (HYB 41256-12) 150 ns access time

 - 260 ns cycle time (HYB 41256-15) 200 ns access time
 - 330 ns cycle time (HYB 41256-20)
- All inputs and outputs TTL compatible
- · On-chip substrate bias generator

- Three-state data output
- Read, write, read-modify-write, RAS-onlyrefresh, hidden refresh
- Common I/O capability using "early write" operation
- · Page mode read and write, read-write
- 256 refresh cycles with 4ms refresh period
- Redundancy incorporated for increasing yield
 - activation via laser links
 - roll-call mode as pretest with DI at 10V provides: redundancy signature individual address decoder scrambling

Pin configuration АВ П 1 16 TI VSS 15 TTAS DI 🛮 2 WE [] 3 14 DD RAS 13 ∏ A6 HYB 41256 12 A3 A0 🛮 5 11 🛮 A4 A2 ∏ 6 10 A5 A1 Γ ∏ A7 vcc [

A0-A8	Address Inputs	
CAS	Column Address Strobe	
DI	Data In	
DO	Data Out	
RAS	Row Address Strobe	
WE	Write Enable	
VCC	Power Supply (+5V)	

Ground (OV)

The HYB 41256 is a 262,144 word by 1-bit dynamic Random Access Memory. This 5V-only component is fabricated with Siemens new high performance N-channel silicon gate technology. The use of tantalum polycide provides high speed. A Siemens proprietary chip cover protects the chip against α radiation.

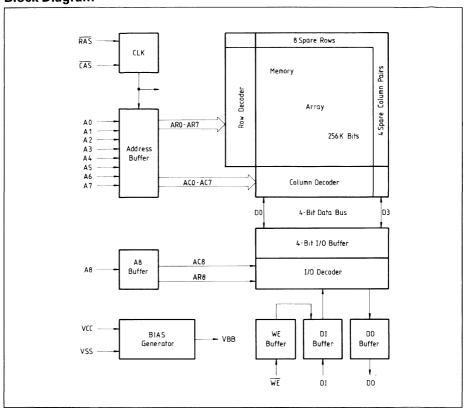
Nine multiplexed address inputs permit the HYB 41256 to be packaged in an industry standard 16-pin dual-in-line package. System-oriented features include single power supply with $\pm 10\%$ tolerance, on-chip address and data registers which eliminate the need for interface registers, and fully TTL compatible inputs and output, including clocks.

In addition to the usual read, write and readmodify-write cycles, the HYB 41256 is capable of early and late write cycles, RAS-only refresh, and hidden refresh. Common I/O capability is given by using early write operation.

The HYB 41256 also features page mode which allows high-speed random access of bits in the same row.

The HYB 41256 has the capability of using laser links to perform redundancy. With the roll-call mode, which is a new test feature, the user can separate repaired devices easily, and additionally gets information on the individual row and column addresses which have been repaired and how they are substituted by redundant lines. 10.84

Block Diagram



Functional Description

Device Initialization

Since the HYB 41256 is a dynamic RAM with a single 5V supply, no power sequencing is required. For power-up, an initial pause of 200 microseconds is necessary for the internal bias generator to establish the proper substrate bias voltage. To initialize the nodes of the dynamic circuitry, a minimum of 8 active cycles of the Row Address Strobe (RAS) has to be performed. This is also necessary after an extended inactive state of greater than 4 milliseconds.

Addressing (A0-A8)

For selecting one of the 262,144 memory cells, a total of 18 address bits are required. First 9 Row Address bits are set up on pins A0 through A8 and latched into the row address latches by the Row Address Strobe (\overline{RAS}). Then the 9 column address bits are set up on pins A0 through A8 and latched into the column address latches by the Column Address Strobe (\overline{CAS}). All input addresses must be stable on the falling edges of \overline{RAS} and \overline{CAS} . It should be noted that \overline{RAS} is similar to a Chip Enable in that it activates the sense amplifiers as well as the row decoder. \overline{CAS} is used as a chip select activating the column decoder and the input and output buffers.

Write enable (WE)

The read or write mode is selected with the \overline{WE} input. A logic high (VIH) on \overline{WE} dictates read mode; logic low (VIL) dictates write mode. The data input is disabled when read mode is selected. When \overline{WE} goes low prior to \overline{CAS} , data ouput (DO) will remain in the high-impedance state for the entire cycle permitting common I/O operation.

Data input (DI)

Data is written during a write or read-modify-write cycle. The falling edge of \overline{CAS} or \overline{WE} strobes data into the on-chip data latch. In an early write cycle \overline{WE} is brought low prior to \overline{CAS} and the data is strobed in by \overline{CAS} with setup and hold times referenced to this signal.

Data output (DO)

The output is three-state TTL compatible with a fan-out of two standard TTL loads. Data Out has the same polarity as Data In. The output is in a high impedance state until $\overline{\text{CAS}}$ is brought low. In a read cycle or read-write cycle, the output is valid after tRAC from transition of $\overline{\text{RAS}}$ when tRCD (min) is satisfied, or after tCAC from transition of $\overline{\text{CAS}}$ when the transition occurs after tRCD (max). In an early write cycle, the output is always in the high impedance state. In a delayed write or read-modifywrite cycle, the output will follow the sequence for the read cycle. With $\overline{\text{CAS}}$ going high the output returns to the high impedance state within tOFF.

Hidden refresh

RAS-only refresh cycle may take place while maintaining valid output data. This feature is referred to as Hidden Refresh. Hidden Refresh is performed by holding CAS at VIL of a previous memory read cycle.

Refresh cycle

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in the high impedance state unless CAS is applied, the RAS-only refresh sequence avoids any signal during refresh. Strobing each of the 256 row addresses (A0 through A7) with RAS, causes all bits in each row to be refreshed. CAS can remain high (inactive) for this refresh sequence to conserve power.

Page mode

Page-mode operation allows effectively faster memory access by maintaining the row address and strobing random column addresses onto the chip. Thus, the time necessary to setup and strobe sequential row addresses for the same page is no longer required. The maximum number of columns that can be addressed in sequence is determined by tRAS, the maximum RAS low pulse width.

Absolute Maximum Ratings*)

Operating Temperature Range
Storage Temperature Range
Voltage on Any Pin Relative to VSS
Voltage on DI Relative to VSS
-1 to 1V
Power Dissipation
Tw
Data Out Current (Short Circuit)

Ot 70 °C
-65 to 150 °C
-1 to 70 °C
-1 t

DC Characteristics

TA = 0 to 70 °C, VSS = OV, VCC = $+5 \text{ V} \pm 10 \%$

	Parameter	Limi	Limit values		T4	
Symbol		Min.	Max.	Unit	Test condition	
VIH	Input high voltage (all inputs)	2.4	VCC+1			
VIL	Input low voltage (all inputs)	-1.0	0.8	V	1) 2)	
VOH	Output high voltage	2.4	_			
VOL	Output low voltage		0.4			
ICC1	Average VCC supply current -12 tRC=220ns -15 tRC=260ns -20 tRC=330ns		85 70 60		3)	
ICC2	Standby VCC supply current		5		4)	
ICC3	Average VCC supply current during RAS-only refresh cycles -12 tRC=220ns -15 tRC=260ns -20 tRC=330ns		65 55 45	mA	3)	
ICC4	Average VCC supply current during page mode -12 tPC=120ns -15 tPC=150ns -20 tPC=200ns		65 55 45			
II(L)	Input leakage current (any input)		10			
IO(L)	Output leakage current (\overline{CAS} at logic 1, $0 \le V$ out ≤ 5.5)			μΑ		
VCC	VCC supply voltage	4.5	5.5	V	1)	
VSS	VSS supply voltage	0	0] '		

Notes see page 5

Capacitance

Symbol	Parameter	Limi	Limit values		
	1 di diffetei	Min.	Max.	Unit	rest condition
CI1	Input capacitance (A0-A8)		6		Test condition
CI2	Input capacitance (RAS, DI)		7	pF	
CI3	Input capacitance (CAS, WE)				
C0	Output capacitance (DO, CAS=VIH to disable output)		8		

5) Effective capacitance calculated from the equation

$$C = \frac{I - \Delta \, t}{\Delta \, V}$$
 with $\Delta \, V = 3V$ or measured with Boonton meter.

^{*)} Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

¹⁾ All voltages referenced to VSS.

²⁾ Overshooting and undershooting on input levels of 6.5V or –2V for a period of 30ns max. will not influence function and reliability of the device.

³⁾ ICC depends on frequency of operation. Maximum current is measured at the fastest cycle rate.

⁴⁾ RAS and CAS are both at VIH.

AC Test Conditions

Input pulse levels

0 to 3.0V

5ns between 0.8 and 2.4V Input rise an fall times Input timing reference levels

0.8 to 2.4V

Output timing reference levels

0.4 to 2.4V

Output load

equivalent to 2 standard

TTL loads and 100pF

AC Characteristics

TA=0 to 70 °C, VCC=5 V \pm 10% (unless otherwise specified; see notes 6, 7, 8)

			Limit values						
Symbol	Parameter	HYB 41256						Unit	
			-12		-15		-20		
		Min.	Max.	Min.	Max.	Min.	Max.		
tRC	Random read or write cycle time 9)	220		260	_	330			
tRWC	Read-modify-write cycle time 9)	265		310		390			
tRAC	Access time from RAS 10) 11)		120		150		200	ns	
tCAC	Access time from CAS 10) 11) 12)		60		75		100		
tRAS	RAS pulse width	120	10 ⁴	150	10 ⁴	200	10 ⁴		
tCAS	CAS pulse width	60	_	75	_	100	I —	1	
tREF	Refresh period	—	4		4	_	4	ms	
tRP	RAS precharge time	90		100		120			
tCRP	CAS to RAS precharge time	10]	10		10			
tRCD	RAS to CAS delay time 13)	30	60	30	75	35	100		
tRSH	RAS hold time	60		75		100		1	
tCSH	CAS hold time	120	1	150]	200			
tASH	Row address setup time	0	7	0	1	0	1		
tRAH	Row address hold time	20	1_	20	1-	25			
tASC	Column address setup time	0	1	0]	0			
tCAH	Column address hold time	30	1	30	1	35]_		
tAR	Column address hold time referenced to RAS 14)	90		105		135			
tT	Transition time (rise and fall) 6)	3	50	3	50	3	50	ns	
tRCS	Read command setup time			0		0			
tRCH	Read command hold time referenced to CAS 15)	0	_	0	_	0			
tRRH	Read command hold time referenced to RAS 15)	25		25		30			
tOFF	Output buffer turn-off delay 16)		30		40		50	1	
tWCS	Write command setup time 17]	0		0		0		1	
tWCH	Write command hold time	40	1-	45	1-	55	_		

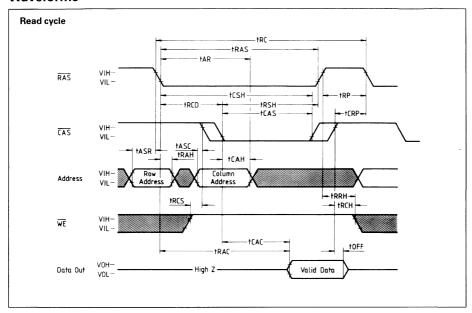
Notes see page 7

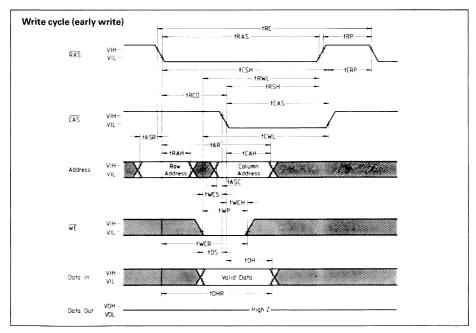
				Limit	values			1	
Symbol	Parameter		HYB 41256						
		_	-12 -			-2	0		
		Min.	Max.	Min.	Max.	Min.	Max.		
tWCR	Write command hold time referenced to RAS ¹⁴⁾	100		120		155			
tWP	Write command pulse width		1]		
tRWL	Write command to RAS lead time	40		45		55			
tCWL	Write command to CAS lead time								
tDS	Data in setup time 18)	0	1	0		0			
tDH	Data in hold time ¹⁸⁾	40	1	45		55]_		
tDHR	Data in hold time referenced to RAS ¹⁴⁾	100		120		155		ns	
tCWD	CAS to WE delay 17)	60		75		100			
tRWD	RAS to WE delay 17)	120		150	1	200			
tRRW	RMW cycle RAS pulse width	165		200	1	260			
tCRW	RMW cycle CAS pulse width	105		125	1	160			
tPC	Page mode cycle time 9)	120		150	1	200			
tPRWC	Page mode read-write cycle time	160		195	1	255			
tCP	Page mode CAS precharge time	50		65	1	90	1		

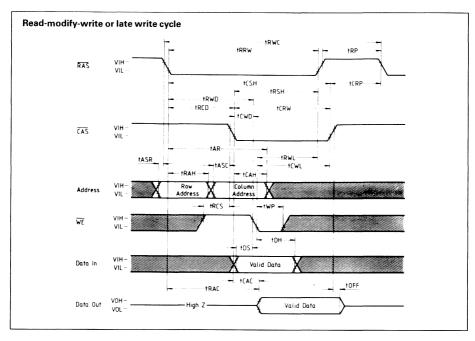
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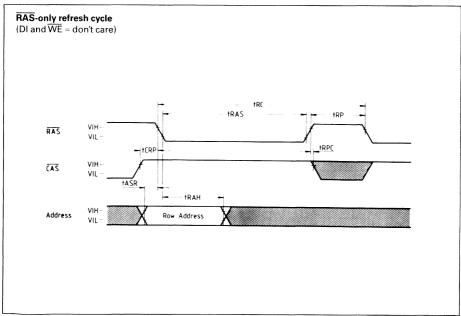
- 6) VIH and VIL are reference levels to measure timing of input signals. Also, transition times are measured between VIH and VIL.
- 7) An initial pause of 200 µs is required after power-up followed by a minimum of eight initialization cycles prior to normal operation.
- 8) The time parameters specified here are valid for a transition time of tT = 5ns for the input signals.
- 9) The specification for tRC (min), tRWC (min), and page-mode cycle time (tPC) are only used to indicate cycle time at which proper operation over full temperature range (0 °C \leq TA \leq 70 °C) is assured.
- 10) Measured with a load equivalent to two TTL loads and 100pF.
- 11) Assumes that tRCD ≤ tRCD (max). If tRCD is greater than the maximum recommended value shown in this table, tRAC will increase by the amount that tRCD exceeds the value shown.
- 12) Assumes that tRCD ≥ tRCD (max).
- 13) Operation within the tRCD (max) limit ensures that tRAC (max) can be met. tRCD (max) is specified as a reference point only; if tRCD is greater than the specified tRCD (max) limit, then access time is controlled exclusively by tCAC.
- 14) $tRCD + tCAH \ge tAR min, tRCD + tDH \ge tDHR min, tRCD + tWCH \ge tWCR min.$
- 15) Either tRRH or tRCH must be satisfied for a read cycle.
- 16) tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- 17) tWCS, tCWD and tRWC are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If tWCS ≥ tWCS (min), the cycle is an early write cycle and the Data Out will remain open circuit (high impedance) throughout the entire cycle; if tCWD ≥ tCWD (min) and tRWD ≥ tRWD (min) the cycle is a read-write cycle and the Data Out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the Data Out (at access time) is indeterminate.
- 18) tDS and tDH are referenced to the leading edge of CAS in early write cycles, and to the leading edge of WE in delayed write of read-modify-write cycles.

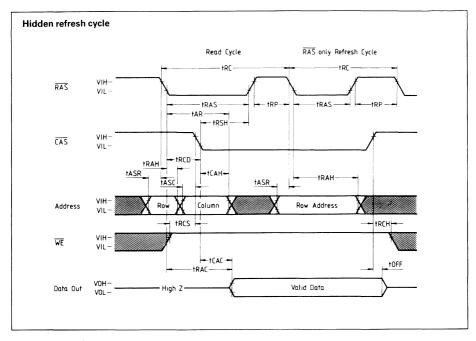
Waveforms

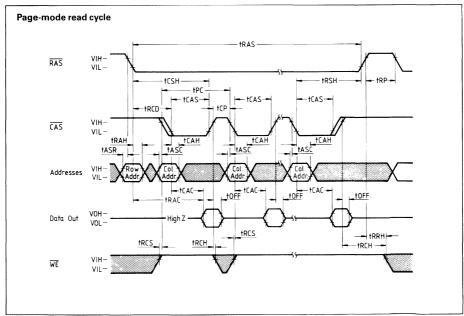


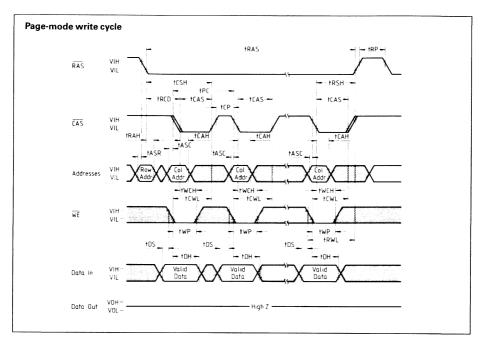


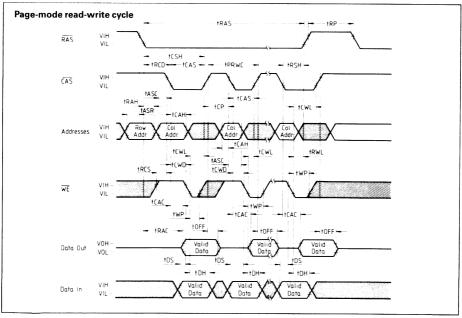






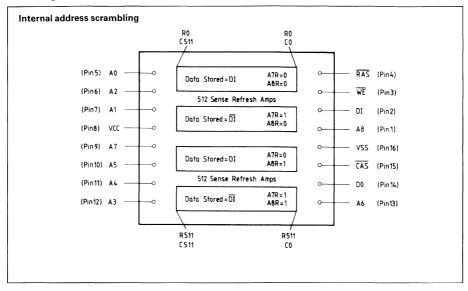


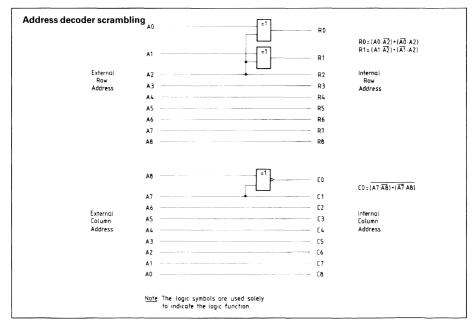




Address Decoder Scrambling (without redundancy)

The evaluation and incoming testing of RAMs normally requires a description of the internal address scrambling of the device in order to check for 'worst case' pattern.





Redundancy

Redundancy concept

The HYB 41526 takes advantage of the redundancy concept for increasing yield. This is done by providing the chip with a total of 8 spare rows and 4 spare column pairs. Two spare rows can be selected independently in each of four 64K cell arrays, and two spare column pairs can be selected independently in each of two 128K cell blocks. The spare lines can be selected by spare decoders which have to be programmed by laser technique during wafer probe.

Laser technology

For activation of redundant circuitry a laser pulse is used to open polycide links within the spare row and spare column decoders. The laser technique is used because it is mature and has proven reliable in a number of semiconductor applications including the implementation of redundant memory circuitry. Due to the fact, that the laser beam is very fine and can easily and accurately be positioned, and that it incorporates the energy for a controlled blow up of the polycide links, the laser technique is well suited for highly complex memory circuitry. All that results in a more efficient use of chip real estate.

Redundancy testability (roll-call mode)

With the redundancy concept two categories of devices, repaired and non-repaired ones, will be available. These two categories have to be separated easily and reliably by both, the manufacturer and the user (signature). When testing repaired devices, the reconfigurated address scrambling which results from activating spare rows and columns has to be taken into account for efficient device testing (individual bit map recognition).

The HYB 41256 has the capability of performing these two novel functions. It is done with a simple electrical test at the beginning of the final test or incoming inspection of each device (roll-call mode). The roll-call mode for performing both signature and individual bit map recognition can be activiated with DI at VIHR (10 V \pm 10%).

Signature

With DI at VIHR and performing at least one RASonly cycle with a cycle time of tRCR on any address combination, in the case of non-repaired devices the Data Output is in the high-performance state as in normal RAS-only cycles. For repaired devices the Data Output will go to VOLR or VOHR after the access time tRACR.

Individual bit map recognition

If the test for signature has shown a repaired device, additional tests can be performed to reognize which addresses have been repaired and how they are replaced by spare lines.

Row and column redundancy can be recognized independently.

Row redundancy

Row redundancy can be recognized with DI at VIHR and CAS at high, and RAS-only cycles on all 512 row address combinations. The data output is low (VOLR) for non-repaired addresses, and is high (VOHR) for repaired addresses only. Within each 64K cell array, spare row 1 is always used if only one row is to be replaced. If two rows are to be replaced in an 64K cell array, spare row 2 is used to replace the defective row with the higher address.

Column redundancy

Column redundancy can be recognized with DI at VIHR, and early write cycles with tRCDR ≤ tRCD (min) on all 512 column address combinations. A8 row must be used to distinguish between the two 128K cell blocks. The data output is low (VOLR) for non-repaired addresses, and high (VOHR) for repaired addresses. Within each 128K cell block, spare column pair 1 is always used if only one column is to be replaced. Otherwise, spare column pair 2 is used to replace the defective column with the higher address.

Recommended operating conditions

Roll-call mode

 $DC\ operating\ conditions\ and\ characteristics\ (Full\ operating\ voltage\ and\ temperature\ range\ unless\ otherwise\ specified.)$

			Limit values				
Symbol	Parameter	Min.	Тур.	Max.]		
VCC VSS	Supply voltage HYB 41256 –12, –15, –20 1)	4.75 0	5.0 0	5.25 0			
VIH	Logic 1 voltage: All inputs (except DI)	2.4		VCC+1			
VIHR	Logic 1 voltage: DI 1)2)	9.0	10	11	V		
VIL	Logic 0 voltage: All inputs 1)	-1.0		0.8	1		
VOHR	Output logic 1 voltage lout = -5 mA 1)	2.0	1-	_			
VOLR	Output logic 0 voltage lout = -4.2 mA 1)			0.4			

¹⁾ All voltages referenced to VSS.

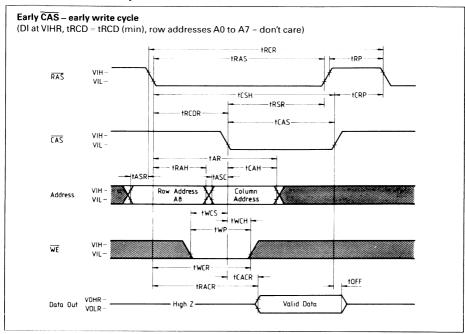
AC operating conditions and characteristics

(Full operating voltage and temperature range unless otherwise specified.)

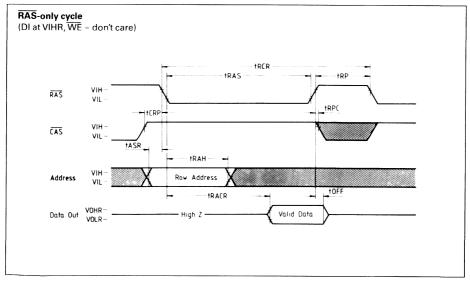
			Limit values						
Symbol	Parameter	_	HYB 41256						
		Min.	Max.	Min.	Max.	Min.	Max.		
tRCR	Roll-call cycle time	330	_	390	_	490			
tRCDR	Roll-call RAS to CAS delay	_	30		30	35	35]	
tRACR	Roll-call RAS access time	180		225		300	_	ns	
tCACR	Roll-call CAS access time	90		115		150			

²⁾ VIHR at DI must only be used for the roll-call-mode test and not for normal memory tests or applications. To avoid device damage, VIHR is to be applied after the initialization conditions (initial pause of $200\mu s$ and 8 cycles) have been satisfied, and must never exceed 11V.

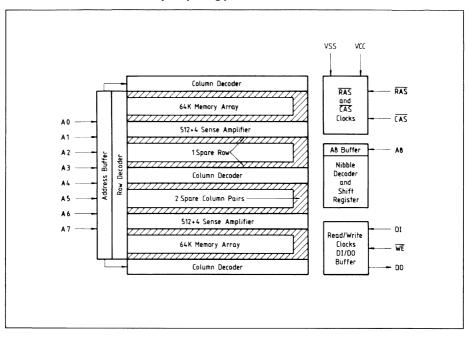
Column Redundancy



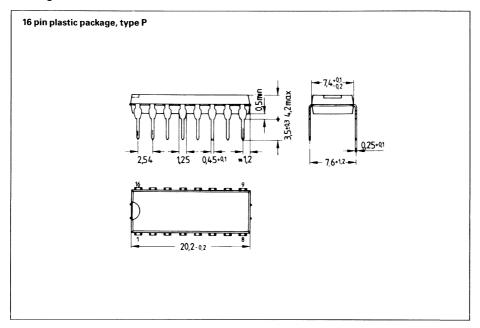
Row Redundancy and Signature



Siemens 256K DRAM Chip Topology



Package Outline



HYB 41256

Ordering Information

Туре	Description	Ordering code
HYB 41256-12	DRAM (access time 120 ns)	Q 67100-Q 346
HYB 41256-15	DRAM (access time 130 ns)	Q 67100-Q 347
HYB 41256-20	DRAM (access time 200 ns)	Q 67100-Q 348

HYB 41257-12/-15/-20 262,144-Bit Dynamic Random

- Access Memory (RAM)

 262,144 × 1-bit organization

 Fast nibble
- Single +5V supply, ±10% tolerance
- Low power dissipation:
 - 385 mW active (max.)

Industry standard 16 pins

- 28 mW standby (max.)
- 120 ns access time
 220 ns cycle time (HYB 41257-12)
 150 ns access time
 - 260 ns cycle time (HYB 41257-15)
 - 200 ns access time 330 ns cycle time (HYB 41257-20)
- All inputs and outputs TTL compatible
- Common I/O capability using "early write" operation
- Valid data during CAS precharge until start of next nibble cycle provides higher system data rate

- Fast nibble mode on read and write cycles via addresses A8 row and A8 column
 - 30 ns access time
 - 65 ns cycle time (HYB 41257-12)
 - 40 ns access time
 - 80 ns cycle time (HYB 41257-15)
 - 50 ns access time
 - 110 ns cycle time (HYB 41257-20)
- Read, write, read-modify-write, RAS-only-refresh, hidden refresh
- On-chip substrate bias generator
- · Three-state data output
- · 256 refresh cycles with 4 ms refresh period
- Redundancy incorporated for increasing yield
 - activation via laser links
 - roll-call-mode as pretest with DI at 10V provides: redundancy signature individual address decoder scrambling

Pin configuration				Pin name:	3
	A8 🗖 1	\circ	16 🛘 VSS	$\overline{A\emptyset - A8}$	Address Inputs
	D1 🗆 2		15 CAS	CAS	Column Address Strobe
	₩E [] 3 RAS [] 4 HYB	14 00	DI	Data In	
		13 🛮 A6	DO	Data Out	
	A0 [] 5		12 D A3	RAS	Row Address Strobe
	A2 [] 6 A1 [] 7		11 A4 10 A5	WE	Write Enable
VCC □ 8	9 A7	VCC	Power Supply (+5V)		
	···- <u>-</u>		VSS	Ground (0 V)	

The HYB 41257 is a 262,144 word by 1-bit dynamic Random Access Memory. This 5V-only component is fabricated with Siemens new high performance N-channel silicon gate technology. The use of tantalum polycide provides high speed. A Siemens proprietary chip cover protects the chip against α radiation.

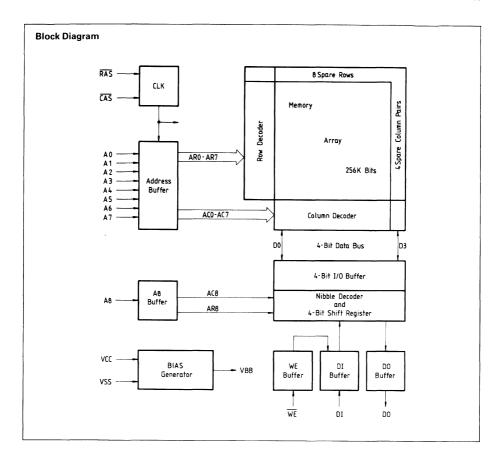
Nine multiplexed address inputs permit the HYB 41257 to be packaged in an industry standard 16-pin dual-in-line package. System-oriented features include single power supply with $\pm\,10\%$ tolerance, on-chip address and data registers which eliminate the need for interface registers, and fully TTL compatible inputs and output, including clocks. In addition to the usual read, write and readmodify-write cycles, the HYB 41257 is capable of

early and late write cycles, \overline{RAS} -only refresh, and hidden refresh. Common I/O capability is given by using "early write" operation.

Nibble Mode is a new feature of the HYB 41257 allowing the user to perform a serial access of 4 bits at a high data rate by using an on-chip nibble shift register which is controlled by one set of addresses on pin 1 (A8 Row and A8 Column) and the CAS clock only.

The HYB 41257 has the capability of using laser links to perform redundancy. With the roll-call mode, which is a new test feature, the user can separate repaired devices easily, and additionally gets information on the individual row and column addresses which have been repaired and how they are substituted by redundant lines.

12.84



Functional Description

Device Initialization

Since the HYB 41257 is a dynamic RAM with a single 5V supply, no power sequencing is required. For power-up, an initial pause of 200 microseconds is necessary for the internal bias generator to establish the proper substrate bias voltage. To initialize the nodes of the dynamic circuitry, a minimum of 8 active cycles of the Row Address Strobe (RAS) has to be performed. This is also necessary after an extended inactive state of greater than 4 milliseconds.

Adressing (A0-A8)

For selecting one of the 262,144 memory cells, a total of 18 address bits are required. First 9 Row Address bits are set up on pins A0 through A8 and latched into the row address latches by the Row Address Strobe (RAS). Then the 9 column address bits are set up on pins A0 through A8 and latched into the column address latches by the Column Address Strobe (CAS). All input addresses must be stable on the falling edges of RAS and CAS. It should be noted that RAS is similar to a Chip Enable in that it activates the sense amplifiers as well as the row decoder. CAS is used as a chip select activating the column decoder and the input and output buffers.

Write enable (WE)

The read or write mode is selected with the \overline{WE} input. A logic high (VIH) on \overline{WE} dictates read mode; logic low (VIL) dictates write mode. The data input is disabled when read mode is selected. When \overline{WE} goes low prior to \overline{CAS} , data output (DO) will remain in the high-impedance state for the entire cycle permitting common I/O operation.

Data Input (DI)

Data is written during a write or read-modify-write cycle. The falling edge of \overline{CAS} or \overline{WE} strobes data into the on-chip data latch. In an early write cycle \overline{WE} is brought low prior to \overline{CAS} and the data is strobed in by \overline{CAS} with setup and hold times referenced to this signal.

Data output (DO)

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data Out has the same polarity as Data In. The output is in a high impedance state until \overline{CAS} is brought low. In a read cycle or read-write cycle, the output is valid after tRAC from transition of \overline{RAS} when tRCD (min) is satisfied, or after tCAC from transition of \overline{CAS} when the transition occurs after tRCD (max.). In an early write cycle, the output is always in the impedance state. In a delayed write or read-modifywrite cycle, the output will follow the sequence for the read cycle. With \overline{CAS} going high and \overline{RAS} being high, the output returns to the high impedance state within tOFF.

For nibble-mode read cycles, the data output shows a novel function that gives advantages for system application. With RAS low the data output remains valid after and during CAS high. That gives time for a proper strobing of the data despite of system time tolerances, and increases the system data rate because the minimum CAS low time, tCAS and tNAS, can be realized more easily. With CAS going low for the next nibble cycle the data output returns to the high-impedance state within tNOFF. In a read, late write, or read-modify-write mode for a normal cycle or the last nibble cycle, the data output condition depends on whether CAS or RAS is brought high first. With CAS going high and RAS at low, the data output is valid until RAS goes high and returns to the high-impedance state within tOFF referenced to RAS. With CAS being low at RAS high, the data output is valid until CAS goes high and returns to the high-impedance state within tOFF referenced to CAS.

Hidden refresh

RAS-only refresh cycle may take place while maintaining valid output data. This feature is referred to as Hidden Refresh. Hidden Refresh is performed by holding CAS at VIL of a previous memory read cycle.

Refresh cycle

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in the high impedance state unless CAS is applied, the RAS-only refresh sequence avoids any output signal during refresh. Strobing each of the 256 row addresses (A0 through A7) with RAS causes all bits in each row to be refreshed. CAS can remain high (inactive) for this refresh sequence to conserve power.

Nibble-mode cycle

Nibble-mode operation allows a very fast serial data streaming up to 4 bits by applying only one set of addresses for the first bit to be accessed as normal (tCAC). By holding RAS low, only CAS has to be cycled up and then down for reading or writing the next 3 bits at a high data rate with tNAC tCAC. After 4 bits have been accessed, the following bit will be the same as the first bit accessed. Address on pin 1 (row address A8 and column address A8) is used to select 1 of the 4 nibble bits for initial access. Toggling CAS causes row A8 and column A8 to be incremented by the internal shift register with A8 row being the least significant address, and allows access to the next nibble bit. In nibble mode, any combination of read, write, and read-modify-write operation is possible (e.g. first bit: read; second bit: write; third bit: readmodify-write, etc.).

Absolute Maximum Ratings *)

Operating Temperature Range 0 to + 70 °C Storage Temperature Range -65 to +150 °C Voltages on Any Pin Relative to VSS -1 to +7 V Voltage on DI Relative to VSS -1 to +11 V Power Dissipation 1W Data Out Current (Short Circuit) 50 mA

D.C. Characteristics

TA = 0 to 70 °C, VSS = 0V, VCC = $+5V \pm 10\%$

C b l	D	Limi	Limit Values			
Symbol	Parameter	Min.	Max.	Unit	Test condition	
VIH	Input high voltage (all inputs)	2.4	VCC+1		1) 2)	
VIL	Input low voltage (all inputs)	-1.0	0.8]	', =',	
voн	Output high voltage	2.4	_	*	_	
VOL	Output low voltage		0.4			
ICC1	Average VCC supply current - 12 tRC = 220 ns - 15 tRC = 260 ns - 20 tRC = 330 ns		85 70 60		3)	
ICC2	Standy VCC supply current		5		4)	
ICC3	Average VCC supply current during RAS-only refresh cycles - 12 tRC = 220 ns - 15 tRC = 260 ns - 20 tRC = 330 ns		65 55 45	mA	3)	
ICC6	Average VCC supply current during nibble mode - 12 tNC = 65 ns - 15 tNC = 80 ns - 20 tNC = 110 ns		10 8 7			
II(L)	Input leakage current (any input)		10	μΑ	_	
IO(L)	Output leakage current ($\overline{\text{CAS}}$ at logic 1, $0 \le \text{Vout} \le 5.5$)			l ma		
VCC	VCC supply voltage	4.5	5.5	V	1)	
VSS	VSS supply voltage	0	0	\ \ \	''	

Notes see page 5

Capacitance

Symbol		Limit	t values	Unit	Toot condition		
	Parameter	Min.	Max.	Unit	nit Test condition		
CI1	Input capacitance (A0-A8)		6		5)		
CI2	Input capacitance (RAS, DI)		7	pF			
CI3	Input capacitance (CAS, WE)		8] P'			
CO	Output capacitance (D0, CAS = VIH to disable output)						

^{*)} Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

¹⁾ All voltages referenced to VSS.

²⁾ Overshooting and undershooting on input levels of $6.5 \, \text{V}$ or $-2 \, \text{V}$ for a period of 30 ns max. will not influence function and reliability of the device.

³⁾ ICC depends on frequency of operation. Maximum current is measured at the fastest cycle rate.

⁴⁾ RAS and CAS are both at VIH.

⁵⁾ Effective capacitance calculated from the equation C = $\frac{I \cdot \triangle t}{\triangle V}$ with $\triangle V = 3 V$ or measured with Boonton meter.

A.C. Test Conditions

Input pulse levels 0 to 3.0 V
Input rise an fall times 5 ns between 0.8 and 2.4 V
Input timing reference levels 0.8 to 2.4 V
Output timing reference levels 0.4 to 2.4 V

Output load equivalent to 2 standard TTL loads and 100 pF

A.C. Characteristics

TA = 0 to \pm 70 °C; VCC = \pm 5 V \pm 10% (unless otherwise specified; see notes 6, 7, 8)

Symbol	Parameter		Limit values						
Syllibol	Talametel				41257-			Unit	
			- 12		- 15		-20		
		Min.	Max.	Min.	Max.	Min.	Max.		
tRC	Random read or write cycle time 9)	220	_	260	_	330	-		
tRWC	Read-modify-write cycle time 9)	265		310		390			
tRAC	Access time from RAS 10) 11)		120	_	150	_	200	ns	
tCAC	Access time from CAS 10) 11) 12)		60		75		100		
tRAS	RAS pulse width	120	10 ⁴	150	10 ⁴	200	10 ⁴		
tCAS	CAS pulse width	60	_	75	_	100	-		
tREF	Refresh period	-	4	-	4	_	4	ms	
tRP	RAS precharge time	90		100		120			
tCRP	CAS to RAS precharge time	10]	10	1	10		ns	
tRCD	RAS to CAS delay time 13)	30	60	30	75	35	100		
tRSH	RAS hold time	60		75		100			
tCSH	CAS hold time	120		150		200			
tASR	Row address setup time	0	1	0		0			
tRAH	Row address hold time	20	_	20	-	25]_		
tASC	Column address setup time	0		0		0			
tCAH	Column address hold time	30	1	30		35	1_		
tAR	Column address hold time referenced to RAS 14)	90		105		135			
tΤ	Transition time (rise and fall) 6)	3	50	3	50	3	50	ns	
tRCS	Read command setup time	0				0			
tRCH	Read command hold time referenced to CAS 15)	0	_	0	_	U			
tRRH	Read command hold time referenced to RAS 15)	25		25		30			

Notes see page 8

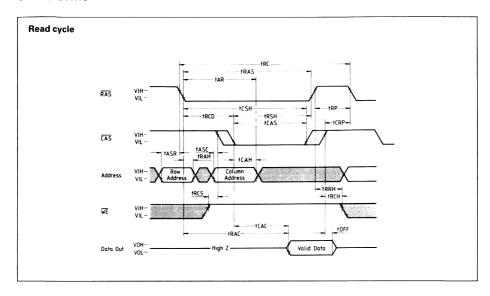
Symbol	Parameter			Limit	values			Unit
Symbol	raiametei		10		41257- - 15		- 20	Omi
		Min.	– 12 Max.	Min.	Max.	Min.	Max.	
tOFF	Output buffer turn-off delay 16)		30		40	0	50	
tWCS	Write command setup time 17)	0		0				
tWCH	Write command hold time	40	1-	45	1	55	-	
tWCR	Write command hold time referenced to RAS 14)	100		120		155		
tWP	Write command pulse width		1					
tRWL	Write command to RAS lead time	40		45		55		
tCWL	Write command to CAS lead time							
tDS	Data in setup time 18)	0		0		0		
tDH	Data in hold time 18)	40		45]_	55		
tDHR	Data in hold time referenced to RAS 14)	100		120		155		ns
tCWD	CAS to WE delay 17)	60	1	75		100		
tRWD	RAS to WE delay 17)	120		150		200		
tRRW	RMW cycle RAS pulse width	165		200		260		
tCRW	RMW cycle CAS pulse width	105		125		160		
tNC	Nibble-mode cycle time 9)	65		80		110	_	
tNAC	Nibble-mode access time from CAS 10)	-	30	_	40	_	50	
tNAS	Nibble-mode setup time	30		40				
tNP	Nibble-mode precharge time	25]	30		50		
tNRSH	Nibble-mode RAS hold time	30		40				
tNCWD	Nibble-mode CAS to WE delay]-		_		_	
tNCRW	Nibble-mode RMW CAS pulse width	65		85		105		
tNCWL	Nibble-mode WE to CAS lead time	30		40		50		
tNWRH	Nibble-mode write RAS hold time	45		55		75		
tNOFF	Nibble-mode output buffer turn-off delay 19)	0		0		0		
tNWP	Nibble-mode WE pulse width	30		40		50		
tNWCH	Nibble-mode WE command hold time	30						

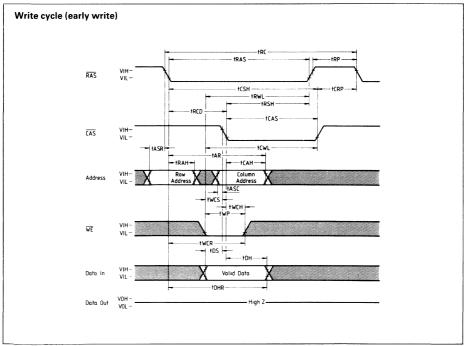
Notes see page 8

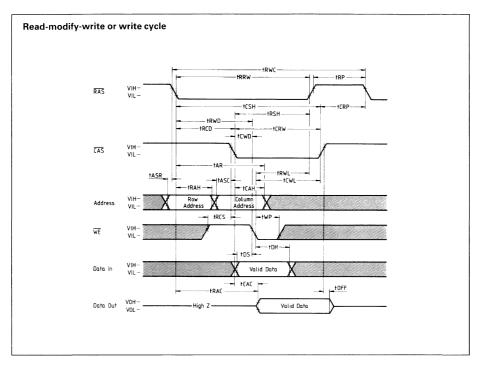
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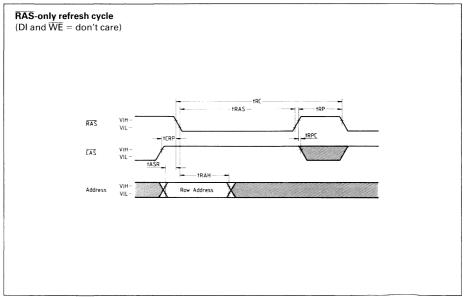
- 6) VIH and VIL are reference levels to measure timing of input signals. Also, transition times are measured between VIH and VIL.
- 7) An initial pause of 200 µs is required after powerup following by a minimum of eight initialization cycles prior to normal operation.
- 8) The time parameters specified here are valid for a transition time of tT = 5 ns for the input signals.
- 9) The specifications for tRC (min), tRWC (min), and nibble cycle time (tNC) are only used to indicate cycle time at which proper operation over full temperature range (0 °C \leq TA \leq 70 °C) is assured.
- 10) Measured with a load equivalent to two TTL loads and 100 pF.
- 11) Assumes that tRCD ≤ tRCD(max). If tRCD is greater than the maximum recommended value shown in this table, tRAC will increase by the amount that tRCD exceeds the value shown.
- 12) Assumes that tRCD ≥ tRCD (max).
- 13) Operation within the tRCD (max) limit ensures that tRAC (max) can be met. tRCD (max) is specified as a reference point only; if tRCD is greater than the specified tRCD (max) limit, then access time is controlled exclusively by tCAC.
- 14) $tRCD + tCAH \ge tAR min, tRCD + tDH \ge tDHR min, tRCD + tWCH \ge tWCR min.$
- 15) Either tRRH or tRCH must be satisfied for a read cycle.
- 16) tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels. tOFF is referenced either to the CAS leading edge with RAS being high or to the RAS leading edge with CAS being high.
- 17) tWCS, tCWD and tRWC are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If tWCS ≥ tWCS(min), the cycle is an early write cycle and the Data Out will remain open circuit (high impedance) throughout the entire cycle; if tCWD ≥ tCWD (min) and tRWD ≥ tRWD (min) the cycle is a read-write cycle and the Data Out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the Data Out (at access time) is indeterminate.
- 18) tDS and tDH are referenced to the leading edge of CAS in early write cycles, and to the leading edge of WE in delayed write or read-modify-write cycles.
- 19) tNOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels. tNOFF is referenced to the CAS falling edge of the next nibble cycle with RAS being low.

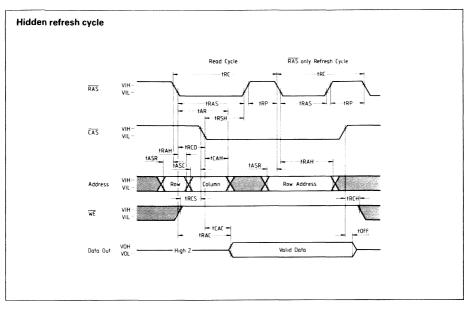
Waveforms

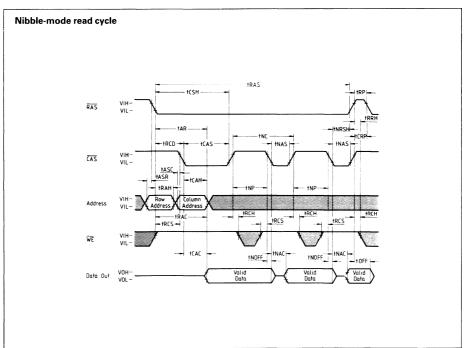


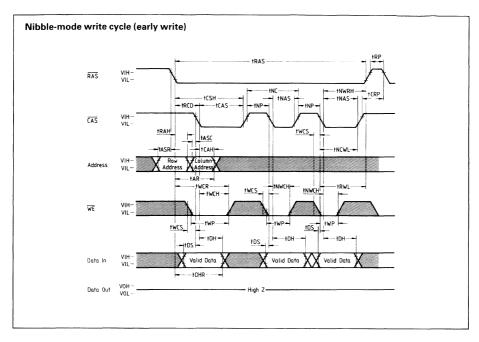


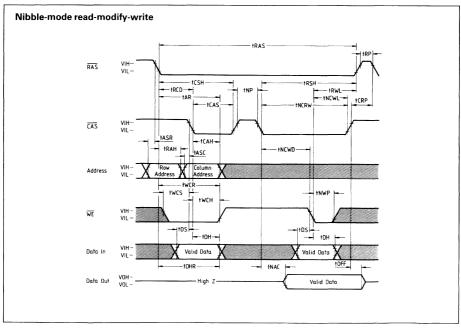








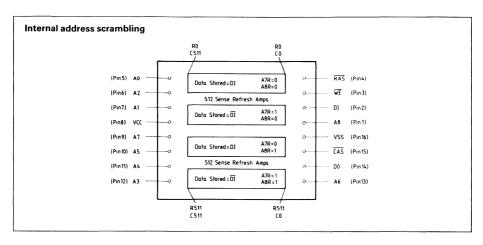


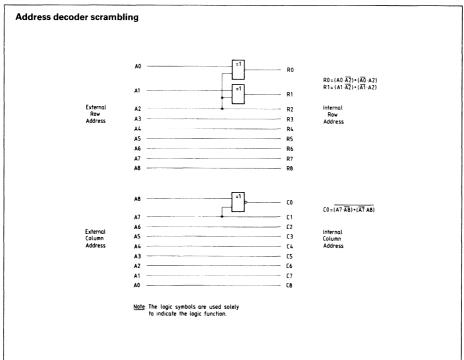


Address Decoder Scrambling (without redundancy)

The evaluation and incoming testing of RAMs normally requires a description of the internal

address scrambling of the device in order to check for 'worst case' pattern.





Redundancy

Redundancy concept

The HYB 41257 takes advantage of the redundancy concept for increasing yield. This is done by providing the chip with a total of 8 spare rows and 4 spare column pairs. Two spare rows can be selected independently in each of four 64K cell arrays, and two spare column pairs can be selected independently in each of two 128K cell blocks. The spare lines can be selected by spare decoders which have to be programmed by laser technique during wafer probe.

Laser technology

For activation of redundant circuitry a laser pulse is used to open polycide links within the spare row and spare column decoders. The laser technique is used because it is mature and has proven reliable in a number of semiconductor applications including the implementation of redundant memory circuitry. Due to the fact, that the laser beam is very fine and can easily and accurately be positioned, and that it incorporates the energy for a controlled blow up of the polycide links, the laser technique is well suited for highly complex memory circuitry. All that results in a more efficient use of chip real estate.

Redundancy testability (roll-call mode)

With the redundancy concept two categories of devices, repaired and non-repaired ones, will be available. These two categories have to be separated easily and reliably by both, the manufacturer and the user (signature). When testing repaired device, the reconfigurated address scrambling which results from activating spare rows and columns has to be taken into account for efficient device testing (individual bit map recognition).

The HYB 41257 has the capability of performing these two novel functions. It is done with a simple electrical test at the beginning of the final test or incoming inspection of each device (roll-call mode). The roll-call mode for performing both signature and individual bit map recognition can be activated with DI at VIHR (10V ± 10%).

Signature

With DI at VIHR and performing at least one RASonly cycle with a cycle time of tRCR on any address combination, in the case of non-repaired devices the Data Output is in the high-impedance state as in normal early write cycles. For repaired devices the Data Output will go to VOLR or VOHR after the access time tRACR.

Individual bit map recognition

If the test for signature has shown a repaired device, additional tests can be performed to recognize which addresses have been repaired and how they are replaced by spare lines. Row and column redundancy can be recognized independently.

Row redundancy

Row redundancy can be recognized with DI at VIHR and \overline{CAS} at high, and \overline{RAS} -only cycles on all 512 row address combinations. The data output is low (VOLR) for non-repaired addresses, and is high (VOHR) for repaired addresses only. Within each 64K cell array, spare row 1 is always used if only one row is to be replaced. If two rows are to be replaced in an 64K cell array, spare row 2 is used to replace the defective row with the higher address.

Column redundancy

Column redundancy can be recognized with DI at VIHR, and early write cycles with tRCDR ≤ tRCD (min) on all 512 column address combinations.

A8 row must be used to distinguish between the two 128K cell blocks. The data output is low (VOLR) for non-repaired addresses, and high (VOHR) for repaired addresses. Within each 128K cell block, spare column pair 1 is always used if only one column is to be replaced. Otherwise, spare column pair 2 is used to replace the defective column with the higher address.

Recommended operating conditions

Roll-call mode

DC operating conditions and characteristics (Full operating voltage and temperature range unless otherwise specified).

Cumbal	Parameter		ues	Unit	
Symbol	r drameter	Min.	Typ.	Max.	Unit
VCC VSS	Supply voltage HYB 41257-12, -15, -20 1) 1)	4.75 0	5.0 0	5.25 0	
VIH	Logic 1 voltage: All inputs (except DI)	2.4	_	VCC+1	
VIHR	Logic 1 voltage: DI 1) 2)	9.0	10	11	\Box_{v}
VIL	Logic 0 voltage: All inputs 1)	-1.0		0.8	
VOHR	Output logic 1 voltage lout = -5mA 1)	2.0	_	_	
VOLR	Output logic 0 voltage lout = -4.2 mA 1)	-		0.4	

A.C. operating conditions and characteristics

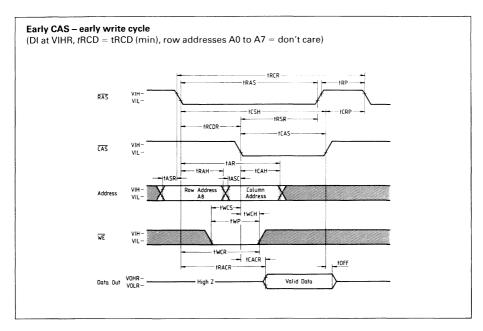
(Full operating voltage and temperature range unless otherwise specified.)

Symbol	Parameter	Limit values							
Symbol	T drameter		HYB 41257-						
			- 12		- 15	-20			
		Min.	Max.	Min.	Max	Min.	Max.		
tRCR	Roll-call cycle time	330	-	390	-	490	-		
tRCDR	Roll-call RAS to CAS delay	_	30	-	30	_	35	ns	
tRACR	Roll-call RAS access time		180		225		300		
tCARC	Roll-call CAS access time		90		115		150		

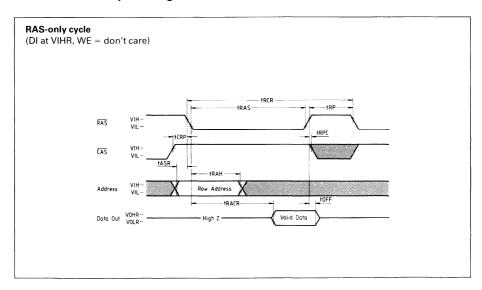
¹⁾ All voltages referenced to VSS.

²⁾ VIHR at DI must only be used for the roll-call mode test and not for normal memory tests or applications. To avoid device damage, VIHR is to be applied after the initialization conditions (initial pause of 200 ms and 8 cycles) have been satisfied, and must never exceed 11V.

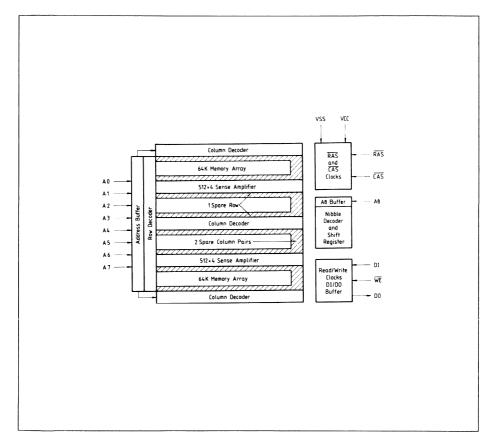
Column Redundancy



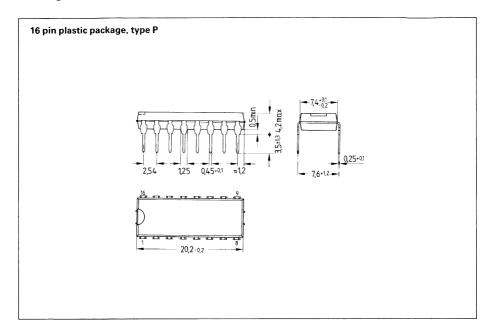
Row Redundancy and Signature



Siemens 256K DRAM Chip Topology



Package Outline



Ordering Information

Туре	Description	Ordering code
HYB 41257-12	DRAM (access time 120 ns)	Q67100-Q349
HYB 41257-15	DRAM (access time 150 ns)	Q67100-Q350
HYB 41257-20	DRAM (access time 200 ns)	Q67100-Q351



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Notes

Notes

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